The Engineering Staff of
TEXAS INSTRUMENTS INCORPORATED
Semiconductor Group

Memories for 9900 Microprocessors

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TEXAS INSTRUMENTS

TABLE OF CONTENTS

SUMMARY SCHOTTKY TTL MEMORIES

FIELD PROGRAMMABLE READ-ONLY MEMORY (PROM) LINE SUMMARY (SEE PAGE)

MASK-PROGRAMMED READ-ONLY MEMORY (ROM) LINE SUMMARY

TYPE NUMBER (PACKAGES)		TYPE OF OUTPUT(S)	BIT SIZE (ORGANIZATION)	TYPICAL PERFORMANCE		SEE PAGE
−55°C to 125°C	0° to 70°C			ADDRESS ACCESS TIME	POWER DISSIPATION	
SN5488A(J, W)	SN7488A(J, N)	Open-Collector	256 Bits (32 W x 8 B)	26 ns	320 mW	7
SN54187(J, W)	SN74187(J, N)	Open-Collector	1024 Bits (256 W x 4 B)	40 ns	460 mW	7
SN54S270(J)	SN74S270(J, N)	Open-Collector	2048 Bits (512 W x 4 B)	45 ns	525 mW	7
SN54S370(J)	SN74S370(J, N)	3-State				
SN54S271(J)	SN74S271(J, N)	Open-Collector	2048 Bits (256 W x 8 B)	45 ns	525 mW	7
SN54S371(J)	SN74S371(J, N)	3-State				

READ/WRITE MEMORY (RAM) LINE SUMMARY

TYPE NUMBER (PACKAGES)		BIT SIZE (ORGANIZATION)	OUTPUT CONFIGURATION	TYPICAL PERFORMANCE		SEE PAGE
−55°C to 125°C	0°C to 70°C			ADDRESS ACCESS TIME	POWER DISSIPATION	
SN54S189(J, W)	SN74S189(J, N)	64 bits (16 W x 4B)	Three-state	25 ns	375 mW	15
SN54S289(J, W)	SN74S289(J, N)		Open-Collector			
SN54S200A(J, W)	SN74S200A(J, N)	256 bits (256 W x 1B)	Three-State	25 ns	500 mW	19
SN54LS200A(J, W)	SN74LS200A(J, N)			35 ns	275 mW	
SN54LS202(J, W)	SN74LS202(J, N)				275/100* mW	
SN54S300A(J, W)	SN74S300A(J, N)		Open-Collector	25 ns	500 mW	
SN54LS300A(J, W)	SN74LS300A(J, N)			35 ns	275 mW	
SN54LS302(J, W)	SN74LS302(J, N)				275/100* mW	
	SN74S214A(J, N)	1024 bits (1024 W x 1B)	Three-State	30 ns	550 mW	25
SN54S214(J)	SN74S214(J, N)			40 ns	550 mW	
SN54LS214(J)	SN74LS214(J, N)			65 ns	200 mW	
SN54LS215(J)	SN74LS215(J,N)			75 ns	200/100*mW	
	SN74S314A(J, N)		Open-Collector	30 ns	550 mW	
SN54S314(J)	SN74S314(J, N)			40 ns	550 mW	
SN54LS314(J)	SN74LS314(J, N)			75 ns	200 mW	
SN54LS315(J)	SN74S314(J, N)			75 ns	200/100*mW	
SN54S207(J)	SN74S207(J, N)	1024 bits (256 W x 4B)	Three-State	40 ns	600 mW	
SN54LS207(J)	SN74LS207(J, N)			75 ns	200 mW	
SN54S208(J)	SN74S208(J,N)			40 ns	600 mW	
SN54LS208(J)	SN74LS208(J,N)			75 ns	200 mW	
SN54S400(J)	SN74S400(J, N)	4096 bits (4096 W x 1B)	Three-State	75 ns	500 mW	37
SN54S401(J)	SN74S401(J, N)		Open-Collector			

FIRST-IN/FIRST-OUT (FIFO) MEMORY

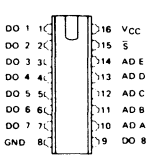
TYPE NUMBER (PACKAGES)	BIT SIZE (ORGANIZATION)	TYPICAL PERFORMANCE				SEE PAGE
		DATA RATES		FALL THROUGH	POWER DISSIPATION	
		INPUT	OUTPUT			
SN74S225(J, N)	80 bits (16 W x 5B)	d-c to 10 MHz	d-c to 10 MHz	215 ns	400 mW	39

*Powered down

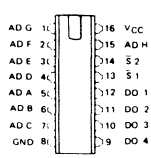
- Titanium-Tungsten (Ti-W) Fuse Links for Fast, Low-Voltage, Reliable Programming
- All Schottky-Clamped PROM's Offer:
  - Fast Chip Select to Simplify System Decode
  - Choice of Three-State or Open-Collector Outputs
  - P-N-P Inputs for Reduced Loading on System Buffers/Drivers
- Full Decoding and Chip Select Simplify System Design
- Applications Include:
  - Microprogramming/Firmware Loaders
  - Code Converters/Character Generators
  - Translators/Emulators
  - Address Mapping/Look-Up Tables

TYPE NUMBER (PACKAGES)		BIT SIZE (ORGANIZATION)	OUTPUT CONFIGURATION	TYPICAL PERFORMANCE	
−55°C to 125°C	0°C to 70°C			ADDRESS ACCESS TIME	POWER DISSIPATION
54S188(J, W)	SN74S188(J, N)	256 bits (32 W x 8 B)	open-collector	25 ns	400 mW
SN54S288(J, W)	SN74S288(J, N)		three-state		
SN54S287(J, W)	SN74S287(J, N)	1024 bits (256 W x 4 B)	three-state	42 ns	500 mW
SN54S387(J, W)	SN74S387(J, N)		open-collector		
SN54S470(J)	SN74S470(J, N)	2048 bits (256 W x 8 B)	open-collector	50 ns	550 mW
SN54S471(J)	SN74S471(J, N)		three-state		
SN54S472(J)	SN74S472(J, N)	4096 bits (512 W x 8 B)	three-state	55 ns	600 mW
SN54S473(J)	SN74S473(J, N)		open-collector		
SN54S474(J, W)	SN74S474(J, N)	4096 bits (512 W x 8 B)	three-state	55 ns	600 mW
SN54S475(J, W)	SN74S475(J, N)		open-collector		

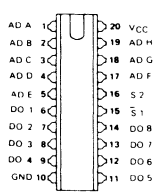
256 BITS (32 WORDS BY 8 BITS) 'S188, 'S288



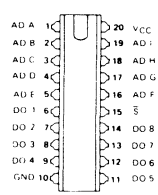
1024 BITS (256 WORDS BY 4 BITS) 'S287, 'S387



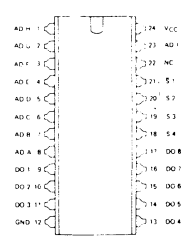
2048 BITS (256 WORDS BY 8 BITS) 'S470, 'S471



4096 BITS (512 WORDS BY 8 BITS) 'S472, 'S473



4096 BITS (512 WORDS BY 8 BITS) 'S474, 'S475



Pin assignments for all of these memories are the same for all packages.

description

These monolithic TTL programmable read-only memories (PROM's) feature titanium-tungsten (Ti-W) fuse links with each link designed to program in one millisecond or less. These PROM's offer considerable flexibility for upgrading existing designs or improving new designs as they feature full Schottky clamping for improved performance, low-current MOS-compatible p-n-p inputs, choice of bus-driving three-state or open-collector outputs, and improved chip-select access times.

The high-complexity 2048- and 4096-bit 20-pin PROM's can be used to significantly improve system density for fixed memories as all are offered in a dual-in-line package having pin-row spacings of 0.300 inch.

†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U. S. Patent Number 3,463,975.

description (continued)

Data can be electronically programmed, as desired, at any bit location in accordance with the programming procedure specified. All PROM's, except the 'S287 and 'S387, are supplied with a low-logic-level output condition stored at each bit location. The programming procedure open-circuits Ti-W metal links, which reverses the stored logic level at selected locations. The procedure is irreversible; once altered, the output for that bit location is permanently programmed. Outputs never having been altered may later be programmed to supply the opposite output level. Operation of the unit within the recommended operating conditions will not alter the memory content.

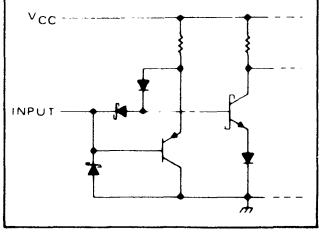
Active level(s) at the chip-select input(s) enables all of the outputs. An inactive level at any chip-select input causes all outputs to be off.

The three-state output offers the convenience of an open-collector output with the speed of a totem-pole output; it can be bus-connected to other similar outputs yet it retains the fast rise time characteristic of the TTL totem-pole output. The open-collector output offers the capability of direct interface with a data line having a passive pull-up.

schematics of inputs and outputs

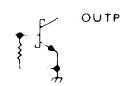
'S188, 'S287, 'S288, 'S387, 'S470, 'S471, 'S472, 'S473, 'S474, 'S475

EQUIVALENT OF EACH INPUT



'S188, 'S387, 'S470, 'S473, 'S475

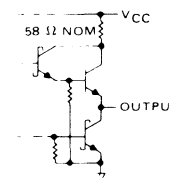
TYPICAL OF ALL OUTPUTS



Programming circuit not shown

'S287, 'S288, 'S471, 'S472, 'S474

TYPICAL OF ALL OUTPUTS



Programming circuit not shown

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54S' Circuits . . . . . −55°C to 125°C
SN74S' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended conditions for programming

		SN54S', SN74S'			UNIT
		MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	Steady state	4.75	5	5.75	V
	Program pulse	10	10.5	11†	
Input voltage	High level, V_{IH}	2.4		5	V
	Low level, V_{IL}	0		0.5	
Termination of all outputs except the one to be programmed		See load circuit (Figure 1)			
Voltage applied to output to be programmed, $V_{O(pr)}$ (see Note 2)		0	0.25	0.3	V
Duration of V_{CC} programming pulse Y (see Figure 2 and Note 3)		0.9	1	10	ms
Programming duty cycle			25	35	%
Free-air temperature		0		55	°C

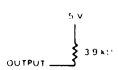
†Absolute maximum ratings.

NOTES: 1. Voltage values are with respect to network ground terminal. The supply-voltage rating does not apply during programming.
2. The 'S188, 'S288, 'S470, 'S471, 'S472, 'S473, 'S474, and 'S475 are supplied with all bit locations containing a low logic level, and programming a bit changes the output of the bit to high logic level. The 'S287 and 'S387 are supplied with all bit outputs at a high logic level, and programming a bit changes it to a low logic level.
3. Programming is guaranteed if the pulse applied is 0.9 ms long.

step-by-step programming procedure

1. Apply steady-state supply voltage (V_{CC} = 5 V) and address the word to be programmed.
2. Verify that the bit location needs to be programmed. If not, proceed to the next bit.
3. If the bit requires programming, disable the outputs by applying a high-logic-level voltage to the chip-select input(s).
4. Only one bit location is programmed at a time. Connect each output not being programmed to 5 V through 3.9 kΩ and apply the voltage specified in the table to the output to be programmed. Maximum current out of the programming output supply during programming is 150 mA.
5. Step V_{CC} to 10.5 V nominal. Maximum supply current required during programming is 750 mA.
6. Apply a low-logic-level voltage to the chip-select input(s). This should occur between 10 μs and 1 ms after V_{CC} has reached its 10.5-V level. See programming sequence of **Figure 2.**
7. After the X pulse time (1 ms) is reached, a high logic level is applied to the chip-select inputs to disable the outputs.
8. Within 10 μs to 1 ms after the chip-select input(s) reach a high logic level, V_{CC} should be stepped down to 5 V at which level verification can be accomplished.
9. The chip-select input(s) may be taken to a low logic level (to permit program verification) 10 μs or more after V_{CC} reaches its steady-state value of 5 V.
10. At a Y pulse duty cycle of 35% or less, repeat steps 1 through 8 for each output where it is desired to program a bit.

NOTE: Only one programming attempt per bit is recommended.



LOAD CIRCUIT FOR EACH OUTPUT NOT BEING PROGRAMMED OR FOR PROGRAM VERIFICATION
FIGURE 1

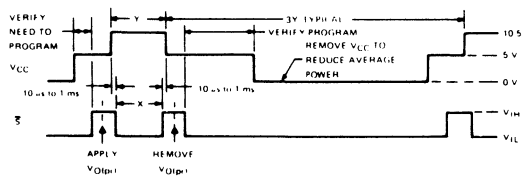


FIGURE 2–VOLTAGE WAVEFORMS FOR PROGRAMMING

recommended operating conditions

		'S287, 'S471			'S288			'S472, 'S474			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	Series 54S	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	Series 74S	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}	Series 54S			−2			−2			−2	mA
	Series 74S			−6.5			−6.5			−6.5	
Low-level output current, I_{OL}				16			20			12	mA
Operating free-air temperature, T_A	Series 54S	−55		125♦	−55		125	−55		125	°C
	Series 74S	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54S'			SN74S'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = MAX	2.4	3.4		2.4	3.2		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = MAX			0.5			0.5	V
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_O = 2.4 V	V_{IH} = 2 V,			50			50	μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_O = 0.5 V	V_{IH} = 2 V,			−50			−50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V			25			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.5 V			−250			−250	μA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−30		−100	−30		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, Chip select(s) at 0 V, Outputs open, See Note 4	'S287		100	135		100	135	mA
			'S288		80	110		80	110	
			'S471		110	155		110	155	
			'S472, 'S474		120	155		120	155	

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

TYPE	TEST CONDITIONS	$t_{a(ad)}$ (ns) Access time from address		$t_{a(\overline{S})}$ (ns) Access time from chip select (enable time)		t_{PXZ} (ns) Disable time from high or low le	
		TYP‡	MAX	TYP‡	MAX	TYP‡	MA
SN54S287	C_L = 30 pF for $t_{a(ad)}$ and $t_{a(\overline{S})}$ 5 pF for t_{PXZ}; R_L = 300 Ω; See Figure 4	42	75	15	40	12	40
SN74S287		42	65	15	35	12	35
SN54S288		25	50	12	30	8	30
SN74S288		25	40	12	25	8	20
SN54S471		50	80	20	40	15	35
SN74S471		50	70	20	35	15	30
SN54S472, SN54S474		55	85	20	45	15	40
SN74S472, SN74S474		55	75	20	40	15	35

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
♦An SN54S287 in the W package operating at free-air temperatures above 108°C requires a heat sink that provides a thermal resistance from case-to-free-air, $R_{\theta CA}$, of not more than 42°C/W.
NOTE 4: The typical values of I_{CC} shown are with all outputs low.

recommended operating conditions

		'S188			'S387, 'S470			'S473, 'S475			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	Series 54S	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	Series 74S	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output voltage, V_{OH}				5.5			5.5			5.5	V
Low-level output current, I_{OL}				20			16			12	mA
Operating free-air temperature, T_A	Series 54S	−55		125	−55		125♦	−55		125	C
	Series 74S	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

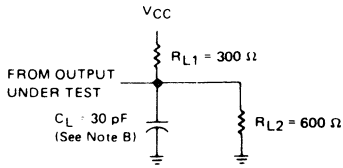
PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.2	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	V_{OH} = 2.4 V			50	μA
			V_{OH} = 5.5 V			100	
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = MAX			0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.5 V			−250	μA
I_{CC}	Supply current	V_{CC} = MAX, Chip select(s) at 0 V, Outputs open, See Note 4	'S188		80	110	mA
			'S387		100	135	
			'S470		110	155	
			'S473; 'S475		120	155	

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

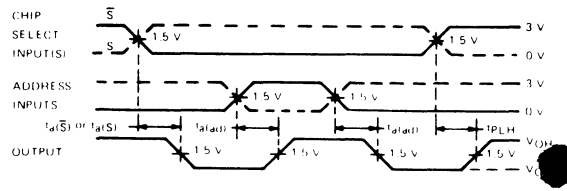
TYPE	TEST CONDITIONS	$t_{a(ad)}$ (ns) Access time from address		$t_{a(\overline{S})}$ (ns) Access time from chip select (enable time)		t_{PLH} (ns) Propagation delay time, low-to-high-level output from chip select (disable time)	
		TYP‡	MAX	TYP‡	MAX	TYP‡	MAX
SN54S188	C_L = 30 pF, R_{L1} = 300 Ω, R_{L2} = 600 Ω, See Figure 3	25	50	12	30	12	30
SN74S188		25	40	12	25	12	25
SN54S387		42	75	15	40	15	40
SN74S387		42	65	15	35	15	35
SN54S470		50	80	20	40	15	35
SN74S470		50	70	20	35	15	30
SN54S473, SN54S475		55	85	20	45	15	40
SN74S473, SN74S475		55	75	20	40	15	35

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
♦An SN54S387 in the W package operating at free-air temperatures above 108°C requires a heat sink that provides a thermal resistance from case-to-free-air, $R_{\theta CA}$, of not more than 42°C/W.
NOTE 4: The typical values of I_{CC} shown are with all outputs low.

PARAMETER MEASUREMENT INFORMATION



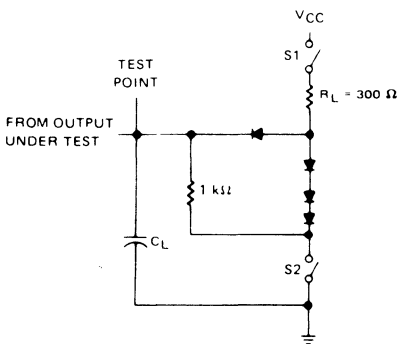
LOAD CIRCUIT



VOLTAGE WAVEFORMS

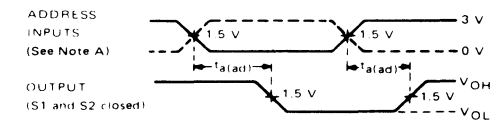
NOTES:
A. The input pulse generator has the following characteristics: $Z_{out} \approx 50\ \Omega$, PRR ≤ 1 MHz, $t_r \leq 2.5$ ns, and $t_f \leq 2.5$ ns.
B. C_L includes probe and jig capacitance.
C. The pulse generator is connected to the input under test. The other inputs, memory content permitting, are connected so that the input will switch the output under test.

FIGURE 3 – SWITCHING TIMES OF 'S188, 'S470, 'S387, 'S473, AND 'S475

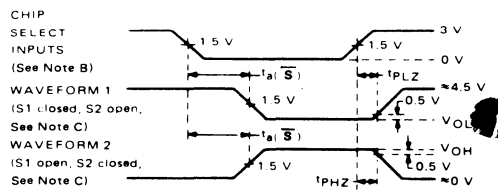


C_L includes probe and jig capacitance
All diodes are 1N3064

LOAD CIRCUIT



ACCESS TIME FROM ADDRESS INPUTS
VOLTAGE WAVEFORMS



$t_{PXZ} = t_{PHZ}$ or t_{PLZ}

ACCESS (ENABLE) TIME AND DISABLE TIME FROM CHIP SELECT
VOLTAGE WAVEFORMS

NOTES:
A. When measuring access times from address inputs, the chip-select input(s) is(are) low.
B. When measuring access and disable times from chip-select input(s), the address inputs are steady-state.
C. Waveform 1 is for the output with internal conditions such that the output is low except when disabled. Waveform 2 is for the output with internal conditions such that the output is high except when disabled.
D. Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns, PRR ≤ 1 MHz, and $Z_{out} \approx 50\ \Omega$.

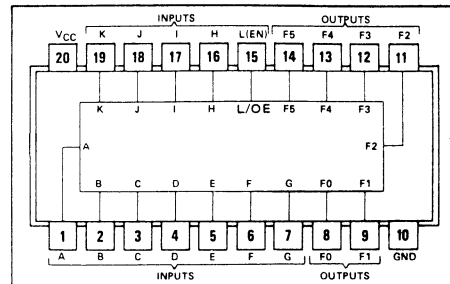
FIGURE 4 – SWITCHING TIMES OF 'S287, 'S288, 'S471, 'S472, AND 'S474

TYPES SN54S330, SN54S331, SN74S330, SN74S331
EXPANDABLE 12-INPUT, 50-TERM
FIELD-PROGRAMMABLE LOGIC ARRAYS

DECEMBER 1976

- Field-Programmable Logic Array Organized 12-Inputs/50-Product Terms/6-Outputs
- Programmable Options Include:
  - Active High or Low Inputs/Outputs
  - Choice of Dedicated Enable Input or Automatic Enable by True Product Terms
- Number of Inputs, Outputs, and Product Terms are Expandable
- High Density 20-Pin Package
- Full Schottky Clamping for High-Performance:
  - 35 ns Typical Data Delay Time
  - 20 ns Typical Enable Time
- Reliable TI-W Fuse Links for Fast, Low-Voltage Programming
- Choice of 3-State ('S330) or 2.5 kΩ Passive-Pullup ('S331) Outputs

SN54S330, SN54S331 . . . J PACKAGE
SN74S330, SN74S331 . . . J OR N PACKAGE



positive logic: See description and function tables.

description

These high-performance, Schottky-clamped 12-input, 6-output logic arrays can be field programmed to provide 50 product terms derived from the 12 inputs and sum the 50 products onto 6-output lines. They feature a programmable option which permits the FPLA outputs to be automatically enabled by a true product term or, to dedicate during programming, input (L/OE) to serve as an output enable (OE). Either option makes the FPLA expandable with respect to product terms.

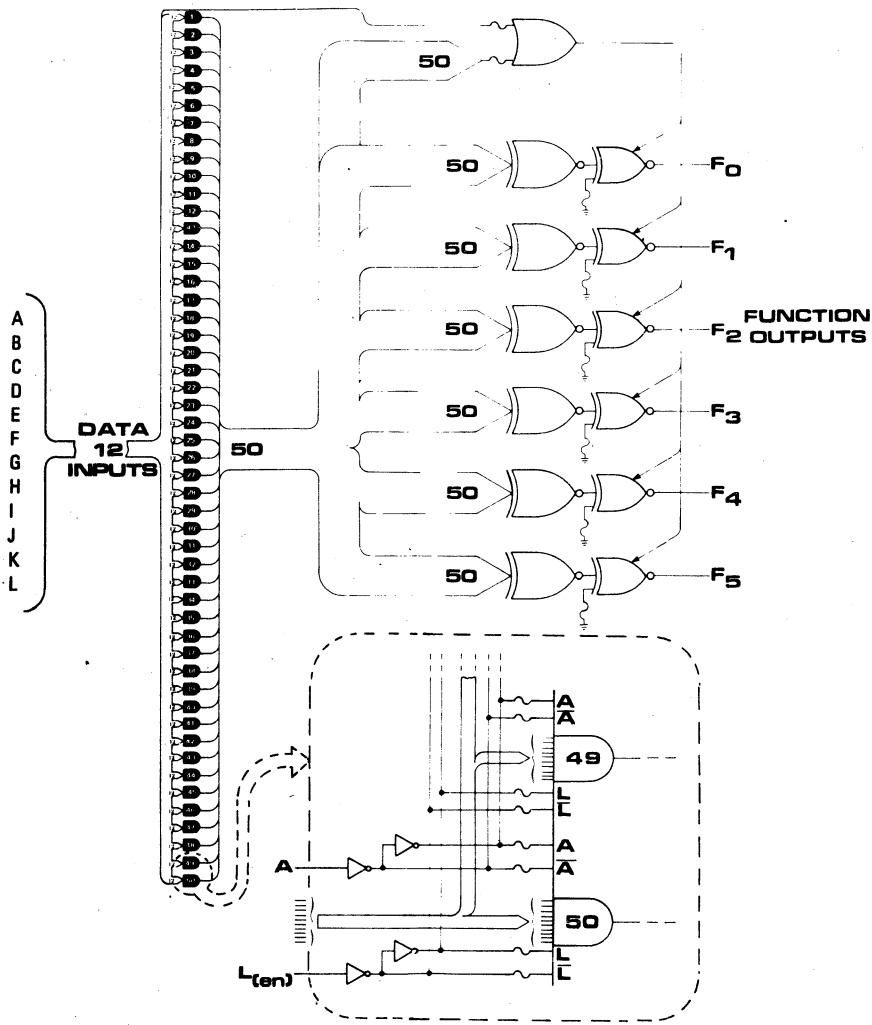
For every product term, 12 input variables can be programmed as high or low. Logic flexibility is further enhanced by the feature that the six outputs can be programmed individually to be active high or low.

The SN54S/74S330 is implemented with bus-driving 3-state outputs and can be connected directly to similar outputs in a bus-organized system. The SN54S/74S331 is implemented with a 2.5 kΩ passive pull-up resistor on each output meaning that:

a. The output can be combined with other similar or open-collector outputs to perform the logical wire-AND or a simple enable/disable function.

b. The series SN74S' outputs are also rated to source 250 μA of current at V_{OH} = 3.7 minimum for direct interface with MOS input thresholds.

The TI-W fuse links, used in the 'S330/'S331, feature the same low-voltage programming characteristics and proven reliability which Texas Instruments PROM's have demonstrated over a number of years.



WHERE:

$F_i = F_0, F_1, F_2, F_3, F_4,$ or F_5

$(ABC \ldots\ldots L)_i$ = 12 PROGRAMMABLE INPUTS (H = TRUE OR L = TRUE) FOR EACH OF 50 PRODUCT TERMS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54S330, SN54S331 . . . . . −55°C to 125°C
SN74S330, SN74S331 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54S330, SN54S331			SN74S330, SN74S331			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	'S330 (T-S)			−2			−6.5	mA
	'S331 (2.5 kΩ Pullup)			−0.2			−0.25	
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54S330, SN54S331			SN74S330, SN74S331			UNIT
					MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	High-level output voltage	'S330	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	I_{OH} = MAX	2.4	3.4		2.4	3.1		V
		'S331		I_{OH} = MAX	3.7	4.5		3.7	4.4		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 20 mA			0.5			0.5	V
I_{OZH}	Off-state output current, high-level voltage applied	'S330	V_{CC} = MAX	V_O = 2.4V			50			50	μA
I_{off}		'S331		V_O = 2.4V			50			50	
I_{OZL}	Off-state output current, low-level voltage applied	'S330	V_{CC} = MAX,	V_O = 0.5 V			−50			−50	μA
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V			50			50	μA
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.5 V			−0.25			−0.25	mA
I_{OS}	Short-circuit output current§	'S330	V_{CC} = MAX		−30		−100	−30		−100	mA
		'S331			−1.4		−4.4	−1.4		−4.4	
I_{CC}	Supply current	'S330	V_{CC} = MAX,	See Note 2		110			110		mA
		'S331				122			122		

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output of the 'S330 should be shorted at a time.
NOTE 2: I_{CC} is measured with all outputs open and all inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM	TO	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any input	Any output	C_L = 30 pF		35		ns
t_{PHL}					35		
t_{ZL}	Enable	Any output			15		ns
t_{ZH}					15		
t_{HZ}	Enable	Any output	C_L = 5 pF		15		ns
t_{LZ}					15		

programming the FPLA

The 'S330 and 'S331 are fabricated to include reliable low-voltage programmable Ti-W fuse links which have identical fusing characteristics with those used in TI's PROM's. The conditions recommended for programming the FPLA are virtually identical to those used for TI's PROM's; however, the AND-OR combinational logic performed by an FPLA requires that sequential programming be employed which establishes the AND term including the data/enable L/OE input before the OR term. Programming the automatic enable feature active, the true/false logic level of the outputs, and the data/enable input (L/OE) can be accomplished before or after the AND and OR matrices are established.

recommended conditions for programming

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC} (see Note 1)		4.75	5	5.75	V
Program pulse voltage, $V_{(pr)}$ (see Note 1)		10	10.5	11†	V
Program pulse rise time			100		ns
Input voltage (see Note 1)	High level, V_{IH}	2.4		5	V
	Low level, V_{IL}	0		0.5	
Voltage applied to output for OR programming, $V_{O(pr)}$ (see Figure D)		0	0.25	0.3	V
Duration of programming pulse Y (see Figures A, C, D, and Note 2)		0.9	1	20	ms
Programming duty cycle			25	35	%
Free-air temperature		0		55	°C

† Absolute maximum ratings.

NOTES: 1. Voltage values are with respect to the GND terminal.
2. Programming is guaranteed if the pulse applied is 0.9ms long. Typically, programming occurs in 1 ms.

programming the true/false logic level of the outputs

The FPLA is supplied with internal conditions established such that when a programmed AND or $\overline{\text{AND}}$ input term is true the associated function output (F_n) will be at a high logic level voltage, V_{OH}.

Programming the output to provide a low logic level voltage (V_{OL}) when the programmed input term is true can be accomplished by using AND/$\overline{\text{AND}}$ terms 50 through 55 shown in Table I and fusing the desired outputs using the step-by-step procedure.

TABLE I – ADDRESSES FOR PROGRAMMING OUTPUT LEVELS AND ENABLES

ADDRESS APPLIED TO OUTPUTS						PRODUCT TERM	PROGRAMS
F_5	F_4	F_3	F_2	F_1	F_0	ADDRESSED	
H	H	L	L	H	L	50	Output F_5 true low
H	H	L	L	H	H	51	Output F_4 true low
H	H	L	H	L	L	52	Output F_3 true low
H	H	L	H	L	H	53	Output F_2 true low
H	H	L	H	H	L	54	Output F_1 true low
H	H	L	H	H	H	55	Output F_0 true low
H	H	H	L	L	L	56	L/OE input into logical product term
H	H	H	L	L	H	57	Automatic output enable active

Programming can be verified before AND-OR programming by applying V_{CC} = 5 V and measuring $V_{OL} \leq 0.5$ V at the programmed output(s). After programming this test can be made by applying the input conditions which correspond to each term programmed to result in an active low-level output.

step-by-step programming procedure for outputs and enables

1. Apply steady-state supply voltage (V_{CC} = 5 V) and disable the outputs by applying 10.5 volts to the 12 data inputs. See Figure 1.
2. Verify that the fuse link needs to be programmed. If not, proceed to the next term.
3. Only one fuse link is programmed at a time. Address the term to be programmed by applying V_{IH} and V_{IL} to the outputs in accordance with Table I.
4. Step V_{CC} to 10.5 V nominal. Maximum supply current required during programming is 750 mA.
5. After the Y pulse time (1 ms) is reached, V_{CC} should be stepped down to 5V at which level verification can be accomplished.
6. The data inputs may be taken to logic levels (to permit program verification) 10 μs or more after V_{CC} reaches its steady-state value of 5 V.
7. At a Y pulse duty cycle of 35% or less, repeat steps 1 through 6 for each function to be programmed.

NOTES 3: V_{CC} should be removed between program-pulses to reduce dissipation and chip temperatures. See Figure 1.

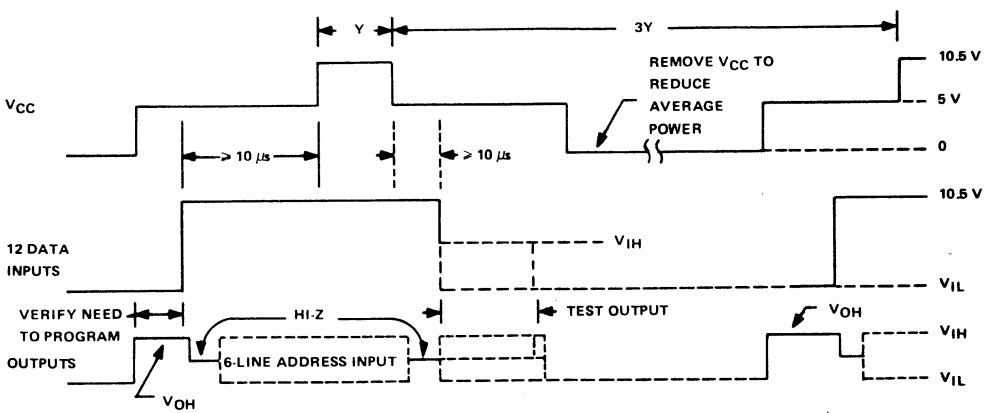


FIGURE 1 – OUTPUTS AND ENABLES PROGRAMMING SEQUENCE

programming the L(en) input

The L/OE input must be programmed either to function as a dedicated enable or to function as the 12th data input.

If it is to become the 12th data input a single fuse, at term 56_2 (see Table I), should be programmed in accordance with steps 1 through 4 above; then, input L is programmed logically into each AND/$\overline{\text{AND}}$ product term.

If input L/OE is to function as a dedicated output enable, term 56_2 is not fused: however, both AND/AND fuse links at each of the 50 product term addresses must be fused as outlined below creating a "don't care" for input L. This causes the input to become an overriding output enable/disable for the package.

programming the automatic disable to be inactive

The 'S330 and 'S331 are supplied with fuse links completing a circuit which automatically disables the six outputs (high-impedance (Z) for 'S330, high (H) for 'S331) for any product term which is purely "don't care"; i.e., not decoded by the AND matrix. Fusing one link inactivates the automatic output enabling circuit resulting in the six outputs being enabled for any input term, even "don't care".

The automatic disable fuse is programmed inactive by addressing term 57_2 (see Table I) and fusing in accordance with the step-by-step procedure above.

programming the AND/$\overline{\text{AND}}$ product terms

Each of the 50 product terms are capable of being programmed to decode a 12-wide term consisting of any combina of active (true) high, active (true) low, or don't care (H or L) input conditions at each of the 12 lines. This capabilit implemented by providing AND/NAND decode input gates each having a pair of associated fusible links which can be programmed to inactivate the unused decode level. Both decode levels can be removed resulting in a "don't care" input. The equivalent logic diagram showing the fusible links is shown in Figure 2.

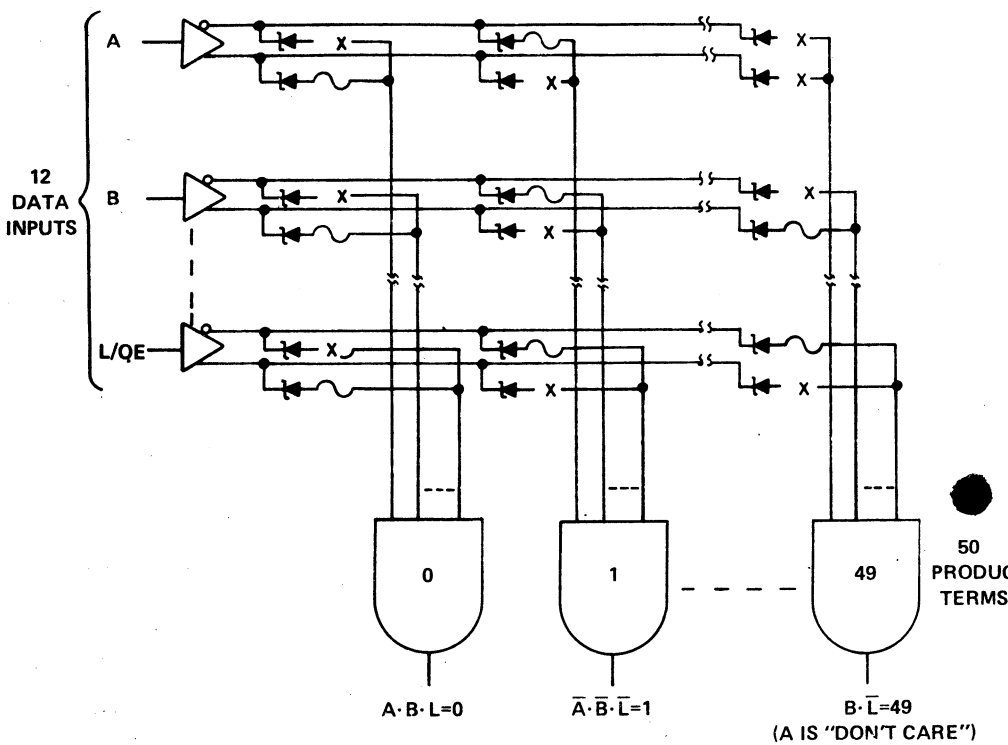


FIGURE 2 – EQUIVALENT LOGIC DIAGRAM OF FPLA PRODUCT TERMS

A particular pattern is assumed to have been programmed into the AND/$\overline{\text{AND}}$ fuse matrix with fused links opened at the locations marked with an "X". The resultant product terms are enumerated for the outputs of each product-term AND gate.

Product terms programmed into the AND/AND matrix will be used to select the term for programming the OR (summing) matrix. Redundant product terms will select two sum terms in the OR matrix, and overlapping product terms may select two or more sum terms. Reliable programming can be accomplished if redundant product terms are avoided and overlapping product terms are made unique for programming.

Redundant product terms are defined as being absolutely equal; i.e., $A\bar{B}CD\bar{E}FG \equiv A\bar{B}CD\bar{E}FG$. Use of apparently redundant terms is possible if the term does not use all inputs as the remaining inputs can be utilized to create unique terms for programming purposes by expansion:

Example:

$A\bar{B}CD\bar{E}FGH \equiv A\bar{B}CE\bar{D}FG\bar{H}$

After programming the OR matrix, the product terms can be readdressed and the H input can be programmed "don't care".

Overlapping terms are defined as two or more product terms in which the lesser product term can be addressed as a result of the application of a larger product term.

Examples:

$A\bar{B}CD\bar{E}FG$ ◄——— This large product term

$A\bar{B}$ $D\bar{E}$ G ◄
A CD F ◄ ——— also addresses these small terms

The small terms can be made unique for programming by simply expanding to non-redundant inputs.

$A\bar{B}CD\bar{E}FG$ ◄——— Large term

$A\bar{B}$ $D\bar{E}FG$ ◄
A CD $F\bar{G}$ ◄ ——— Small terms made unique by expanding (one fuse link each)

After programming the OR matrix, the product terms can be shortened by readdressing each and programming the added inputs to a "don't care". The AND/$\overline{\text{AND}}$ matrix is programmed one fuse at a time by addressing the term in accordance with Table II and fusing the input while applying the logic level desired to be active. See Figure 3.

TABLE II – ADDRESSES FOR PROGRAMMING PRODUCT TERMS

ADDRESS APPLIED TO OUTPUTS						PRODUCT TERM ADDRESSED
F_5	F_4	F_3	F_2	F_0	F_1	
L	L	L	L	L	L	0
L	L	L	L	L	H	1
L	L	L	L	H	L	2
L	L	L	L	H	H	3
						.
						.
						.
H	H	L	L	L	L	48
H	H	L	L	L	H	49

step-by-step programming procedure for AND matrix

1. Apply steady-state supply (V_{CC} = 5 V) and disable the outputs by applying 10.5 volts to the 12 data inputs. See Figure 3.
2. Verify that the fuse link needs to be programmed. If not, proceed to the next term.
3. Only one fuse link is programmed at a time. Address the term to be programmed by applying V_{IH} and V_{IL} to the outputs in accordance with Table II.
4. Apply the level to be true at the input to be programmed.
5. Step V_{CC} to 10.5 V nominal. Maximum supply current required during programming is 750 mA.
6. After the Y pulse time (1 ms) is reached, V_{CC} should be stepped down to 5 V at which level verification can be accomplished.
7. The data inputs may be taken to logic levels (to permit program verification) 10 μs or more after V_{CC} reaches its steady-state value of 5 V.
8. At a Y pulse duty cycle of 35% or less, repeat steps 1 through 7 for each input to be programmed.

NOTES: 4. V_{CC} should be removed between program-pulses to reduce dissipation and chip temperatures. See Figure 3.
5. If the input just programmed is to be a "don't care" and is not being used to expand the product term repeat steps 4 and 5 with the opposite logic level applied to the input. Before changing the product term address, program all inputs (A through L/OE for this product term including all "don't cares".
6. If input L/OE is to be used as a dedicated package enable it must be programmed as a "don't care" by fusing both links at each of the 50 product term locations.

The OR (summing) matrix for each product term can be programmed immediately upon completion of the 12-wide AND/$\overline{\text{AND}}$ term associated with it; or, the entire AND/$\overline{\text{AND}}$ term matrix can be programmed for all 50 product terms before programming the summing matrix.

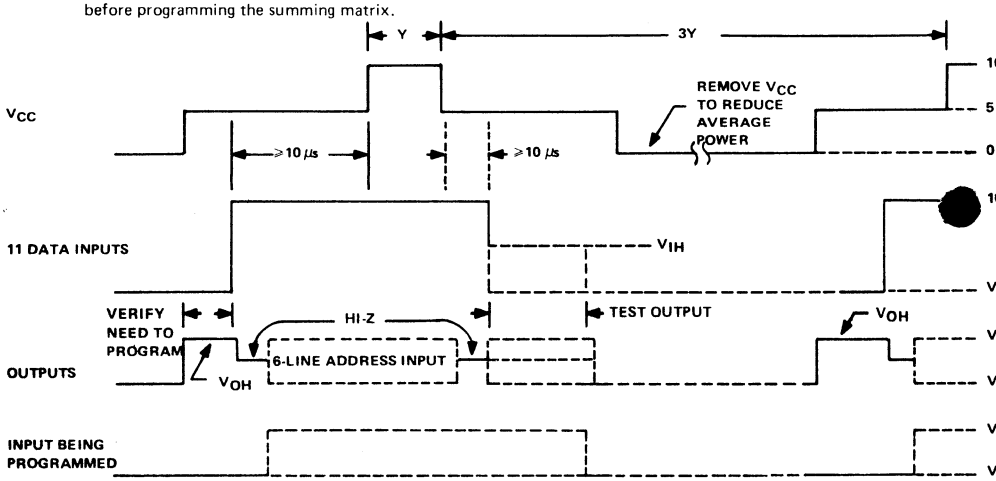


FIGURE 3 – AND MATRIX PRODUCT TERM PROGRAMMING SEQUENCE

programming the OR (summing) matrix

Product term(s) programmed into the AND/$\overline{\text{AND}}$ matrix can now be selected to provide a true logic level output. The true logic level output at F_0 through F_5 will be high if the output polarity fuses are intact, or F_0 through F_5 will be low if the output polarity fuses have been programmed, or a combination of highs and lows if some of the output polarity fuses have been programmed.

step-by-step programming procedure for OR matrix

Programming the OR matrix consists of fusing (one at a time) those outputs (F_0 through F_5) which are desired to be false in the addressed product term. The procedure is:

1. Apply steady-state supply voltage (V_{CC} = 5 V) and apply the unique product term. See Figure 4.
2. Verify that the fuse link needs to be programmed. If not, proceed to the next fuse link.
3. Only one fuse link is programmed at a time. Enable the term to be programmed by applying $V_{O(pr)}$ to the first output to be false in the product term.
4. Step V_{CC} to 10.5 V nominal. Maximum supply current required during programming is 750 mA.
5. After the Y pulse time (1 ms) is reached, V_{CC} should be stepped down to 5 V at which level verification can be accomplished.
6. Program verification can occur 10 μs or more after V_{CC} reaches its steady-state value of 5 V.
7. At a Y pulse duty cycle of 35% or less repeat steps 1 through 6 for each output to be programmed false for the active product term.

NOTES: 7. V_{CC} should be removed between program pulses to reduce dissipation and chip temperatures. See Figure 1.
8. If product terms were expanded to make them unique for programming purposes the product terms can be addressed and the added inputs can be removed by programming them to a "don't care" (fuse the remaining links).

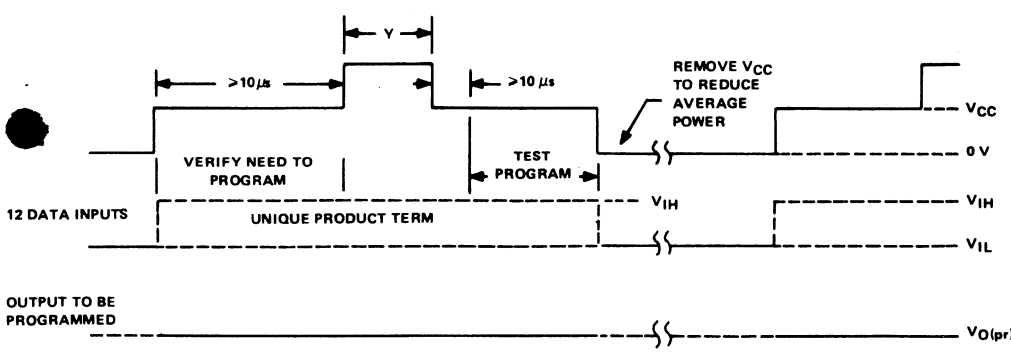
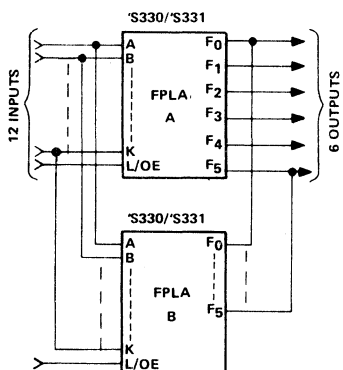


FIGURE 4 – OR TERM PROGRAMMING SEQUENCE

TYPES SN54S330, SN54S331, SN74S330, SN74S331
12-INPUT/6-OUTPUT EXPANDABLE FIELD-PROGRAMMABLE LOGIC ARRAYS

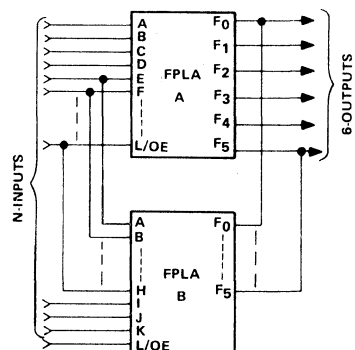
EXPAND
PRODUCT TERMS



OVERLAP INPUTS
AND OUTPUTS 1:1

- CODE OUTPUT ENABLES TO ENABLE FPLA "A" FOR SOME INPUT PATTERNS AND FPLA "B" FOR THE REST.

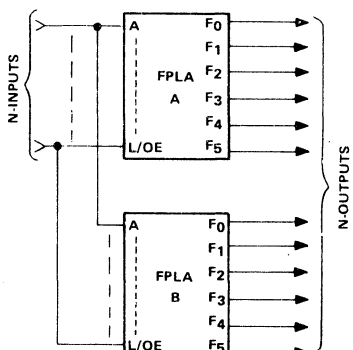
EXPAND
NUMBER OF INPUTS



OVERLAP INPUTS N:N
AND OUTPUTS 1:1

- OVERLAP INPUTS BY N-BITS
- CODE OUTPUT ENABLES TO ENABLE FPLA "A" OR "B" AS APPROPRIATE.

EXPAND
NUMBER OF OUTPUTS



OVERLAP INPUTS N:N

- USE OUTPUTS INDEPENDANTLY.
- CODE OUTPUTS ENABLED FOR BOTH FPLA "A" AND "B".

FIGURE 5 – EXPANDING THE 'S330, 'S331 FPLA

APPLICATIONS

The FPLA is efficiently suited for generating the sum of product terms which are normally required to implement:

- Memory mapping/supplemental functions
- Random logic or function generators
- Sequential controllers
- Status decoders or result interpreters
- Priority encoders

In addition, the FPLA introduces an alternative approach to the implementation of some code converters, pattern generators, and look-up tables which have commonly utilized PROMs and/or ROMs.

MEMORY CONTROL/SUPPLEMENTAL FUNCTIONS

The FPLA is ideally suited for implementing a wide variety of functions with respect to the control and/or supplementing of system memory capabilities. Some are:

- Memory mapping
- Microprogram control
- Memory patch
- PROM extension

The wide input capability of the 'S330/'S331 FPLA makes it ideal for decoding either a current memory address or a variety of status lines and generate a unique system control function.

MEMORY MAPPING/MICROPROGRAM CONTROL (See Figure 6)

These similar control functions utilize FPLAs which decode the assigned (mapped) addresses to accomplish system memory management; and/or, the FPLAs decode the current system address/status and implement the hardwired jump, branch-to-subroutine, or starting address in the microprogram control memory.

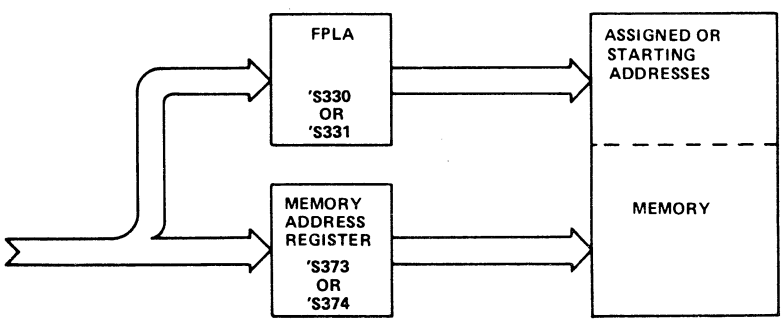


FIGURE 6 – MEMORY MAPPING/MICROPROGRAM CONTROL

MEMORY PATCH/PROM EXTENSION (See Figures 7 and 8)

These supplemental functions are cost-effective solutions for enhancing or upgrading existing memory systems or designs. Either the patch or extension can be used to correct existing deficiencies, to prioritize improved control over existing functions, or to extend the existing capabilities. Priority and source select can be programmed into the FPLA.

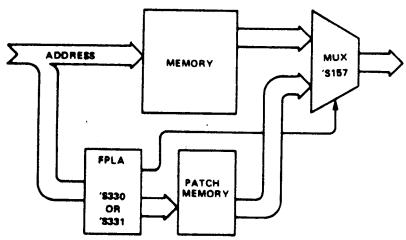


FIGURE 7 – MEMORY PATCH

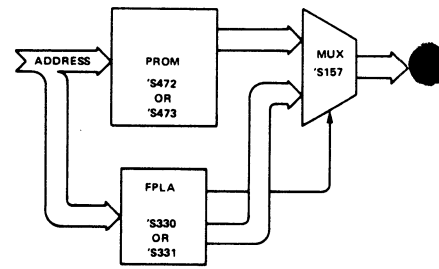


FIGURE 8 – PROM EXTENSION

DIGITAL SEQUENTIAL CONTROLLERS (See Figure 9)

This broad category of functions range from simple stand-alone machine controllers to the microprogram sequencing of any size computer or machine. The identifiable common denominator being that a sequential controller decodes a present state and generates the next state. Contrasted to a data processor or computer which generates information from operating on a word of data, the sequential controller generates information on a bit-by-bit basis.

Sequences generated can range from simple counting schemes to arbitrary bit-by-bit generation of any unique output states.

This application shows how the FPLA can simplify the implementation of a sequential controller. When the combinatorial logic of the FPLA is combined with the flexibility and synchronization of standard flip-flops in a feed-back loop, the full capability to generate a next state functional directive can be decoded from the present state the outputs of the flip flops (present state) in conjunction with the status inputs.

STATUS DECODERS/RESULT INTERPRETERS

This broad category of functions, generally described as the elements which monitor the execution results of present instructions in sequential machines, can provide the decision-making hardware needed to both determine that the present operation is complete and simultaneously generate the next starting address or state. The actual configuration varies widely, but one popular method is to configure the FPLA similar to that shown for memory mapping.

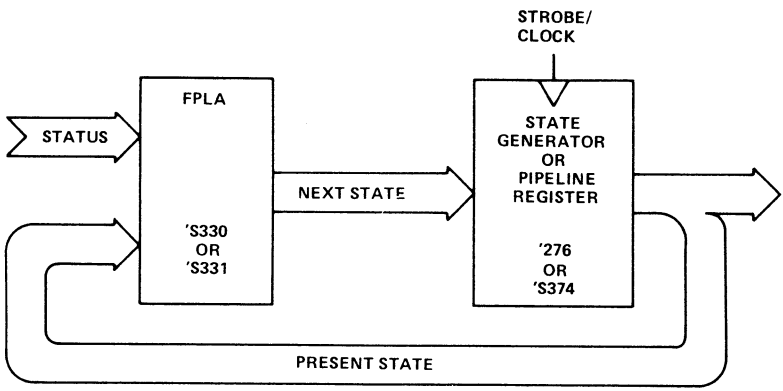


FIGURE 9 – SEQUENTIAL CONTROLLER

PRIORITY ENCODERS

The unique properties of the FPLA's capability to be programmed for decoding a number of product terms in virtaully any combination provides the user with the flexibility of identifying and implementing virtually any prioritized scheme. This option is normally available in any use shown for the 'S330/'S331.

RANDOM LOGIC OR FUNCTION GENERATORS

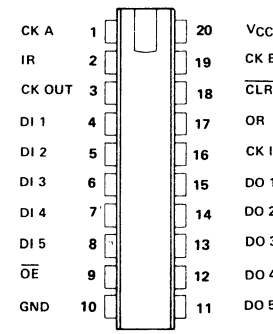
The 'S330/'S331 FPLAs provide the system designer with the options of reducing package count and/or system design time. Random gate logic can potentially be replaced at a package ratio of 12.5-to-1 up to 50-to-1 depending on the particular system needs. Function generators can be programmed directly into the FPLA from simple truth tables. In addition to reducing design and production start-up time, this technique can reduce the direct and indirect costs associated with logic and package minimization processes.

TYPE SN74S225
16 x 5 ASYNCHRONOUS FIRST-IN/FIRST-OUT MEMORY

SEPTEMBER 1976

- Independent Synchronous Inputs and Outputs
- Organized as 16-Words of 5 Bits
- DC to 10 MHz Data Rate
- 3-State Data Outputs
- 20-Pin, 300-mil, High Density Package

SN74S225 . . . J OR N PACKAGE
(TOP VIEW)



Pin assignments are same for all packages

description

This 80-bit active-element memory is a monolithic, Schottky-clamped transistor-transistor logic (STTL) array organized as 16 words of five-bits each. The 'S225 can easily be expanded to 16N-words of 5N-bits in length and features a single enable control for all 3-state data outputs.

operation

A FIFO is a memory storage device which allows data to be written into and/or read from its array at independent data rates. The 'S225 is a FIFO which will process data at any desired clock rate from DC to 10 MHz. The data is processed in a parallel format, word by word.

Reading or writing is done independently utilizing separate synchronous data clocks. Data may be written into the array on the low-to-high transition of either load clock input. Data may be read out of the array on the low-to-high transition of the unload clock input (normally high). When writing data into the FIFO one of the load clock inputs must be held high while the other strobes in the data. This arrangement allows either load clock to function as an inhibit for the other.

Status of the 'S225 is provided by three outputs. Input ready monitors the status of the last word location and signifies when the memory is full. This output is high whenever the memory is available to accept any data. The unload clock output also monitors the last word location. This output generates a low-logic-level pulse (synchronized to the inter clock pulse) when the location is vacant. The third status output, output ready, is high when the first word locat contains valid data and unload clock input is high. When unload clock input is low, output ready will be low. The first word location is defined as the location from which data is provided to the outputs.

The data outputs are noninverted with respect to the data inputs and are three-state with a common control input, output enable. When output enable is low, the data outputs are enabled to function as totem-pole outputs. A high-logic-level forces each data output to a high-impedance state while all other inputs and outputs remain active.

The clear input invalidates all data stored in the memory array by clearing the control logic and setting output ready to a low-logic-level on the high-to-low transition of a low-active pulse. The data outputs do not change as a result of the clear input; however, the output ready at a low-logic-level signifies invalid data.

FUNCTION TABLES

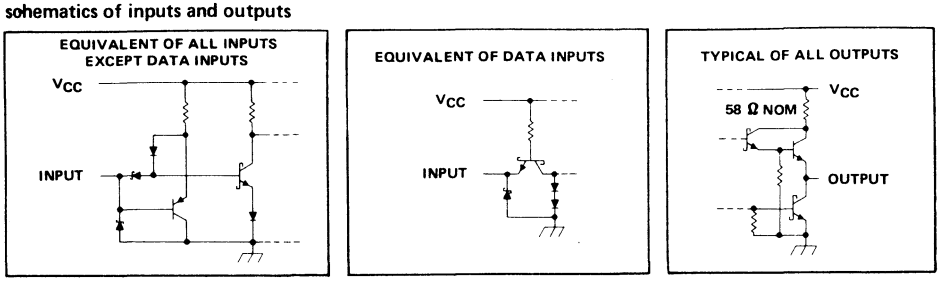
Table 1 – Input Functions

Input	Pin	Description
CK A	1	Load Clock A
DI 1 - DI 5	4-8	Data Inputs
$\overline{OE}$	9	Output Enable
CK IN	16	Unload Clock Input
$\overline{CLR}$	18	Clear
CK B	19	Load Clock B
GND	10	Ground pin
V_{CC}	20	Supply Voltage

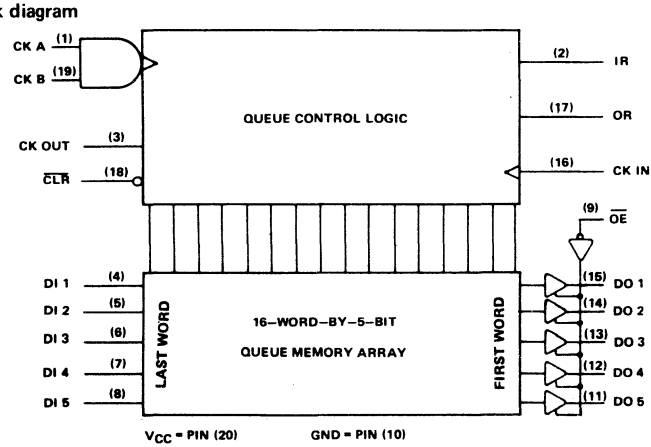
Table 2 – Output Functions

Output	Pin	Description
IR	2	Input Ready
CK OUT	3	Unload Clock Output
DO 5 - DO 1	11 - 15	Data Outputs
OR	17	Output Ready

schematics of inputs and outputs



functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltage, V_{CC} (see Note 1) 7V
Input Voltage 5.5V
Off-State Output Voltage 5.5V
Operating Free-Air Temperature Range . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

NOTE 1: All voltage values are with respect to network ground terminal.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply Voltage, V_{CC}		4.75	5	5.25	V
High-level output current, I_{OH}	All Outputs Except Data			−3.2	mA
	Data Outputs			−6.5	
Low-level output current, I_{OL}	All Outputs Except Data			8	mA
	Data Outputs			16	
Pulse Width	Load Clock A or B, t_w (high)	25			ns
	Unload Clock Input, t_w (low)	7			
	Clear, t_w (low)	40			
Setup Time	Data to Load Clock, t_{su} (DIi) See Note 2	−15†			ns
	Clear Release to Load Clock, t_{su}	25†			
Hold Time, Data from Load Clock, t_h(DIi)		70†			ns
Operating free-air temperature, T_A		0		70	°C

NOTE 2: Data must be setup within 15 ns after the load clock positive transition.

† ≡ The arrow indicates that the low-to-high transition of the load clock is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			-1.2	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = MAX	2.4	2.9		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = MAX		0.35	0.50	V
I_{OZH}	Off-state output current, high-level voltage applied		V_{CC} = MAX, V_{IL} = 0.8 V,	V_{IH} = 2 V, V_O = 2.4 V			50	μA
I_{OZL}	Off-state output current, low-level voltage applied		V_{CC} = MAX, V_{IL} = 0.8 V,	V_{IH} = 2 V, V_O = 0.5 V			-50	μA
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	Data In	V_{CC} = MAX,	V_I = 2.7 V			40	μA
		All Inputs Except Data In					25	
I_{IL}	Low-level input current	Data In	V_{CC} = MAX,	V_I = 0.5 V			−1	mA
		All Inputs Except Data In					-250	μA
I_{OS}	Short-circuit output current§		V_{CC} = MAX		-30		-100	mA
I_{CC}	Supply Current		V_{CC} = MAX,	See Note 3		80	120	mA

† For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Duration of the short circuit should not exceed one second.
NOTE 3: I_{CC} is measured with all inputs grounded and the output open.

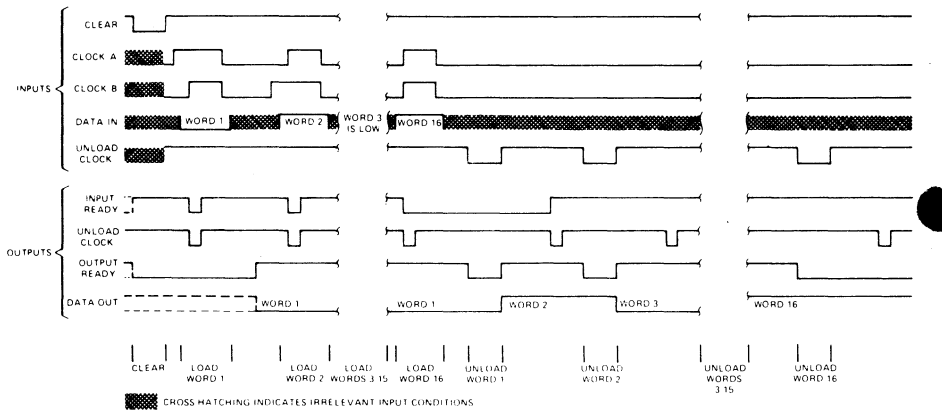
switching characteristics over recommended operating ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETERS¶	FROM	TO	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
f_{max}	CK A		C_L = 30 pF, R_L = 300 Ω, See Note 4	10	20		MHz
f_{max}	CK B			10	20		MHz
f_{max}	CK IN			10	20		MHz
t_w	CK OUT			7	14		ns
t_{PLZ}	$\overline{OE}$	DOi	C_L = 5 pF, R_{L1} = 300 Ω, See Note 4			40	ns
t_{PHZ}						40	
t_{PLH}	CK IN	DOi			50	75	ns
t_{PHL}					50	75	
t_{PLH}	CK A or CK B	OR			215	325	ns
t_{PLH}	CK IN	OR			40	60	ns
t_{PHL}					30	45	
t_{PHL}	$\overline{CLR}$	OR			40	60	ns
t_{PHL}	CK A or CK B	CK OUT	C_L = 30 pF, R_L = 300 Ω, See Note 4		35	50	ns
t_{PHL}	CK IN	CK OUT			300	450	ns
t_{PHL}	CK A or CK B	IR			42	65	ns
t_{PLH}	CK IN	IR			290	450	ns
t_{PLH}	$\overline{CLR}$	IR			20	35	ns
t_{PHL}							
t_{PLH}	OR↑	DOi			5	15	ns
t_{PHL}	OR↓				5	15	

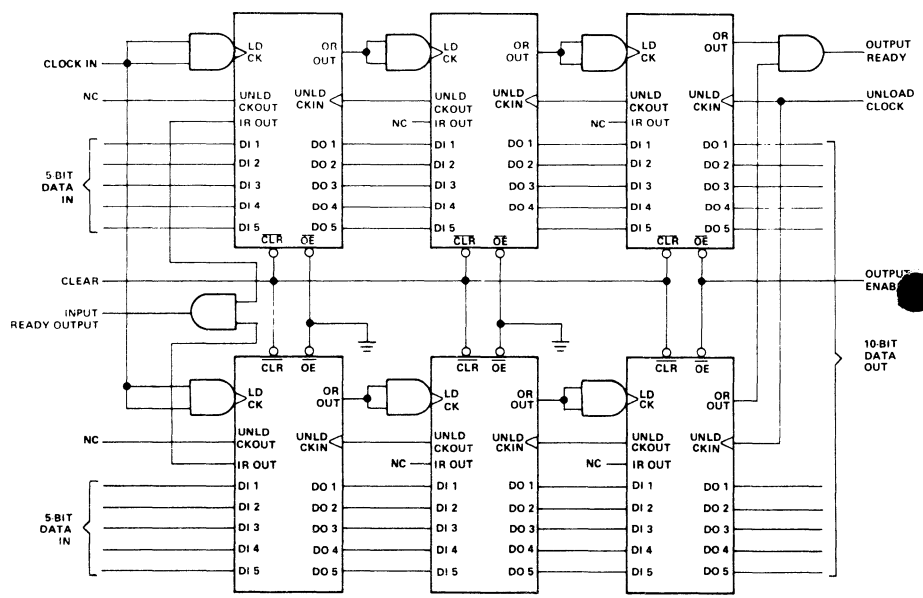
¶ f_{max} ≡ maximum clock frequency.
t_w ≡ pulse width (output)
↑↓ ≡ The arrow indicates that the low-to-high (↑) or high-to-low (↓) transition of the output ready (OR) output is used for reference.
t_{PLH} ≡ propagation delay time, low-to-high level output.
t_{PHL} ≡ propagation delay time, high-to-low-level output.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 4: Load circuit and voltage waveforms are shown in Appendix A.

TYPICAL WAVEFORMS



EXPANDING THE S225 FIFO
(48 WORDS OF 10 BITS SHOWN)

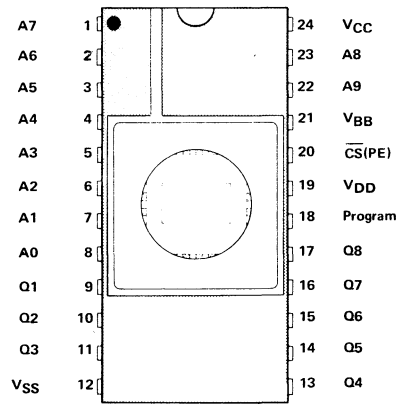


TMS 2708 JL and TMS 27L08 JL
1024-WORD BY 8-BIT ERASABLE PROGRAMMABLE READ-ONLY MEMORIES

JULY 1977

- 1024 x 8 Organization
- All Inputs and Outputs Fully TTL-Compatible
- Static Operation (No Clocks, No Refresh)
- Maximum Access Time . . . 450 ns
- Minimum Cycle Time . . . 450 ns
- 3-State Outputs for OR-Ties
- N-Channel Silicon-Gate Technology
- 8-Bit Output for Use in Microprocessor Based Systems
- TMS 27L08 Features
  - Low Power . . . 245 mW (Typical)
  - 10% Power Supply Tolerance
  - Guaranteed d.c. Noise Immunity with Standard TTL Loads
  - Increased Output Drive Capability

24-PIN CERAMIC
DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

The TMS 2708 JL and TMS 27L08 JL are 8,192-bit ultra-violet light erasable, electrically programmable read-only memories organized as 1024 words of 8-bit length. The devices are fabricated using N-channel silicon-gate technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull-up resistors and each output can drive one Series 74 TTL circuit without external resistors. The TMS 27L08 also guarantees 250 mV d.c. noise immunity in the high state and 200 mV in the low state. It will also directly drive 1 Series 74, 74S, or 74LS TTL circuit. The data outputs for both circuits are three-state for OR-tieing multiple devices on a common bus. A pin-compatible mask programmed ROM, the TMS4700 is available for large volume requirements.

The TMS 2708 and TMS 27L08 are designed for high-density fixed-memory applications where fast turn arounds and/or program changes are required. These EPROMs are supplied in a 24-pin dual-in-line ceramic (JL suffix) package designed for insertion in mounting-hole rows on 600-mil centers. The devices are characterized for operation from 0°C to 70°C.

operation (read mode)

address (A0-A9)

The address-valid interval determines the device cycle time. The 10-bit positive-logic address is decoded on-chip to select one of 1024 words of 8-bit length in the memory array. A0 is the least-significant bit and A9 the most-significant bit of the word address.

chip select, program enable [$\overline{CS}$(PE)]

When the chip select is low (logic 0), all eight outputs are enabled and the eight-bit addressed word can be read. When the chip select is high (logic 1), all eight outputs are in a high-impedance state. When the chip select, program enable is brought to V_{DD}, the outputs become inputs and the EPROM is ready for programming.

data out (Q1-Q8)

The chip must be selected before the eight-bit output word can be read. Data will remain valid until the address is changed or the chip is deselected. When deselected, the three-state outputs are in a high-impedance state. The outputs will drive TTL circuits without external components. The program pin must be held below V_{CC} in the read mode.

operation (program mode)

erase

Before programming, the TMS 2708 or TMS 27L08 is erased by exposing the chip through the transparent lid to high-intensity ultraviolet light (wavelength 2537 angstroms). The recommended exposure is ten watt-seconds per square centimeter. This can be obtained by, for instance, 20 to 30 minutes exposure of a filterless Model S52 short wave UV lamp about 2.5 centimeters above the EPROM. After erasure all bits are in the "1" state.

programming

Programming consists of successively depositing a small amount of charge to a selected memory cell that is to be changed from the erased "1" state to the "0" state. A "0" can be changed to a "1" only by erasure. Programming is normally accomplished on a PROM or EPROM Programmer, an example of which is TI's Universal PROM Programming Module in conjunction with the 990 prototyping system.

to start programming

First bring the $\overline{CS}$(PE) pin to +12 V to disable the outputs and convert them to inputs. This Program Enable pin is held high for the duration of the programming sequence. The first word to be programmed is addressed (it is customary to begin with the "0" address) and the data to be stored is placed on the Q1-Q8 program inputs. Then a +26 V program pulse is applied to the Program Pin. After 0.1 to 1.0 milliseconds the program pin is brought back to 0 V. After at least one microsecond the word address is sequentially changed to the next location, the new data is set up and the program pulse is applied.

Programming continues in this manner until all 1024 words have been programmed. This constitutes one of N program loops. The entire sequence is then repeated N times with N x $t_{W(PR)} \geqslant 100$ ms. Thus, if $t_{W(PR)}$ = 1 ms; then, N = 100, the minimum number of program loops required to program the EPROM.

to stop programming

After cycling through the N program loops, the last program pulse is brought to 0 V, then Program Enable [$\overline{CS}$(PE)] is brought to V_{IL} which takes the device out of the program mode. The data supplied by the programmer must be removed before the address is changed since the program inputs are now data outputs and a change of address could cause a voltage conflict on the output buffer. Q1-Q8 outputs are invalid up to 10 microseconds after the program enable pin is brought from $V_{IH(PE)}$ to V_{IL}.

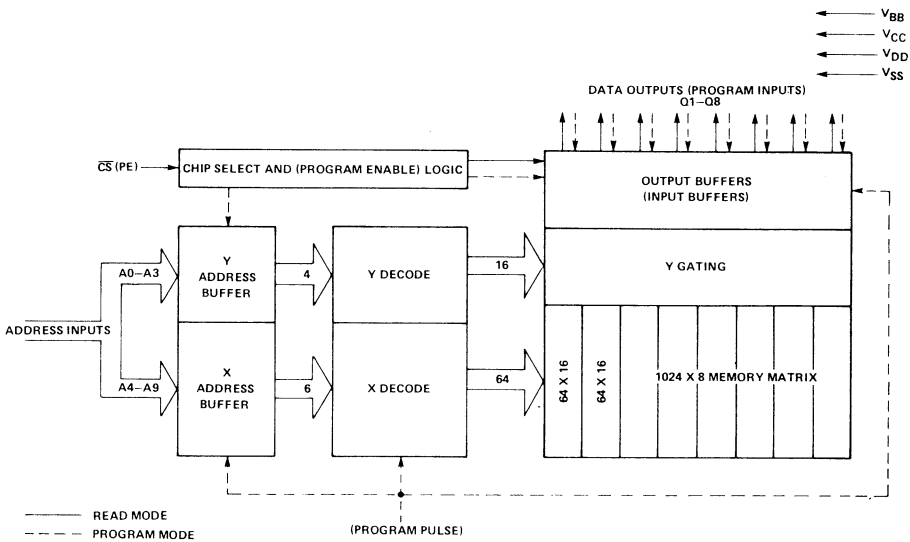
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{CC} (see Note 1)	−0.3 to 15 V
Supply voltage, V_{DD} (see Note 1)	−0.3 to 20 V
Supply voltage, V_{SS} (see Note 1)	−0.3 to 15 V
All input voltages (except program) (see Note 1)	−0.3 to 20 V
Program Input	−0.3 to 35 V
Output voltage (operating, with respect to V_{SS})	−2 to 7 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−55°C to 125°C

NOTE 1: Under absolute maximum ratings, voltage values are with respect to the most-negative supply voltage, V_{BB} (substrate), unless otherwise noted. Throughout the remainder of this data sheet, voltage values are with respect to V_{SS}.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

functional block diagram



recommended operating conditions

PARAMETER	TMS 2708			TMS 27L08			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{BB}	−4.75	−5	−5.25	−4.5	−5	−5.5	V
Supply voltage, V_{CC}	4.75	5	5.25	4.5	5	5.5	V
Supply voltage, V_{DD}	11.4	12	12.6	10.8	12	13.2	V
Supply voltage, V_{SS}		0			0		V
High-level input voltage, V_{IH} (except program and program enable)	2.4		V_{CC}+1	2.2		V_{CC}+1	V
High-level program enable input voltage, $V_{IH(PE)}$	11.4	12	12.6	10.8	12	13.2	V
High-level program input voltage, $V_{IH(PR)}$	25	26	27	25	26	27	V
Low-level input voltage, V_{IL} (except program)	V_{SS}		0.65	V_{SS}		0.65	V
Low-level program input voltage, $V_{IL(PR)}$ Note: $V_{IL(PR)}$ max + $V_{IH(PR)}$ = 25 V	V_{SS}		1	V_{SS}		1	V
Operating free-air temperature, T_A	0		70	0		70	°C
High-level program pulse input current, $I_{IH(PR)}$			40			40	mA

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TMS 2708			TMS 27L08			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −100 μA		3.7			3.7			V
		I_{OH} = −1 mA		2.4			2.4			
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA	TMS 2708			0.45			0.40	V
		I_{OL} = 2 mA	TMS 27L08							
I_I	Input current (leakage)	V_I = 0 V to 5.25 V			1	10		1	10	μA
I_O	Output current (leakage)	V_O = 5.25 V,	$\overline{CS}$(PE) = 5 V		1	10		1	10	μA
I_{BB}	Supply current from V_{BB}	All inputs high			30	45		8	14	mA
I_{CC}	Supply current from V_{CC}	$\overline{CS}$(PE) = 5 V			6	10		2	4	mA
I_{DD}	Supply current from V_{DD}	For I_{DD} MAX,	T_A = 0°C (worst case)		50	65		16	32	mA
P_D	Power dissipation	T_A = 70°C				800			350	mW
$P_{D(av)}$	Power dissipation	T_A = 25°C	65% Duty Cycle					245		mW
P_D	Power dissipation	T_A = 0°C (worst case)							475	mW

capacitance over recommended supply voltage range and operating free-air temperature range f = 1 MHz

PARAMETER		TYP†	MAX	UNIT
C_i	Input capacitance	4	6	pF
C_o	Output capacitance	8	12	pF

† All typical values are at T_A = 25°C and nominal voltages.

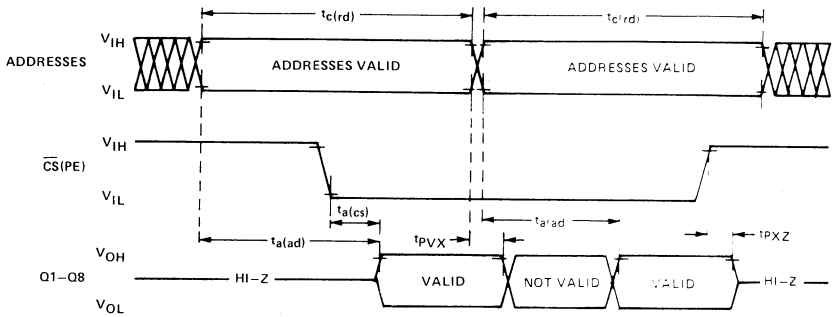
switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{a(ad)}$	Access time from address	C_L = 100 pf 1 Series 74 TTL Load $t_{f(CS)}$, $t_{f(ad)}$ = 20 ns		450	ns
$t_{a(CS)}$	Access time from $\overline{CS}$			120	ns
t_{PVX}	Output invalid from address change		0		ns
t_{PXZ}	Output disable time		0	120	ns

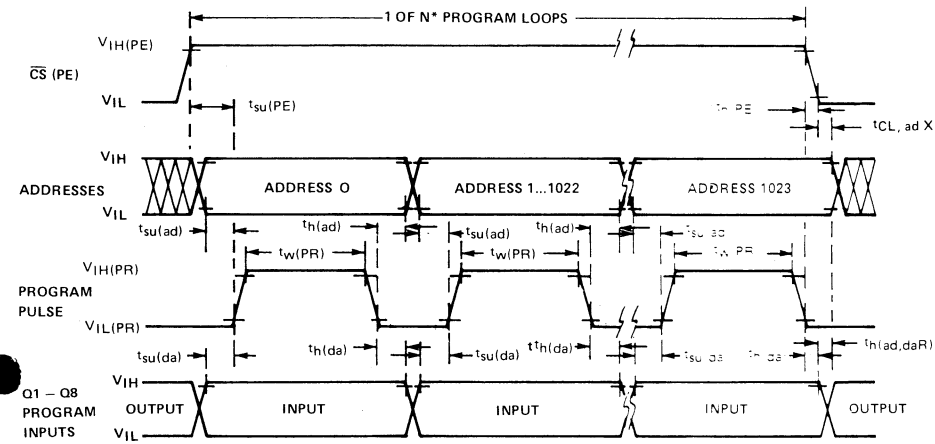
timing requirements over recommended supply voltage and operating free-air temperature range

PARAMETER		MIN	MAX	UNIT
$t_{c(rd)}$	Read cycle time	450		ns
$t_{w(PR)}$	Pulse width, program pulse	0.1	1	ms
t_T	Transition times (except program pulse)		20	ns
$t_{T(PR)}$	Transition times, program pulse	500	2000	ns
$t_{su(ad)}$	Address setup time	10		μs
$t_{su(da)}$	Data setup time	10		μs
$t_{su(PE)}$	Program enable setup time	10		μs
$t_{h(ad)}$	Address hold time	1000		ns
$t_{h(ad,da\ R)}$	Address hold time after program input data stopped	0		ns
$t_{h(da)}$	Data hold time	1000		ns
$t_{h(PE)}$	Program enable hold time	500		ns
$t_{CL,adX}$	Delay time, $\overline{CS}$(PE) low to address change	0		ns

read cycle timing



program cycle timing

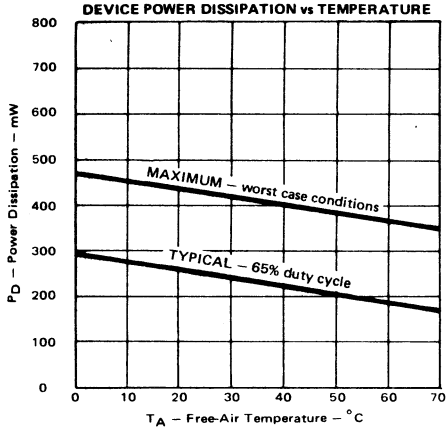


*$\overline{CS}$(PE) is at $V_{IH(PE)}$ through N program loops where N ≥100 ms/$t_{w(PR)}$

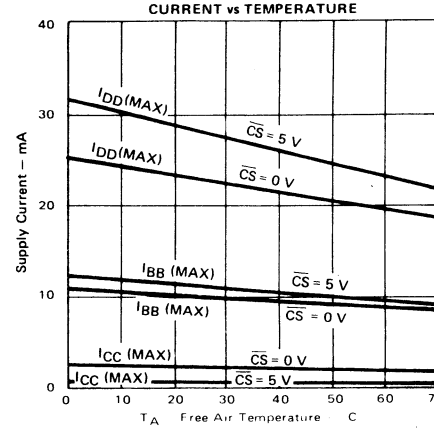
NOTE: Q1–Q8 outputs are invalid up to 10 μsec after programming ($\overline{CS}$(PE) goes low).

TYPICAL TMS 27L08 JL CHARACTERISTICS

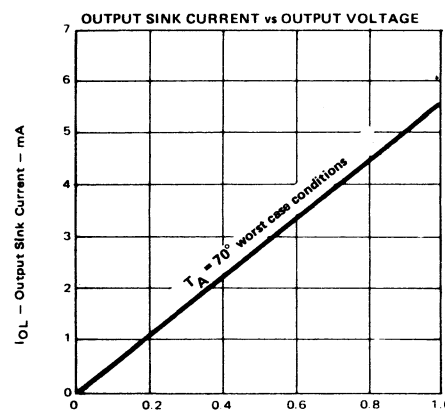
DEVICE POWER DISSIPATION vs TEMPERATURE



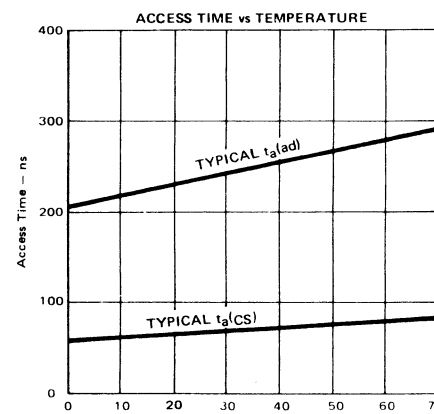
CURRENT vs TEMPERATURE



OUTPUT SINK CURRENT vs OUTPUT VOLTAGE



ACCESS TIME vs TEMPERATURE

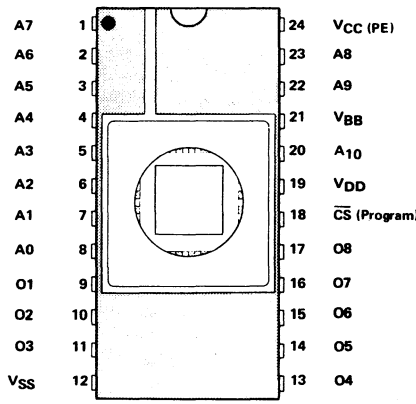


TMS 2716 JL
2048-WORD BY 8-BIT ERASABLE PROGRAMMABLE READ-ONLY MEMORIES

MARCH 1977

- 2048 x 8 Organization
- Plug in Compatible with the 2708 – Doubling Memory Size with Minimal Board Change
- All Inputs and Outputs Fully TTL-Compatible
- Static Operation (No Clocks, No Refresh)
- Maximum Access Time . . . 450 ns
- Minimum Cycle Time . . . 450 ns
- 3-State Outputs for OR-Ties
- 8-Bit Output for Use in Microprocessor Based Systems
- N-Channel Silicon-Gate Technology
- Low Power: 700 mW Maximum at 0°C, 550 mW Maximum at 70°C, 375 mW Typical
- Guaranteed d.c. Noise Immunity with Standard TTL Loads – No Pull-Up Resistors Required

24-PIN CERAMIC
DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

The TMS 2716 JL is a 16,384-bit ultra-violet light erasable, electrically programmable read-only memory organized as 2048 words of 8-bit length. The device is fabricated using N-channel silicon-gate technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull-up resistors and each output can drive one Series 74 TTL circuit without external resistors. In this configuration, the TMS 2716 also guarantees 250 mV noise immunity in the low state. The data outputs are three-state for OR-tieing multiple devices on a common bus. The TMS 2716 is plug-in compatible with the TMS 2708 and the TMS 27L08 8K EPROMs.

The TMS 2716 is designed for high-density fixed-memory applications where fast turn arounds and/or program changes are required. This EPROM is supplied in a 24-pin dual-in-line ceramic (JL suffix) package designed for insertion in mounting-hole rows on 600-mil centers. The device is designed for operation from 0°C to 70°C.

operation (read mode)

address (A0-A10)

The address-valid interval determines the device cycle time. The 11-bit positive-logic address is decoded on-chip to select one of 2048 words of 8-bit length in the memory array. A0 is the least-significant bit and A10 the most-significant bit of the word address.

chip select, Program [$\overline{CS}$(Program)]

When the chip select is low (logic 0), all eight outputs are enabled and the eight-bit addressed word can be read. When the chip select is high (logic 1), all eight outputs are in a high-impedance state. (In the program mode, the chip select feature does not function, as pin 18 inputs only the program pulse.)

data out (O1-O8)

The chip must be selected before the eight-bit output word can be read. Data will remain valid until the address is changed or the chip is deselected. When deselected, the three-state outputs are in a high-impedance state. The outputs will drive TTL circuits without external components.

operation (program mode)

erase

Before programming, the TMS 2716 is erased by exposing the chip through the transparent lid to high-intensity ultraviolet light (wavelength 2537 angstroms). The recommended exposure is ten watt-seconds per square centimeter. This can be obtained by, for instance, 20 to 30 minutes exposure of a filterless Model S52 short wave UV lamp about 2.5 centimeters above the EPROM. After erasure all bits are in the "1" state.

programming

Programming consists of successively depositing a small amount of charge to a selected memory cell that is to be changed from the erased "1" state to the "0" state. A "0" can be changed to a "1" only by erasure. Programming is normally accomplished on a PROM or EPROM Programmer.

to start programming

First bring the $V_{CC(PE)}$ pin to +12 V to disable the outputs and convert them to inputs. This Program Enable pin is held high for the duration of the programming sequence. The first word to be programmed is addressed (it is customary to begin with the "0" address) and the data to be stored is placed on the O1-O8 program inputs. Then a +26 V program pulse is applied to the Program Pin. After 0.1 to 1.0 milliseconds the program pin is brought back to 0 V. After at least one microsecond the word address is sequentially changed to the next location, the new data is set up and the program pulse is applied.

Programming continues in this manner until all 2048 words have been programmed. This constitutes one of N program loops. The entire sequence is then repeated N times with $N \times t_{W(PR)} \geqslant 100$ ms. Thus, if $t_{W(PR)} = 1$ ms; then, N = 100, the minimum number of program loops required to program the EPROM.

to stop programming

After cycling through the N program loops, the last program pulse is brought to 0 V, then Program Enable [$V_{CC(PE)}$] is brought to $V_{IL(PE)}$ which takes the device out of the program mode. The data supplied by the programmer must be removed before the address is changed since the program inputs are now data outputs and a change of address could cause a voltage conflict on the output buffer. O1-O8 outputs are invalid up to 10 microseconds after the program enable pin is brought from $V_{IH(PE)}$ to $V_{IL(PE)}$.

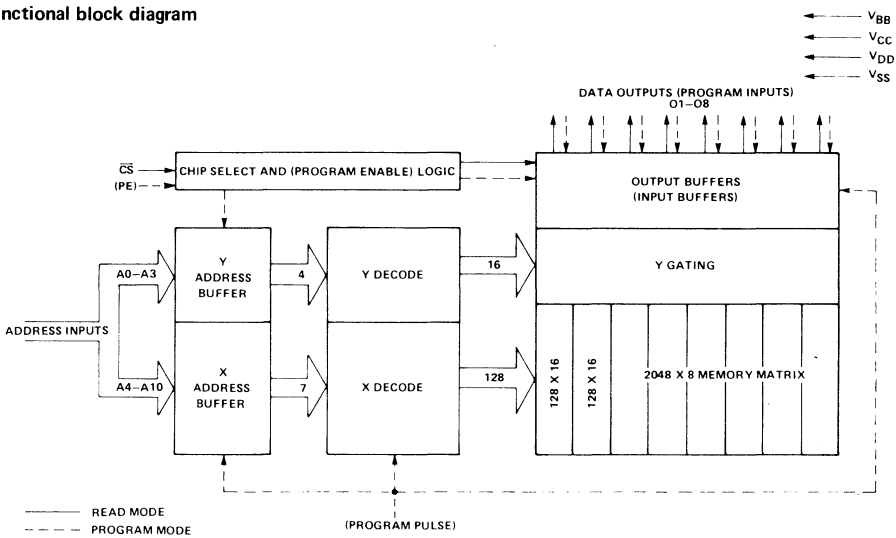
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{CC} (see Note 1)	−0.3 to 15 V
Supply voltage, V_{DD} (see Note 1)	−0.3 to 20 V
Supply voltage, V_{SS} (see Note 1)	−0.3 to 15 V
All input voltages (except program) (see Note 1)	−0.3 to 20 V
Program Input	−0.3 to 35 V
Output voltage (operating, with respect to V_{SS})	−2 to 7 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−55°C to 125°C

NOTE 1: Under absolute maximum ratings, voltage values are with respect to the most-negative supply voltage, V_{BB} (substrate), unless otherwise noted. Throughout the remainder of this data sheet, voltage values are with respect to V_{SS}.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

functional block diagram



recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{BB}	−4.75	−5	−5.25	V
Supply voltage, V_{CC}	4.75	5	5.25	V
Supply voltage, V_{DD}	11.4	12	12.6	V
Supply voltage, V_{SS}		0		V
High-level input voltage, V_{IH} (except program and program enable)	2.4		V_{CC}+1	V
High-level program enable input voltage, $V_{IH(PE)}$	11.4	12	12.6	V
High-level program input voltage, $V_{IH(PR)}$	25	26	27	V
Low-level input voltage, V_{IL} (except program and program enable)	V_{SS}		0.65	V
Low-level program input voltage (in the program mode) $V_{IL(PR)}$ Note: $V_{IL(PR)}$ max ≤ $V_{IH(PR)}$ − 25 V	V_{SS}		1	V
High-level program pulse input current, $I_{IH(PR)}$			40	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −100 μA	3.7			V
		I_{OH} = −1 mA	2.4			
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA			0.45	V
I_I	Input current (leakage)	V_I = 0 V to 5.25 V		1	10	μA
I_O	Output current (leakage)	V_O = 5.25 V, $\overline{CS}$ (Program) = 5 V		1	10	μA
I_{BB}	Supply current from V_{BB}	All inputs high		10	17	mA
I_{CC}	Supply current from V_{CC}	$\overline{CS}$ (Program) = 5 V		1	6	mA
I_{DD}	Supply current from V_{DD}	For I_{DD} MAX, T_A = 0°C (worst case)		26	45	mA
I_{PE}	Supply current from PE on V_{CC} pin	V_{PE} = V_{DD}		1	2	mA
P_D	Power Dissipation			375	700	mW
		70°C			550	

† All typical values are at T_A = 25°C and nominal voltage.

capacitance over recommended supply voltage range and operating free-air temperature range f = 1 MHz

PARAMETER		TYP†	MAX	UNIT
C_i	Input capacitance [except $\overline{CS}$ (Program)]	4	6	pF
$C_{i(CS)}$	$\overline{CS}$ (Program) input capacitance	20	30	pF
C_o	Output capacitance	8	12	pF

† All typical values are at T_A = 25°C and nominal voltages.

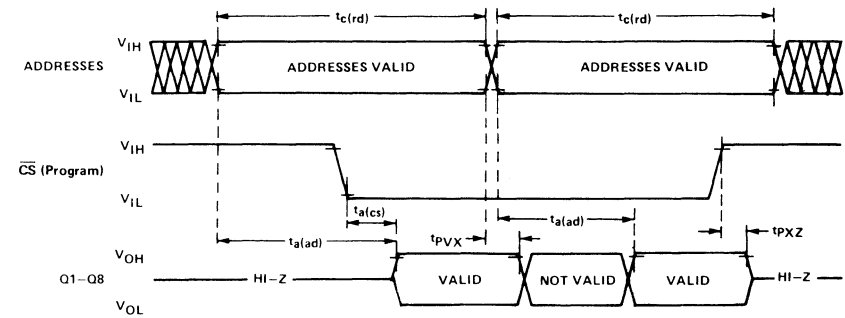
switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{a(ad)}$	Access time from address	C_L = 100 pF 1 Series 74 TTL Load $t_{f(CS)}$, $t_{f(ad)}$ = 20 ns		450	ns
$t_{a(CS)}$	Access time from $\overline{CS}$			120	ns
t_{PVX}	Output invalid from address change		0		ns
t_{PXZ}	Output disable time		0	120	ns

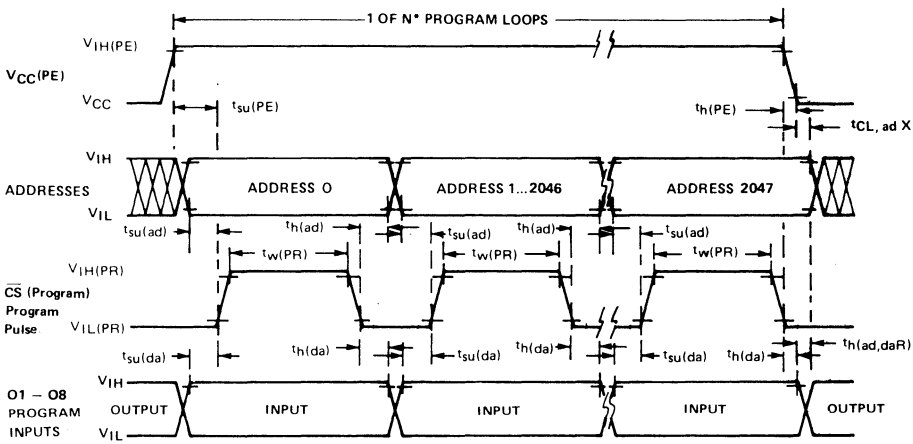
timing requirements over recommended supply voltage and operating free-air temperature range

PARAMETER		MIN	MAX	UNIT
$t_{c(rd)}$	Read cycle time	450		ns
$t_{w(PR)}$	Pulse width, program pulse	0.1	1	ms
t_T	Transition times (except program pulse)		20	ns
$t_{T(PR)}$	Transition times, program pulse	500	2000	ns
$t_{su(ad)}$	Address setup time	10		μs
$t_{su(da)}$	Data setup time	10		μs
$t_{su(PE)}$	Program enable setup time	10		μs
$t_{h(ad)}$	Address hold time	1000		ns
$t_{h(ad,da\ R)}$	Address hold time after program input data stopped	0		ns
$t_{h(da)}$	Data hold time	1000		ns
$t_{h(PE)}$	Program enable hold time	500		ns
$t_{CL,adX}$	Delay time, $\overline{CS}$(Program) low to address change	0		ns

read cycle timing



program cycle timing



* $V_{CC(PE)}$ is at $V_{IH(PE)}$ through N Program loops where $N \geq 100\ ms/t_{w(PR)}$

NOTE: O1–O8 outputs are invalid up to 10 μsec after programming ($V_{CC(PE)}$ goes low).

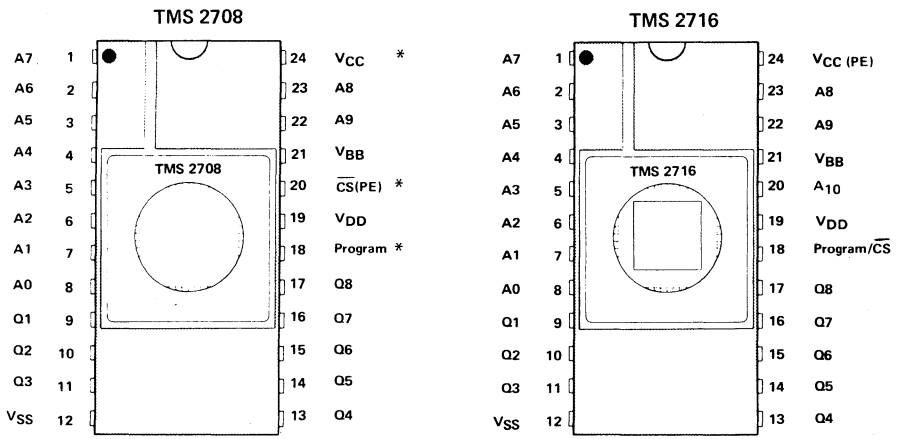
APPLICATIONS INFORMATION

Ease of Conversion From TMS 2708 To TMS 2716

A. The TMS 2716 and TMS 2708 have compatible timing, voltage and current parameters in both modes.

B. The 2716 requires less power than the 2708.

C. The pinouts are compatible. (See below.)



As can be seen from the above diagrams, only three pins* are modified in going from TMS 2708 to TMS 2716:

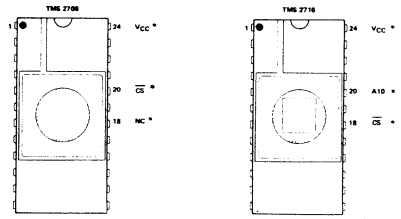
1. The additional address pin required for the 16K EPROM is located on pin 20 which displaces the $\overline{CS}$/PE functions on the 2708.

2. Since V_{CC} is not required during programming, the PE function shares pin 24 with V_{CC}.

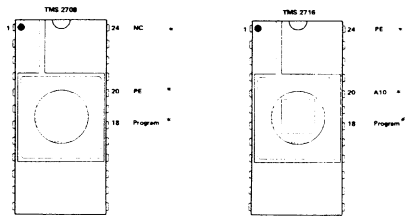
3. The $\overline{CS}$ function and program function are mutually exclusive during normal read mode (and are self-actuated complementary during the program/verify mode) and share pin 18.

The diagrams below show how these three pins are actually utilized in the read mode and in the program mode. Only pins 18, 20, and 24 need to be shown, as all other pin connections are identical.

Read Mode



Program (Write) Mode



TMS 2716 — Easy Programmability On Existing 2708 Programmers

All timing, voltage and current parameters are compatible so that existing 2708 programmers can easily and simply be converted to program the TMS 2716.

A simple cost-effective method to program the TMS 2716 on existing TMS 2708 programmers with no modification to the existing programmer is discussed in a separate application brief. All that is required is two switches and two sockets to allow each 8K half of the TMS 2716 to be programmed/verified separately.

Existing EPROM Programmers — Upgrading To the TMS 2716

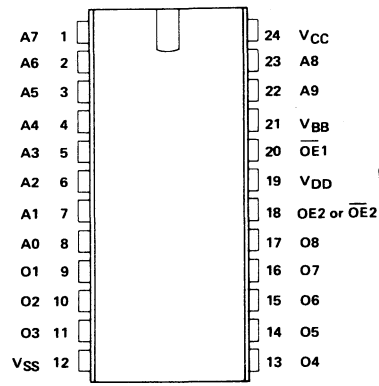
Most of the EPROM manufacturers are in the process of implementing field upgrade modifications to allow TMS 2716 programming on current EPROM programmers. This is greatly simplified because the TMS 2716 and the TMS 2708 are programmed in an identical manner. A slight modification to the socket card, an additional 1K x 8 of RAM, and an extra address signal (A10) are all that is required. All timing and voltage parameters are identical, so the upgrade is easily accomplished. Programmer manufacturers contacted to date on the TMS 2716 include: Data I/O, PRO LOG, Texas Instruments, Technico, CramerKit, Shepardson Micro Systems, Cromenco, MicroPro, and Ramtek.

TMS 4700 JL, NL
1024-WORD BY 8-BIT READ-ONLY MEMORY

BULLETIN NO. DL-S 7512273, MAY 1975

- 1024 x 8 Organization
- All Inputs and Outputs TTL-Compatible
- Maximum Access Time . . . 450 ns
- Minimum Cycle Time . . . 450 ns
- Typical Power Dissipation . . . 310 mW
- 3-State Outputs for OR-Ties
- Output Enable Control
- Silicon-Gate Technology
- 8-Bit Output for use in Microprocessor Based Systems

24-PIN CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGES
(TOP VIEW)



description

The TMS 4700 JL, NL is an 8,192-bit read-only memory organized as 1024 words of 8-bit length. The device is fabricated using N-channel silicon-gate technology for high speed and simple interface with bipolar circuits. All inputs can be driven by Series 74 TTL circuits with the use of external pull-up resistors and each output can drive one Series 74 TTL circuit without external resistors. The data outputs are three-state for OR-tieing multiple devices on a common bus. Two output-enable controls, one customer programmable, allow data to be read. The option on output enable 2 is explained in the section "Software Package".

The TMS 4700 is designed for high-density fixed-memory applications such as logic-function generation and microprogramming. This ROM is supplied in 24-pin dual-in-line ceramic (JL suffix) and plastic (NL suffix) packages designed for insertion in mounting-hole rows on 600-mil centers. The device is characterized for operation from 0°C to 70°C.

operation

address (A0-A9)

The address-valid interval determines the device cycle time. The 10-bit positive-logic address is decoded on-chip to select one of 1024 words of 8-bit length in the memory array. A0 is the least-significant bit and A9 the most-significant bit of the word address.

output enable ($\overline{OE}1$ and OE2†)

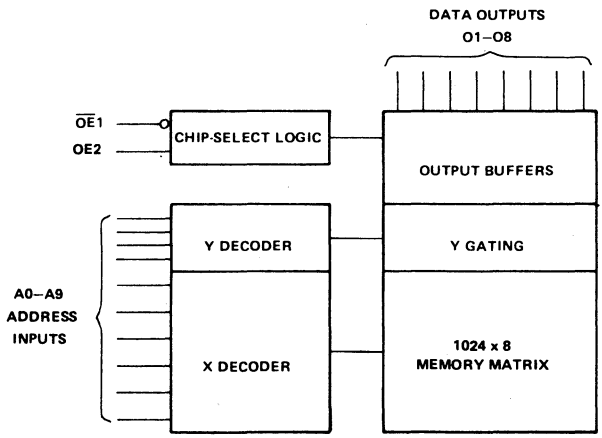
$\overline{OE}1$ is active when it is low. OE2 can be programmed, during mask fabrication, to be active with a high or a low level input. When both output enables are active, all eight outputs are enabled and the eight-bit addressed word can be read. When either output enable is not active, all eight outputs are in a high-impedance state.

data out (O1-O8)

The eight outputs must be enabled by both output enable controls before the output word can be read. Data will remain valid until the address is changed or the outputs are disabled. When disabled, the three-state outputs are in a high-impedance state. The outputs will drive TTL circuits without external components.

†Symbol OE2 assumes output enable 2 is programmed active high. If active low, the symbol would be $\overline{OE}2$.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{CC} (see Note 1) . . . . . –0.3 V to 20 V
Supply voltage, V_{DD} (see Note 1) . . . . . –0.3 V to 20 V
Supply voltage, V_{SS} (see Note 1) . . . . . –0.3 V to 20 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . –55°C to 125°C

NOTE 1: Under absolute maximum ratings, voltage values are with respect to the normally most positive supply, V_{BB} (substrate). Throughout the remainder of this data sheet voltage values are with respect to V_{SS}.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{BB}	–4.75	–5	–5.25	V
Supply voltage, V_{CC}	4.75	5	5.25	V
Supply voltage, V_{DD}	11.4	12	12.6	V
Supply voltage, V_{SS}		0		V
High-level input voltage, V_{IH}	3.3		V_{CC}	V
Low-level input voltage, V_{IL}	V_{SS}		0.8	V
Read cycle time, $t_{c(rd)}$	430			ns
Output-enable rise time, $t_{r(\overline{OE}1)}$ and $t_{r(OE2)}$		10	20	ns
Output-enable fall time, $t_{f(\overline{OE}1)}$ and $t_{f(OE2)}$		10	20	ns
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended supply voltage ranges, T_A = 0°C to 70°C (unless otherwise noted)

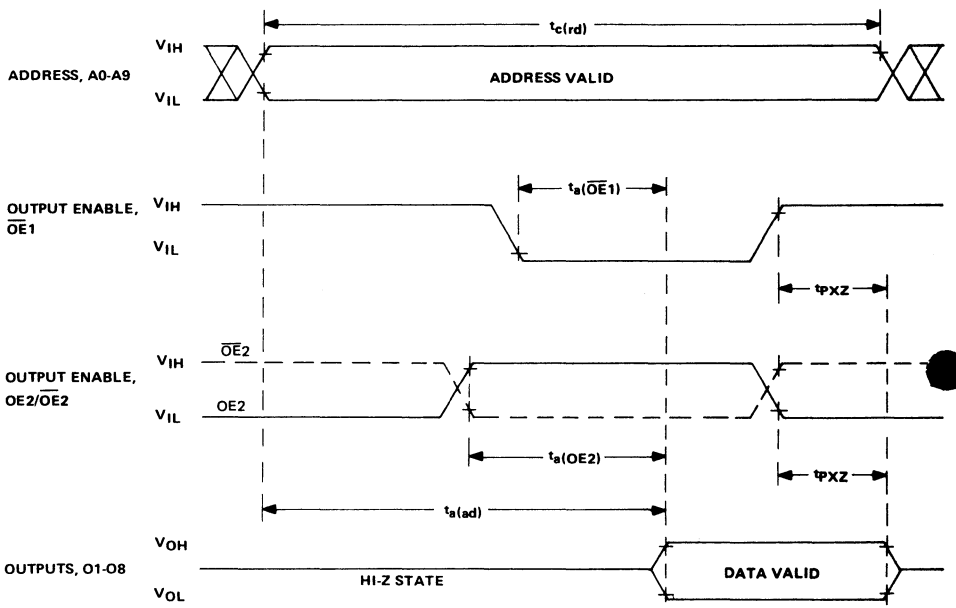
PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −1 mA	3.7			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.45	V
I_I	Input current	V_I = 0 to 6.5 V			±10	μA
I_{BB}	Supply current from V_{BB}	Both output enables active		−0.1		mA
I_{CC}	Supply current from V_{CC}			2		mA
I_{DD}	Supply current from V_{DD}			25		mA
P_D	Power dissipation			310		mW

† All typical values are at T_A = 25°C and nominal voltages.

switching characteristics over recommended supply voltage ranges, T_A = 0°C to 70°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{a(ad)}$	Access time from address	C_L = 50 pF, 1 Series 74 TTL load		430	ns
$t_{a(\overline{OE}1)}$	Access time from output enable 1			90	ns
$t_{a(OE2)}$	Access time from output enable 2			130	ns
t_{PXZ}	Output disable time from either chip enable			90	ns

voltage waveforms



NOTE: Timing points are 90% (high) and 10% (low).

SOFTWARE PACKAGE

The TMS 4700 JL, NL is a fixed-program memory in which the programming is performed by TI at the factory during the manufacturing cycle to the specific customer inputs supplied in the format shown. The device is organized as 1024 8-bit words with address locations numbered 0 to 1023. Any 8-bit word can be coded as a 2-digit hexadecimal number between 00 and FF. All stored words and addresses in the following format are coded in hexadecimal numbers. In coding, all binary words must be in positive logic before conversion to hexadecimal. O1 is considered the least-significant bit and O8 the most-significant bit. For addresses A0 is least significant and A9 is most significant.

Every card should include the TI Custom Device Number in the form ZAXXXX (4-digit number to be assigned by TI) in columns 75 through 80.

Output enable 2 is customer programmable. Every card should include in column 74 a 1 if the output is to be enabled with a high-level input at $\overline{OE2}$ or a 0 for enabling with a low-level input.

The 1024 coded words must be supplied on 64 cards with 16 2-digit hex numbers per card.

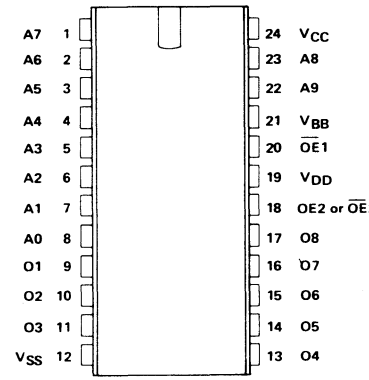
CARD	COLUMN	HEXADECIMAL INFORMATION
1	1–9	BLANK
	10	: (ASCII character colon)
	11–12	10 (specifies 16 words per card)
	13	BLANK
	14–16	Hex address of 1st word on 1st card (0th word, address normally 000)
	17–18	BLANK
	19–20	0th word in Hex
	•	
	•	
	•	
	49–50	15th word in Hex
	51–73	BLANK
64	1–9	BLANK
	10	: (ASCII character colon)
	11–12	10
	13	BLANK
	14–16	Hex address of 1st word on 64th card (1008th word, address normally 3F0)
	17–18	BLANK
	19–20	1008th word in Hex
	•	
	•	
	•	
	49–50	1023rd word in Hex
	51–73	BLANK

MOS
LSI

TMS 4710 JL,NL
COMPLETE ASCII CHARACTER SET GENERATOR
5x7 CHARACTER, 8x8 BLOCK

- TMS 4710 (Standard TMS 4700 8K ROM)
- Full Upper and Lower Case ASCII Character Generator
- Ideal for Video Terminal Applications
- Fully Static Operation
- Block Size 8 x 8
- Character Size 5 x 7
- 1024 x 8 Organization
- All Inputs and Outputs TTL-Compatible
- Maximum Access Time . . . 450 ns
- Minimum Cycle Time . . . 450 ns
- Typical Power Dissipation . . . 310 mW
- 3-State Outputs for OR-Ties
- Output Enable Control
- Silicon-Gate Technology
- 8-Bit Output for use in Microprocessor Based Systems

24-PIN CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGES
(TOP VIEW)



description

The TMS 4710 JL, NL is an 8,192-bit read-only memory organized as 1024 words of 8-bit length. The device is fabricated using N-channel silicon-gate technology for high speed and simple interface with bipolar circuits. All inputs can be driven by Series 74 TTL circuits with the use of external pull-up resistors and each output can drive one Series 74 TTL circuit without external resistors. The data outputs are three-state for OR-tieing multiple devices on a common bus. Two output-enable controls, when active low, allow data to be read, which simplifies overall system design.

The TMS 4710 is designed for ASCII graphics applications such as CRT and printers. This ROM is supplied in 24-pin dual-in-line ceramic (JL suffix) and plastic (NL suffix) packages designed for insertion in mounting-hold rows on 600-mil centers. The device is characterized for operation from 0°C to 70°C.

operation

address (A0-A9)

The address-valid interval determines the device cycle time. The 10-bit positive-logic address is decoded on-chip to select one of 1024 words of 8-bit length in the memory array. A0 is the least-significant bit and A9 the most-significant bit of the word address.

Address lines A0-A2 choose the row to be output. For row zero, all outputs are low (blank).

Address lines A3-A9 select the character to be displayed.

output enable ($\overline{OE}1$ and OE2†)

$\overline{OE}1$ is active when it is low. $\overline{OE}2$ is active when low, and when both output enables are active, all eight outputs are enabled and the eight-bit addressed word can be read. When either output enable is not active, all eight outputs are in a high-impedance state.

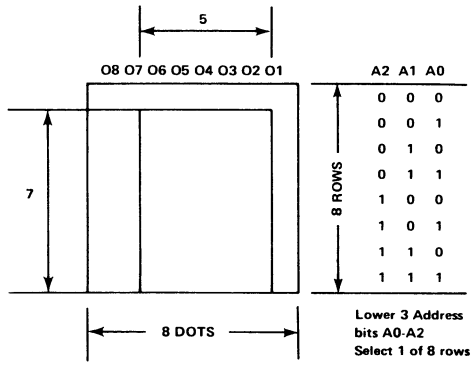
†Symbol OE2 assumes output enable 2 is programmed active high. If active low, the symbol would be $\overline{OE}2$.

data out (O1-O8)

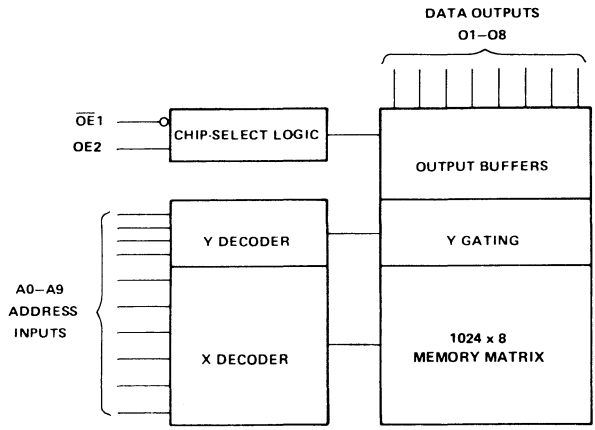
The eight outputs must be enabled by both output enable controls before the output word can be read. Data will remain valid until the address is changed or the outputs are disabled. When disabled, the three-state outputs are in a high-impedance state. The outputs will drive TTL circuits without external components.

Data out bits O1, O7, and O8 are always output as low (blank) display for alphanumeric characters. Data out bit O8 is always output as low (blank) display.

A simulated Video Display of the TMS 4710 Character Generator Output is shown in attached figure.



functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{CC} (see Note 1) . . . . . −0.3 V to 20 V
Supply voltage, V_{DD} (see Note 1) . . . . . −0.3 V to 20 V
Supply voltage, V_{SS} (see Note 1) . . . . . −0.3 V to 20 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 125°C

NOTE 1: Under absolute maximum ratings, voltage values are with respect to the normally most positive supply, V_{BB} (substrate). Throughout the remainder of this data sheet voltage values are with respect to V_{SS}.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{BB}	−4.75	−5	−5.25	V
Supply voltage, V_{CC}	4.75	5	5.25	V
Supply voltage, V_{DD}	11.4	12	12.6	V
Supply voltage, V_{SS}		0		V
High-level input voltage, V_{IH}	3.3		V_{CC}	V
Low-level input voltage, V_{IL}	V_{SS}		0.8	V
Read cycle time, $t_{c(rd)}$	450			ns
Output-enable rise time, $t_{r(\overline{OE}1)}$ and $t_{r(OE2)}$		10	20	ns
Output-enable fall time, $t_{f(\overline{OE}1)}$ and $t_{f(OE2)}$		10	20	ns
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended supply voltage ranges, T_A = 0°C to 70°C (unless otherwise noted)

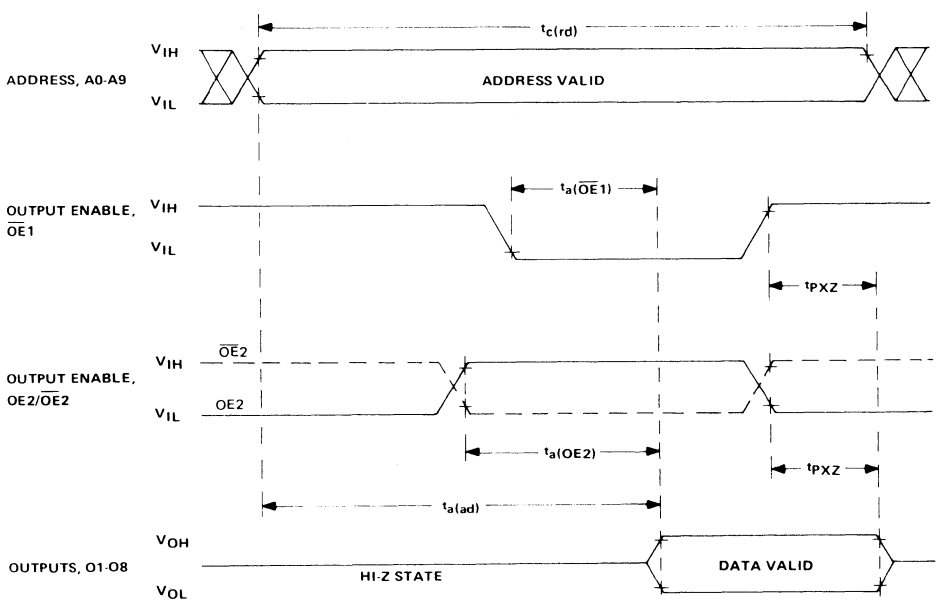
PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −1 mA	3.7			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.45	V
I_I	Input current	V_I = 0 to 6.5 V			±10	μA
I_{BB}	Supply current from V_{BB}	Both output enables active		−0.1		mA
I_{CC}	Supply current from V_{CC}			2		mA
I_{DD}	Supply current from V_{DD}			25		mA
P_D	Power dissipation			310		mW

†All typical values are at T_A = 25°C and nominal voltages.

switching characteristics over recommended supply voltage ranges, T_A = 0°C to 70°C

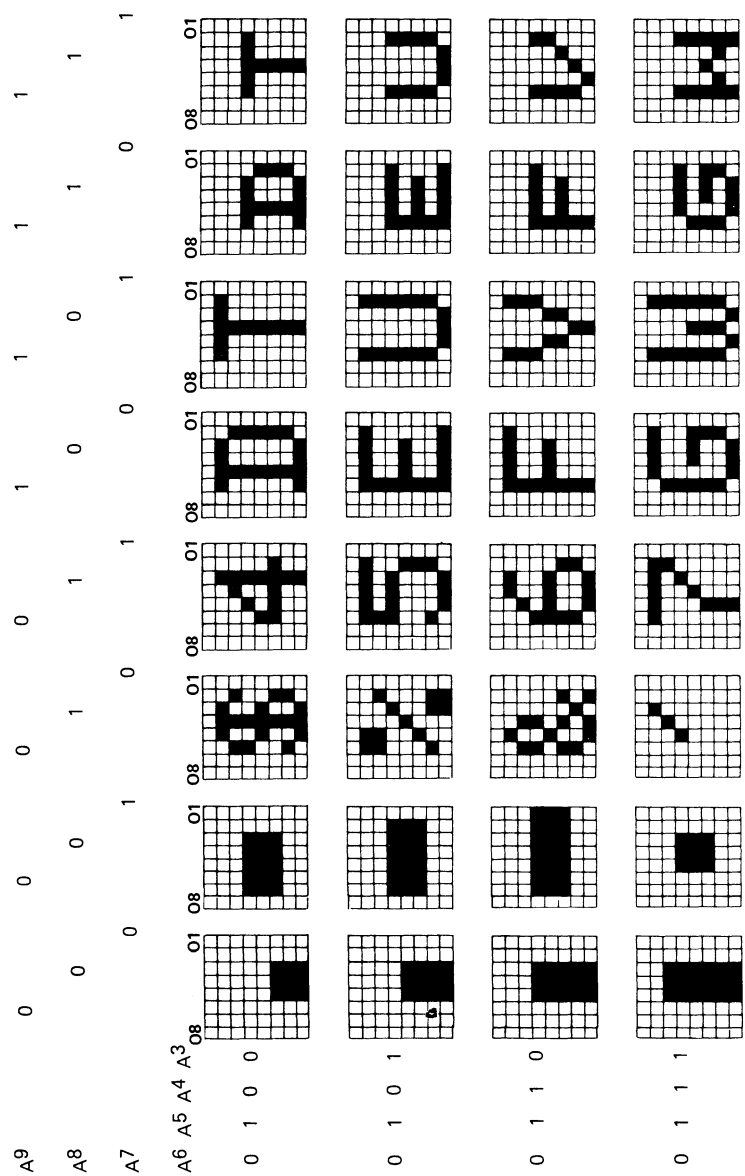
PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{a(ad)}$	Access time from address	C_L = 50 pF, 1 Series 74 TTL load		450	ns
$t_{a(\overline{OE}1)}$	Access time from output enable 1			90	ns
$t_{a(OE2)}$	Access time from output enable 2			130	ns
t_{PXZ}	Output disable time from either chip enable			90	ns

voltage waveforms



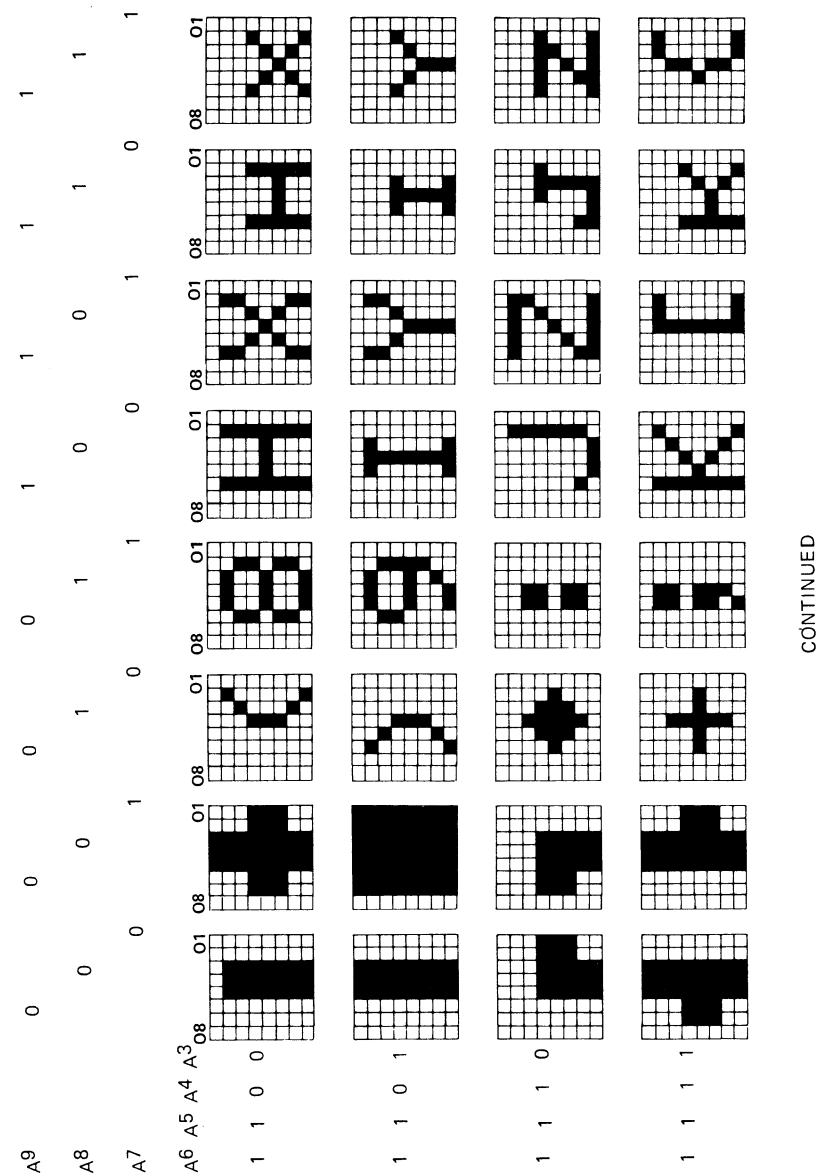
NOTE: Timing points are 90% (high) and 10% (low).

A9
A8
A7
A6 A5 A4 A3
0 0 0 0
0 0 0 1
0 0 1 0
0 0 1 1
01
08
VDU DISPLAYED CHARACTER SET
NOTE: 0 = VIL
1 = VIH


A9 A8 A7 A6 A5 A4 A3
0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1
0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1
0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1
0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1
0 1 0 0
0 1 0 1
0 1 1 0
0 1 1 1
01
08
CONTINUED

A9 A8 A7 A6 A5 A4 A3
0 0 0 0 0 0 0
0 0 0 0 0 0 1
0 0 0 0 0 1 0
0 0 0 0 0 1 1
0 0 0 0 1 0 0
0 0 0 0 1 0 1
0 0 0 0 1 1 0
0 0 0 0 1 1 1
1 0 0 0
1 0 0 1
1 0 1 0
1 0 1 1
01
08

CONTINUED

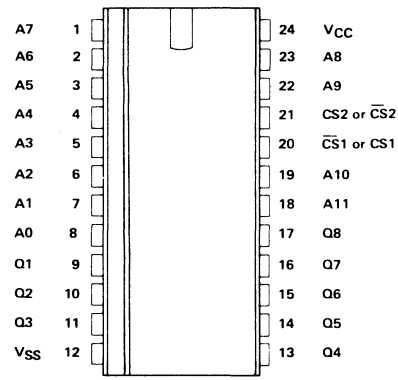

A9 A8 A7 A6 A5 A4 A3
O1
O8
CONTINUED

TMS 4732 JL, NL
4096-WORD BY 8-BIT READ-ONLY MEMORY

MAY 1977

- 4096 x 8 Organization
- All Inputs and Outputs TTL-Compatible
- Fully Static (No Clocks, No Refresh)
- Single 5 V Power Supply
- Maximum Access Time . . . 450 ns
- Minimum Cycle Time . . . 450 ns
- Typical Power Dissipation . . . 580 mW
- 3-State Outputs for OR-Ties
- Pin Compatible with TMS 4700, TMS 2708 and Intel 8316B
- Two Output Enable Controls for Chip Select Flexibility
- N-Channel Silicon-Gate Technology

24-PIN CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGES
(TOP VIEW)



description

The TMS 4732 is a 32,768-bit read-only memory organized as 4096 words of 8-bit length. This makes the TMS 4732 ideal for microprocessor based systems. The device is fabricated using N-channel silicon-gate technology for high speed and simple interface with bipolar circuits.

All inputs can be driven directly by Series 74 TTL circuits without the use of any external pull-up resistor. Each output can drive one Series 74 or 74S load without external resistors. The data outputs are three-state for OR-tieing multiple devices on a common bus. Two chip select controls allow data to be read. These controls are programmable, providing additional system decode flexibility. The data is always available, it is not dependent on external CE clocking.

The TMS 4732 is designed for high-density fixed-memory applications such as logic function generation and microprogramming. Systems utilizing the TMS 4700 1024 x 8-bit ROM or the TMS 2708 1024 x 8-bit EPROM can expand to the 4096 x 8-bit TMS 4732 with changes only to pins 18, 19, and 21. To upgrade from the 8316B, simply replace CS2 with A11 on pin 18.

This ROM is supplied in 24-pin dual-in-line plastic (NL suffix) or ceramic (JL suffix) packages designed for insertion in mounting-hold rows on 600-mil centers. The device is designed for operation from 0°C to 70°C.

operation

address (A0–A11)

The address-valid interval determines the device cycle time. The 12-bit positive-logic address is decoded on-chip to select one of 4096 words of 8-bit length in the memory array. A0 is the least-signifcant bit and A11 the most-significant bit of the word address.

chip select (CS1 and CS2)

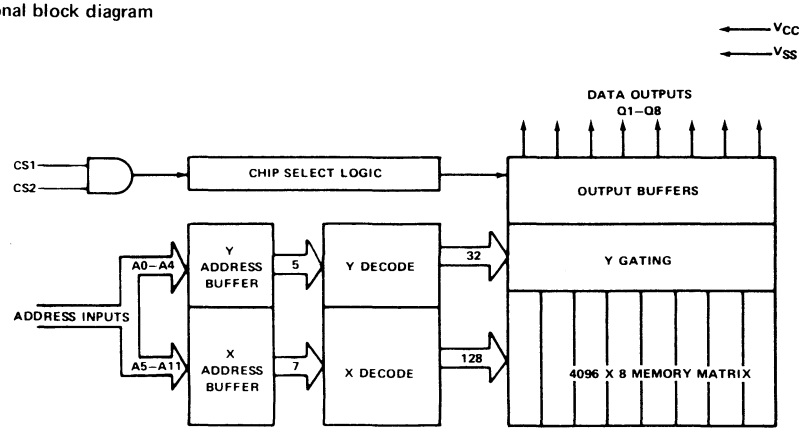
Each chip select control can be programmed during mask fabrication to be active with either a high or a low level input. When both chip select signals are active, all eight outputs are enabled and the eight-bit addressed word can be read. When either chip select is not active, all eight outputs are in a high-impedance state.

data out (Q1–Q8)

The eight outputs must be enabled by both chip select controls before the output word can be read. Data will remain valid until the address is changed or the outputs are disabled (chip deselected). When disabled, the three-state outputs are in a high-impedance state. Q1 is considered the least-significant bit, Q8 the most-significant bit.

The outputs will drive TTL circuits without external components.

functional block diagram



absolute maximum ratings

Supply voltage to ground potential (see Note 1) . . . . . –0.5 to 7 V
Applied output voltage (see Note 1) . . . . . –0.5 to 7 V
Applied input voltage (see Note 1) . . . . . –0.5 to 7 V
Power dissipation . . . . . 1 W
Ambient operating temperature . . . . . 0°C to 150°C
Storage temperature . . . . . –55°C to 150°C

Note 1: Voltage values are with respect to V_{SS}.

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2	2.4	V_{CC}	V
Low-level input voltage, V_{IL}	V_{SS}	0.5	0.65	V
Read cycle time, $t_{c(rd)}$	450			ns
Operating free-air temperature, T_A	0		70	°C

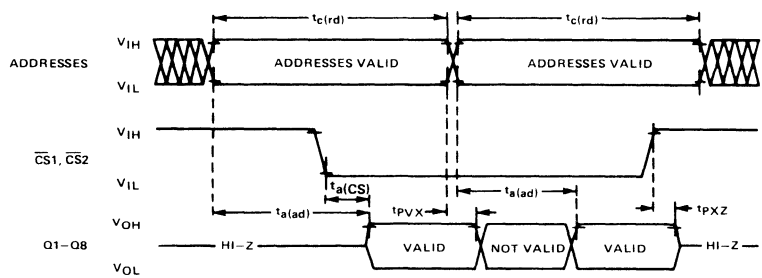
electrical characteristics, T_A = 0°C to 70°C, V_{DD} = 5 V +5% (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = 4.75 V,	I_{OH} −200 μA	2.4	V_{CC}	V
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V,	I_{OL} = 2 mA		0.4	V
I_I	Input current	V_{CC} = 5.25 V,	0V ≤ V_{IN} ≤ 5.25 V		10	μA
I_{OZ}	Output leakage current	V_O = 0.4 V to V_{CC}	Chip deselected		±10	μA
I_{CC}	Supply current from V_{CC}	V_{CC} = 5.25 V,	V_I = V_{CC} output not loaded		150	mA
C_i	Input capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		7	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		10	pF

switching characteristics, T_A = 0°C to 70°C, V_{CC} = 5 V +5%, 1 series 74 TTL load, C_L = 100 pF

PARAMETER		MIN	MAX	UNITS
$t_{a(ad)}$	Access time from address		450	ns
$t_{a(CS)}$	Access time from chip select		200	ns
t_{PVX}	Previous output data valid after address change		450	ns
t_{PXZ}	Output disable time fromchip select		200	ns

read cycle timing



TMS 4732 JL, NL
4096-WORD BY 8-BIT READ-ONLY MEMORY

PROGRAMMING DATA

PROGRAMMING REQUIREMENTS: The TMS 4732JL, NL is a fixed program memory in which the programming is performed by TI at the factory during manufacturing cycle to the specific customer inputs supplied in the format below. The device is organized as 4096 8-bit words with address locations numbered 0 to 4095. The 8-bit words can be coded as a 2-digit hexadecimal number between 00 and FF. All data words and addresses in the following format are coded in hexadecimal numbers. In coding, all binary words must be in positive logic before conversion to hexadecimal. Q1 is considered the least significant bit and Q8 the most significant bit. For addresses, A0 is least significant bit and A11 is the most significant bit.

Every card should include the TI Custom Device Number in the form ZAXXXX (4 digit number to be assigned by TI) in columns 75 through 80.

PROGRAMMABLE CHIP SELECTS: The chip select inputs shall be programmed according to the data punched in columns 73 and 74. Every card should include in column 73 a 1 if the output is to be enabled with a high level at CS2 or a 0 (zero) to enable the output with a low level at CS2. The column 74 entry is the same for programming CS1.

PROGRAMMED DATA FORMAT: The format for the cards to be supplied to TI to specify the data to be programmed is provided below. The card deck for each device consists of 128 cards with each card containing data for 32 memory locations.

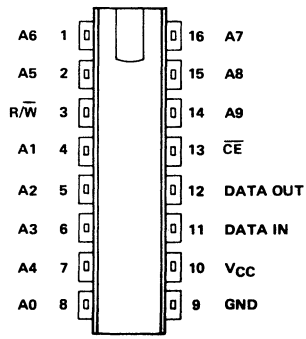
CARD COLUMN	HEXADECIMAL FORMAT
1 to 3	Hexadecimal address of first word on the card
4	Blank
5 to 68	Data. Each 8-bit memory byte is represented by two ASCII characters to represent a hexadecimal value of '00' to 'FF'.
69, 70	Checksum. The checksum is the negative of the sum of all 8-bit bytes in the record from columns 1 to 68, evaluate modulo 256 (carry from high order bit ignored). (For purposes of calculating the checksum, the value of Column 4 is defined to be zero). Adding together, modulo 256, all 8-bit bytes from Column 1 to 68 (Column 4 = 0), then adding the checksum, results in zero.
71, 72	Blank
73	One (1) to zero (0) for CS2
74	One (1) or zero (0) for CS1
75, 76	ZA
77 to 80	XXXX (4 digit number assigned by TI)

TMS 4033 JL, NL; TMS 4034 JL, NL; TMS 4035 JL, NL
1024-WORD BY 1-BIT STATIC RANDOM-ACCESS MEMORIES

BULLETIN NO. DL-S 7512189, OCTOBER 1974—REVISED MAY 1975

- 1024 x 1-Bit Organization
- Static Operation (No Clocks, No Refresh)
- Input Interface
  - Fully Decoded
  - TTL Compatible
  - Static Charge Protection
- Output Interface
  - 3-State
  - Fan-out 1 Series 74 TTL Load
  - OR-Tie Capability
- Access Time
  - TMS 4033 JL, NL . . . 450 ns Max
  - TMS 4034 JL, NL . . . 650 ns Max
  - TMS 4035 JL, NL . . . 1000 ns Max
- Interchangeable with Intel 2102-1, 2102-2, and 2102 Respectively
- N-Channel Silicon-Gate Technology

16-PIN CERAMIC AND PLASTIC DUAL-IN-LINE PACKAGES
(TOP VIEW)



description

This series is a family of static random-access memories, each organized as 1024 one-bit words. Due to their static design, system overhead costs are minimized by elimination of refresh-clocking circuitry and by simplification of the timing requirements. In addition all inputs and outputs are fully compatible with Series 74 TTL, including the single 5-volt power supply. These memories are fabricated by means of the same technology employed with the TMS 4030 JL, NL 4K RAM – N-channel silicon-gate. This technology provides optimum chip density and performance when cost is considered. Three performance ranges allow the designer to better match the memory to the specific system requirements, thereby maximizing the cost/performance trade-off.

The TMS 4033, TMS 4034, and TMS 4035 are offered in 16-pin dual-in-line ceramic (JL suffix) and plastic (NL suffix) packages designed for insertion in mounting-hole rows on 300-mil centers. These devices are characterized for operation from 0°C to 70°C.

operation

Addresses (A0-A9)

Address inputs are used to select individual storage locations within the RAM. Since the addresses are not latched, the address-valid time determines the cycle time during both the read and write cycle. Therefore, the address-valid time must be a minimum of 450 nanoseconds for the TMS 4033, 650 nanoseconds for the TMS 4034, and 1000 nanoseconds for the TMS 4035. The address inputs can be driven from standard Series 54/74 TTL with no external pull-up resistors.

operation (continued)

Chip Enable ($\overline{CE}$)

The $\overline{CE}$ input is used to enable the memory chip for a reading or writing operation. In a single-chip system, this pin can be hardwired to ground so that the chip is continuously enabled. For the read cycle, chip-enable low must extend past the address to ensure valid data for that address. Once the chip-enable goes high, the output buffer will immediately return to the high-impedance state. For the write cycle, chip-enable low must occur before the read/write input goes to the write state ensuring no ambiguity in the chip enabled for a particular write cycle. This input can be driven from Series 54/74 TTL with no external pull-up resistors.

Read/Write (R/$\overline{W}$)

In the write mode prior to an address change, R/$\overline{W}$ must be in the read state (high level) and must remain in that state for a minimum period to eliminate the possibility of data being written into an unwanted location. The read/write input is TTL compatible without external pull-up resistors.

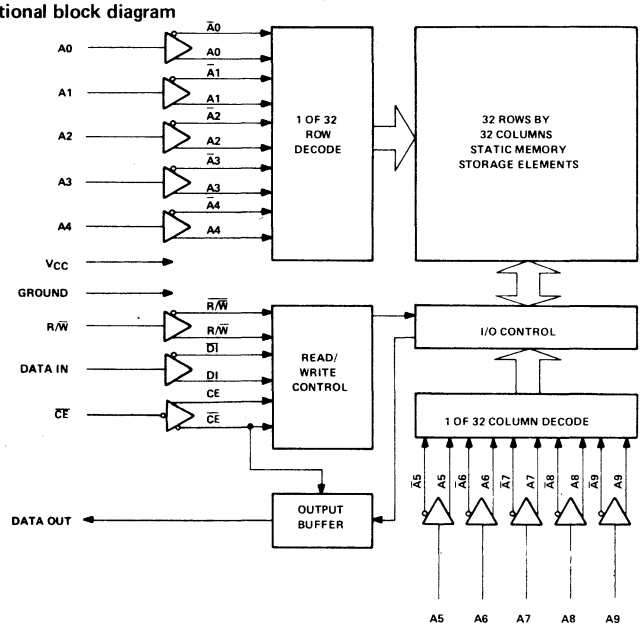
Data In (DI)

The DI input accepts the input data during the write mode. During a write cycle, data must be valid for a minimum time period before the read/write input is brought to the read state ensuring that proper data will enter the location selected. To eliminate any data ambiguity, data must be held valid past the end of the write pulse.

Data Out (DO)

Data out is a three-state terminal controlled by the chip-enable input, which supplies output data during a read cycle. A high level on chip enable places the data-out terminal in the high-impedance state.

functional block diagram



FUNCTION TABLE

$\overline{CE}$	R/$\overline{W}$	I/O
L	L	WRITE
L	H	READ
H	X	HIGH Z

H = HIGH LEVEL
L = LOW LEVEL

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{CC} (see Note 1) . . . . . –0.5 to 7 V
Input voltage (any input) (see Note 1) . . . . . –0.5 to 7 V
Continuous power dissipation . . . . . 1 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

NOTE 1: Voltage values are with respect to the ground terminal.

*COMMENT: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2.2		V_{CC}	V
Low-level input voltage, V_{IL} (see Note 2)	–0.3		0.65	V
Operating free-air temperature, T_A	0		70	°C

NOTE 2: The algebraic convention where the most negative limit is designated as minimum is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –100 µA,	V_{CC} = 4.75 V	2.2			V
V_{OL}	Low-level output voltage	I_{OL} = 1.9 mA,	V_{CC} = 5.25 V			0.45	V
I_I	Input current	V_I = 0 to 5.25 V				±10	µA
I_{OZH}	Off-state output current, high-level voltage applied	$\overline{CE}$ at 2.2 V,	V_O = 4 V			10	µA
I_{OZL}	Off-state output current, low-level voltage applied	$\overline{CE}$ at 2.2 V,	V_O = 0.45 V		–10	–100	µA
I_{CC}	Supply current from V_{CC}	V_{CC} = 5.25 V, All inputs at 5.25 V	Data out open,		45	70	mA
C_i	Input capacitance	T_A = 25°C,	f = 1 MHz		3	5	pF
C_o	Output capacitance	T_A = 25°C,	f = 1 MHz		7	10	pF

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

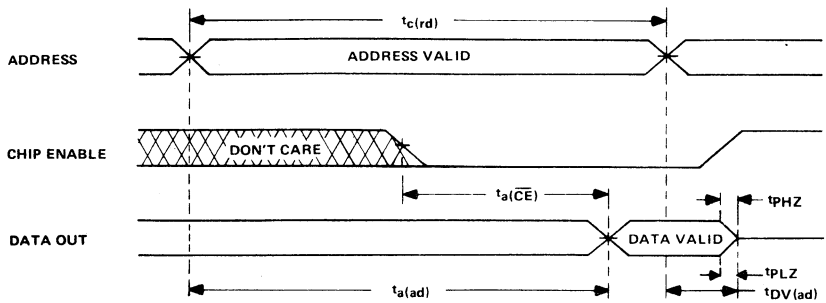
conditions for testing timing requirements

Input high levels . . . . . 2.2 V
Input low levels . . . . . 0.65 V
Input rise and fall times . . . . . 20 ns
Output load . . . . . 1 Series 74 TTL load, C_L = 100 pF
All timing requirements . . . . . 50% point of waveform

read cycle timing requirements over recommended supply voltage range, T_A = 0°C to 70°C (unless otherwise noted)

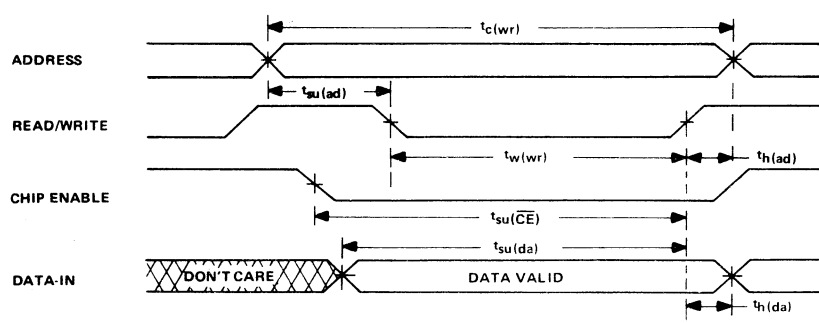
PARAMETER		TMS 4033			TMS 4034			TMS 4035			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	MIN	TYP†	MAX	
$t_{c(rd)}$	Read cycle time	450			650			1000			ns
$t_{a(ad)}$	Access time from address		300	450		450	650		500	1000	ns
$t_{a(\overline{CE})}$	Access time from chip enable			200			300			500	ns
$t_{DV(ad)}$	Previous output data valid from address	50			50			50			ns
t_{PHZ} or t_{PLZ}	Output disable time from chip enable	0		200	0		200	0		200	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.



write cycle timing requirements over recommended supply voltage range, T_A = 0°C to 70°C

PARAMETER		TMS 4033		TMS 4034		TMS 4035		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(wr)}$	Write cycle time	450		650		1000		ns
$t_{w(wr)}$	Write pulse width	250		400		750		ns
$t_{su(ad)}$	Address setup time	150		200		200		ns
$t_{su(\overline{CE})}$	Chip enable to write setup time	350		550		850		ns
$t_{su(da)}$	Data-in to write setup time	300		450		800		ns
$t_{h(ad)}$	Address hold time	50		50		50		ns
$t_{h(da)}$	Data hold time	50		50		50		ns



MOS
LSI

TMS 4036 JL, NL; TMS 4036-1 JL, NL; TMS 4036-2 JL, NL
64-WORD BY 8-BIT STATIC RANDOM-ACCESS MEMORIES

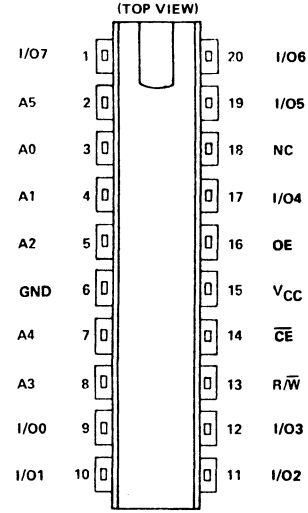
BULLETIN NO. DL-S 7512277, MAY 1975

- 64 x 8 Organization
- Static Operation (No Clocks, No Refresh)
- Compact 20-Pin 300-Mil Dual-in-Line Package
- 3 Performance Ranges:

	ACCESS TIME (MAX)	READ OR WRITE CYCLE (MIN)
TMS 4036	1000 ns	1000 ns
TMS 4036-1	650 ns	650 ns
TMS 4036-2	450 ns	450 ns

- Multiplexed Common Bus I/O
- Input Interface
  - Fully Decoded
  - TTL Compatible
  - Static Charge Protection
- Output Interface
  - 3-State
  - Fan-Out 1 Series 74 TTL Load
  - OR-Tie Capability
- Power Dissipation . . . 450 mW Maximum
- N-Channel Silicon-Gate Technology
- 8-Bit Word Length Ideal for Microprocessor-Based Systems

20-PIN CERAMIC AND PLASTIC DUAL-IN-LINE PACKAGES
(TOP VIEW)



description

This series of static random-access memories is organized as 64 words of 8 bits. Data inputs and outputs are multiplexed on an 8-bit, bidirectional bus controlled by the combination of chip enable and output enable. Static design results in reduced overhead costs by elimination of refresh-clocking circuitry and by simplification of the timing requirements. In addition, all inputs and outputs are fully compatible with Series 74 TTL, including the single 5-volt power supply. The TMS 4036 series is manufactured using TI's reliable N-channel silicon-gate technology to optimize the cost/performance relationship. Readout is nondestructive and the output data polarity is not inverted from data-in.

The TMS 4036 is offered in compact 20-pin ceramic (JL suffix) and plastic (NL suffix) dual-in-line packages designed for insertion in mounting-hole rows on 300-mil centers. The series is guaranteed for operation from 0°C to 70°C.

operation

addresses (A0-A5)

The 6-bit address selects one of 64 8-bit words. The address-valid time determines cycle time during both the read and write cycles. The address inputs can be driven directly from standard Series 54/74 TTL with no external pull-up resistors required.

operation (continued)

chip enable ($\overline{CE}$)

The $\overline{CE}$ terminal is used to enable a specific memory device. If $\overline{CE}$ is low, the device is enabled for either a read or write cycle, depending on the state of the read/write and output-enable terminals. When $\overline{CE}$ is high, the I/O buffers are in the high-impedance state. $\overline{CE}$ may be driven from Series 74 TTL. For a more complete understanding of $\overline{CE}$, see the section on output enable.

read/write (R/$\overline{W}$)

The R/$\overline{W}$ input must be high during read and low during write operations. Prior to an address change, R/$\overline{W}$ must be in the read state and must remain in that state for a minimum period to eliminate the possibility of data being written into an unwanted position. The R/$\overline{W}$ input is TTL-compatible and does not require external resistors.

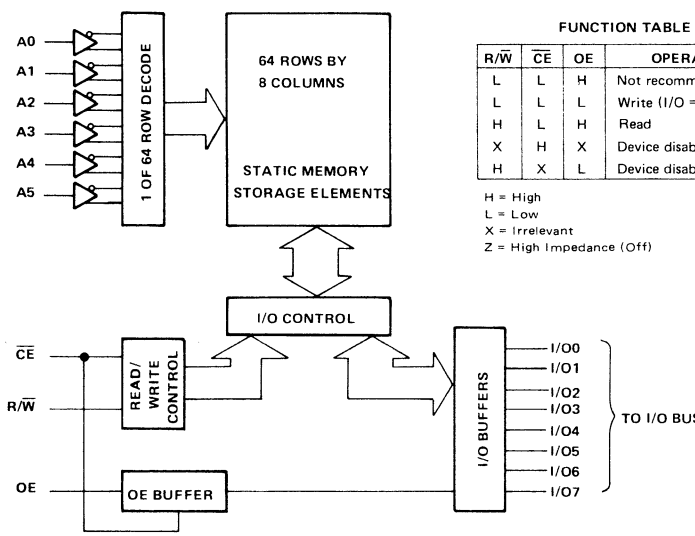
output enable (OE)

The output enable terminal controls the I/O buffer and determines whether the bus is in an input or output mode. When OE is low, the I/O terminals are in the input configuration; when OE is high, the I/O terminals are in the output configuration. The read cycle and write cycle timing diagrams show in detail the relation between $\overline{CE}$, OE, and the other signals (refer to the function table). This input is also compatible with Series 74 TTL circuits.

input/output buffer (I/O0-I/O7)

Each of these terminals interface directly with the external data bus and have the capability of being both an input and an output buffer. These buffers are controlled by a combination of $\overline{CE}$ and OE as described in the output enable section. Each buffer is three-state and fully TTL compatible, both as an input and an output.

functional block diagram



FUNCTION TABLE

R/$\overline{W}$	$\overline{CE}$	OE	OPERATION
L	L	H	Not recommended
L	L	L	Write (I/O = Z)
H	L	H	Read
X	H	X	Device disabled (I/O = Z)
H	X	L	Device disabled (I/O = Z)

H = High
L = Low
X = Irrelevant
Z = High Impedance (Off)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{CC} (see Notes 1 and 2) . . . . . −0.5 to 7 V
Input voltage (any input) (see Notes 1 and 2) . . . . . −0.5 to 7 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES:
1. Voltage values are with respect to the ground terminal.
2. For all combinations of inputs, the I/O lines may be shorted to V_{SS} or V_{CC} for a period not to exceed five milliseconds.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

PARAMETER	TMS 4036			TMS 4036-1			TMS 4036-2			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	V
Supply voltage, V_{SS}		0			0			0		V
High-level input voltage, V_{IH}	2.2		V_{CC}	2.2		V_{CC}	2.2		V_{CC}	V
Low-level input voltage, V_{IL} (see Note 3)	−0.3		0.8	−0.3		0.8	−0.3		0.8	V
Read cycle time, $t_{c(rd)}$	1000			650			450			ns
Write cycle time, $t_{c(wr)}$	1000			650			450			ns
Write pulse width, $t_{w(wr)}$	500			300			200			ns
Address setup time, $t_{su(ad)}$	450			300			200			ns
Chip-enable setup time, $t_{su(\overline{CE})}$	700			500			400			ns
Data setup time, $t_{su(da)}$	600			400			300			ns
Address hold time, $t_{h(ad)}$	50			50			50			ns
Data hold time, $t_{h(da)}$	50			50			50			ns
Operating free-air temperature, T_A	0		70	0		70	0		70	°C

NOTE 3: The albegraic convention where the most negative limit is designated as minimum is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

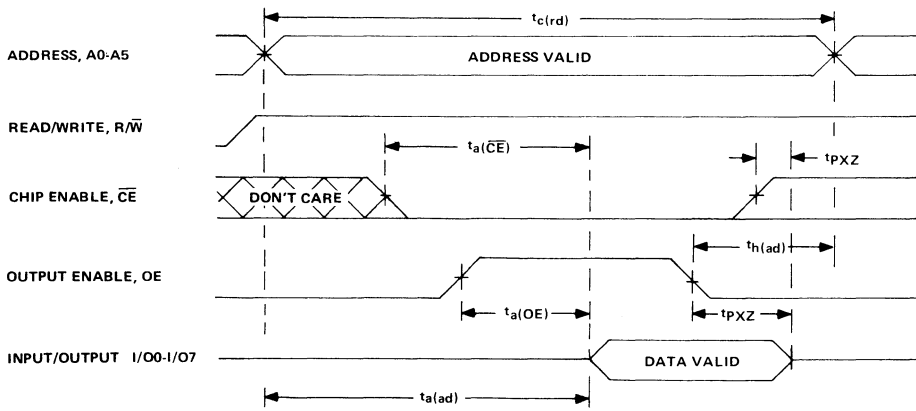
PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −100 μA,	V_{CC} = 4.75 V	2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 1.9 mA,	V_{CC} = 4.75 V		0.4	V
I_{IH}	High-level input current into address, R/$\overline{W}$, $\overline{CE}$, or OE	V_I = 5.25 V			10	μA
I_{OZH}	Off-state output current, high-level voltage applied at I/O terminal	V_O = 5.25 V, $\overline{CE}$ at 5.25 V	OE at 0 V,		10	μA
		V_O = 5.25 V, $\overline{CE}$ at 2.2 V	OE at 5.25 V,		10	
		V_O = 5.25 V, $\overline{CE}$ at 0 V	OE at 0.8 V,		10	
I_{OZL}	Off-state output current, low-level voltage applied at I/O terminal	V_O = 0 V, $\overline{CE}$ at 2.2 V	OE at 5.25 V,		−100	μA
		V_O = 0 V, $\overline{CE}$ at 0 V	OE at 0.8 V,		−100	
I_{CC}	Supply current from V_{CC}				85	mA
C_i	Input capacitance	f = 1 MHz,	T_A = 25°C		10	pF
$C_{i/o}$	I/O terminal capacitance	f = 1 MHz,	T_A = 25°C		20	pF

switching characteristics over recommended supply voltage ranges, T_A = 0°C to 70°C

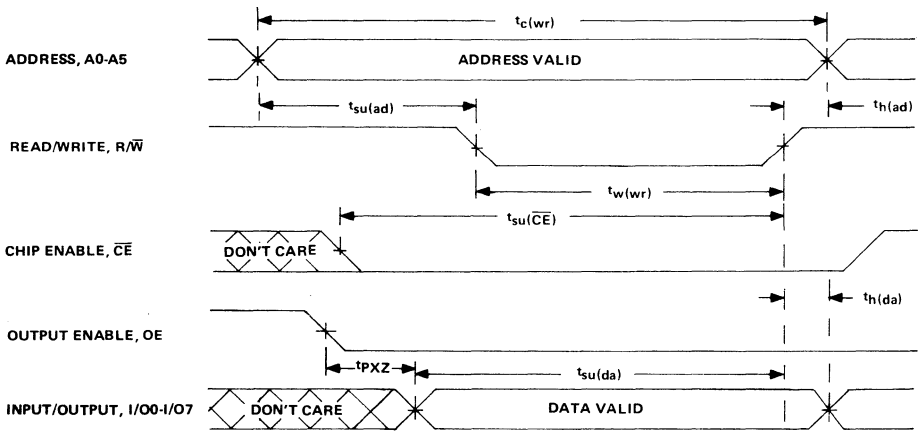
PARAMETER		TMS 4036			TMS 4036-1			TMS 4036-2			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	MIN	TYP†	MAX	
$t_{a(ad)}$	Access time from address			1000			650			450	ns
$t_{a(\overline{CE})}$	Access time from chip enable			200			190			180	ns
$t_{a(OE)}$	Access time from output enable			200			190			180	ns
t_{PXZ}	Output disable time from chip enable	0	60	200	0	60	200	0	60	200	ns
t_{PXZ}	Output disable time from output enable (see Note 4)	0	60	200	0	60	200	0	60	200	ns

NOTE 4: This parameter defines the delay for the I/O bus to enter the input mode.
†All typical values are at T_A = 25°C.

read cycle timing



write cycle timing



NOTE: For measuring timing requirements and characteristics, V_{IH} = 2.2 V, V_{IL} = 0.65 V, $t_r = t_f$ = 20 ns and all timing points are 50% points.

TMS 4039 JL, NL; TMS 4039-1 JL, NL; TMS 4039-2 JL, NL
256-WORD BY 4-BIT STATIC RANDOM-ACCESS MEMORIES

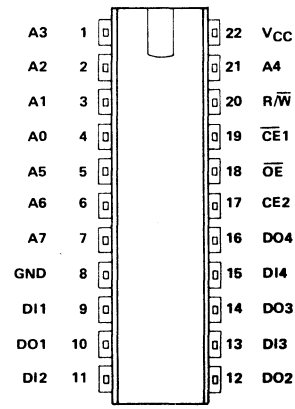
BULLETIN NO. DL-S 7512271, MAY 1975

- 256 x 4 Organization
- Static Operation (No Clocks, No Refresh)
- 3 Performance Ranges:

	ACCESS TIME (MAX)	READ OR WRITE CYCLE (MIN)
TMS 4039	1000 ns	1000 ns
TMS 4039-1	650 ns	650 ns
TMS 4039-2	450 ns	450 ns

- Input Interface
  - Fully Decoded
  - TTL-Compatible
  - Static Charge Protection
- Output Interface
  - Two Chip-Enable Inputs for OR-Tie Capability
  - Fan-out to 1 Series 74 TTL Load
  - 3-State Outputs and Output Enable Control for Common I/O Data Bus Systems
- Power Dissipation . . . 175 mW Typical
- Organized for Microprocessor-Based Systems
- Interchangeable with Intel 2101, 2101-2, and 2101-1, Respectively

22-PIN CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGES
(TOP VIEW)



description

This series of static random-access memories is organized as 256 words of 4 bits. Static design results in reduced overhead costs by elimination of refresh-clocking circuitry and by simplification of timing requirements. All inputs and outputs are fully compatible with Series 74 TTL, including the single 5-volt power supply. The TMS 4039 series is manufactured using TI's reliable N-channel enhancement-type silicon-gate technology to optimize the cost/performance relationship. Readout is nondestructive and output data is not inverted from data in.

The TMS 4039 series is offered in 22-pin dual-in-line ceramic (JL suffix) and plastic (NL suffix) packages designed for insertion in mounting-hole rows on 400-mil centers. The series is characterized for operation from 0°C to 70°C.

operation

addresses (A0-A7)

The eight address inputs select one of 256 4-bit words. The address inputs can be driven directly from standard Series 54/74 TTL with no external pull-up resistors.

chip enable ($\overline{CE}$1 and CE2)

To enable the device, $\overline{CE}$1 must be low and CE2 must be high. The two chip-enable terminals can be driven from a common source with an inverter or either terminal can be hard wired to its enabled level. When the memory is disabled, data cannot be entered and the outputs are in the high-impedance state.

operation (continued)

read/write (R/$\overline{W}$)

The R/$\overline{W}$ input must be high during read and low during write operations. Prior to an address change, R/$\overline{W}$ must be in the read state and must remain in that state for a minimum period to eliminate the possibility of data being written into an unwanted position. The R/$\overline{W}$ input is TTL-compatible and does not require external resistors.

output enable ($\overline{OE}$)

The output enable must be low to read for when it is high the outputs are in the high-impedance state useful for OR-ties or common input/output operation. When the device is not used in the common-input/output configuration, the output enable terminal can be hard wired low.

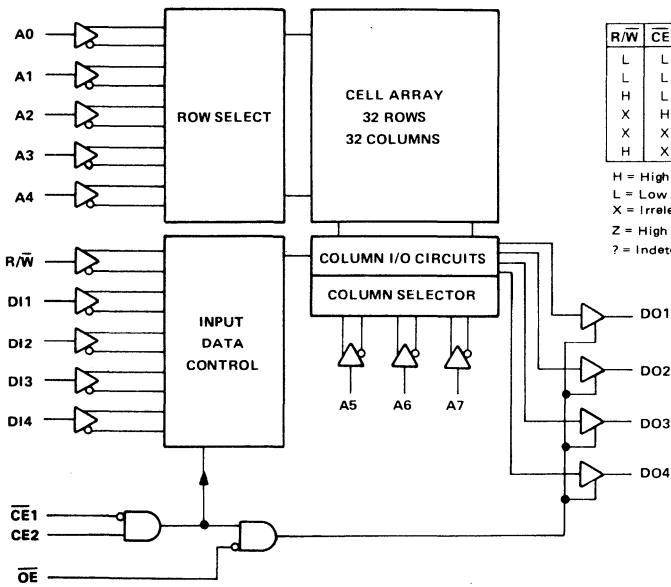
data in (DI1-DI4)

The DI inputs accept input data during a write operation. During a write cycle, data must be set up a minimum time before R/$\overline{W}$ goes to the read state (high) to ensure that correct data will enter the addressed memory cell. Also, input data must be held valid a minimum time after the rise of R/$\overline{W}$.

data out (DO1-DO4)

Data out is a three-state terminal controlled by $\overline{OE}$, $\overline{CE}$1, and CE2. To read data, $\overline{CE}$1 and $\overline{OE}$ must be low with CE2 high. When $\overline{OE}$ or $\overline{CE}$1 goes high or CE2 goes low, the output terminals are forced to the high-impedance state.

functional block diagram



FUNCTION TABLE

R/$\overline{W}$	$\overline{CE}$1	CE2	$\overline{OE}$	OPERATION
L	L	H	L	Write (DO = ?)
L	L	H	H	Write (DO = Z)
H	L	H	L	Read
X	H	X	X	Device Disabled (DO = Z)
X	X	L	X	Device Disabled (DO = Z)
H	X	X	H	Device Disabled (DO = Z)

H = High
L = Low
X = Irrelevent
Z = High Impedance
? = Indeterminate

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{CC} (see Note 1) . . . . . −0.5 to 7 V
Input voltage (any input) (see Note 1) . . . . . −0.5 to 7 V
Continuous power dissipation . . . . . 1 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to the ground terminal.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

PARAMETER	TMS 4039			TMS 4039-1			TMS 4039-2			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	V
High-level input voltage, V_{IH}	2.2		V_{CC}	2.2		V_{CC}	2.2		V_{CC}	V
Low-level input voltage, V_{IL} (see Note 2)	−0.5		0.65	−0.5		0.65	−0.5		0.65	V
Read cycle time, $t_{c(rd)}$	1000			650			450			ns
Write cycle time, $t_{c(wr)}$	1000			650			450			ns
Write pulse width, $t_{w(wr)}$	800			450			300			ns
Address setup time, $t_{su(ad)}$	150			150			100			ns
Chip-enable setup time, $t_{su(CE)}$	900			550			400			ns
Data setup time, $t_{su(da)}$	700			400			280			ns
Address hold time, $t_{h(ad)}$	50			50			50			ns
Data hold time, $t_{h(da)}$	100			100			100			ns
Operating free-air temperature, T_A	0		70	0		70	0		70	°C

NOTE 2: The algebraic convention where the most negative limit is designated as minimum is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −150 µA,	V_{CC} = 4.75 V	2.2			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA,	V_{CC} = 5.25 V			0.45	V
I_I	Input current	V_I = 0 to 5.25 V				±10	µA
I_{OZH}	Off-state output current, high-level voltage applied	$\overline{CE}$ at 2.2 V,	V_O = 4 V			15	µA
I_{OZL}	Off-state output current, low-level voltage applied	$\overline{CE}$ at 2.2 V,	V_O = 0.45 V			−50	µA
I_{CC}	Supply current from V_{CC}	V_{CC} = 5.25 V, I_O = 0 mA	T_A = 25°C			60	mA
			T_A = 0°C			70	
C_i	Input capacitance	V_I = 0 V, f = 1 MHz	T_A = 25°C,		4	8	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		8	12	pF

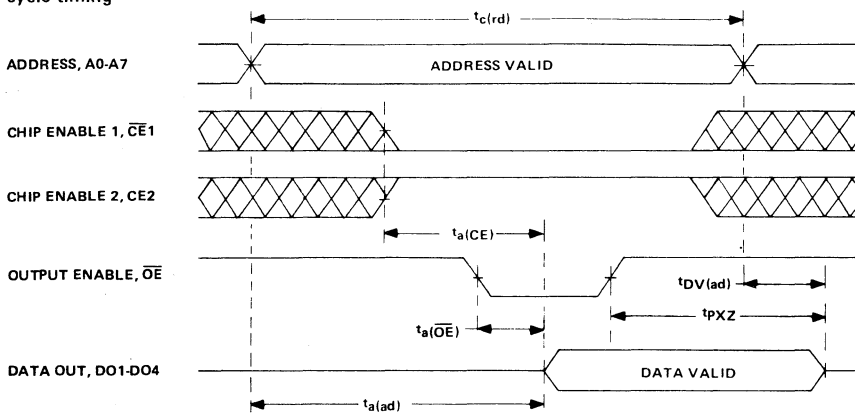
†All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended supply voltage range, T_A = 0°C to 70°C, 1 Series 74 TTL load, C_L = 100 pF

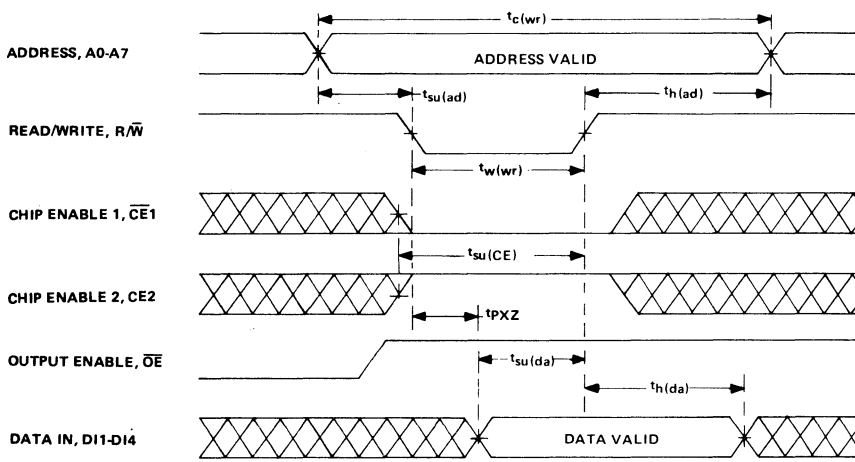
PARAMETER		TMS 4039		TMS 4039-1		TMS 4039-2		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(ad)}$	Access time from address		1000		650		450	ns
$t_{a(CE)}$	Access time from chip enable $\overline{CE1}$ or CE2		800		400		350	ns
$t_{a(\overline{OE})}$	Access time from output enable		700		350		300	ns
$t_{DV(ad)}$	Previous output data valid after address change	40		40		40		ns
t_{PXZ}	Output disable time from output enable (see Note 3)	0	200	0	150	0	150	ns

NOTE 3: With the outputs OR-tied to the inputs, this parameter defines the delay for the I/O bus to enter the input mode.

read cycle timing



write cycle timing



NOTE: For measuring timing requirements and characteristics, V_{IH} = 2.2 V, V_{IL} = 0.65 V, $t_r = t_f$ = 20 ns and all timing points are 50% points.

TMS 4042 JL, NL; TMS 4042-1 JL, NL; TMS 4042-2 JL, NL
256-WORD BY 4-BIT STATIC RANDOM-ACCESS MEMORIES

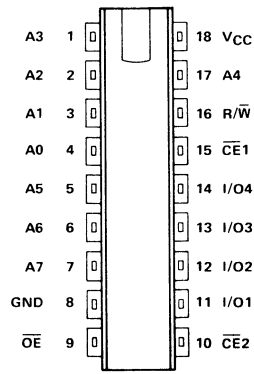
BULLETIN NO. DL-S 7512269, MAY 1975

- 256 x 4 Organization
- Common I/O
- 18-Pin Package
- Static Operation (No Clocks, No Refresh)
- 3 Performance Ranges:

	ACCESS TIME (MAX)	READ OR WRITE CYCLE (MIN)
TMS 4042	1000 ns	1000 ns
TMS 4042-1	650 ns	650 ns
TMS 4042-2	450 ns	450 ns

- Input Interface
  - Fully Decoded
  - TTL-Compatible
  - Static Charge Protection
- Output Interface
  - Two Chip-Enable Inputs for OR-Tie Capability
  - Fan-out to 1 Series 74 TTL Load
  - 3-State Outputs and Output Enable Control for Common I/O Data Bus Systems
- Power Dissipation . . . 175 mW Typical
- Organized for Microprocessor-Based Systems
- Interchangeable with Intel 2111, 2111-2, and 2111-1, Respectively

18-PIN CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGES
(TOP VIEW)



description

This series of static random-access memories is organized as 256 words of 4 bits. Static design results in reduced overhead costs by elimination of refresh-clocking circuitry and by simplification of timing requirements. The use of common input/output terminals, controlled by the chip enable and output enable terminals, allows the use of an 18-pin package and saves board space in comparison to the TMS 4039. The common input/outputs are fully compatible with Series 74 TTL. The device requires a single 5-volt power supply. The TMS 4042 series is manufactured using TI's reliable N-channel enhancement-type silicon-gate technology to optimize the cost/performance relationship. Readout is nondestructive and output data is not inverted from data in.

The TMS 4042 series is offered in 18-pin dual-in-line ceramic (JL suffix) and plastic (NL suffix) packages designed for insertion in mounting-hole rows on 300-mil centers. The series is characterized for operation from 0°C to 70°C.

operation

addresses (A0-A7)

The eight address inputs select one of 256 4-bit words. The address inputs can be driven directly from standard Series 54/74 TTL with no external pull-up resistors.

chip enable 1 and chip enable 2 ($\overline{CE}1$ and $\overline{CE}2$)

To enable the device, $\overline{CE}1$ and $\overline{CE}2$ must be low. The two chip-enable terminals can be driven from a common source or either terminal can be hard wired low. When the memory is disabled, data cannot be entered and the outputs are in the high-impedance state.

operation (continued)

read/write (R/$\overline{W}$)

The R/$\overline{W}$ input must be high during read and low during write operations. Prior to an address change, R/$\overline{W}$ must be in the read state and must remain in that state for a minimum period to eliminate the possibility of data being written into an unwanted position. The R/$\overline{W}$ input is TTL-compatible and does not require external resistors.

output enable ($\overline{OE}$)

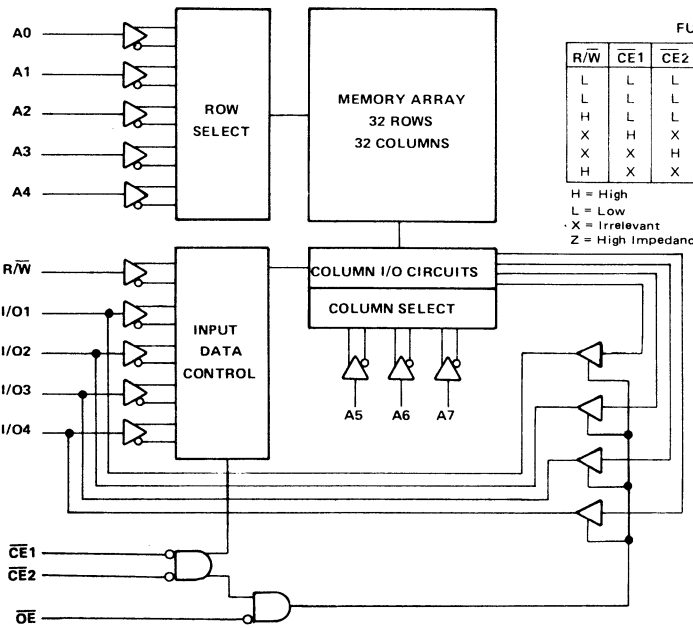
The output enable must be low to read for when it is high the outputs are in the high-impedance state.

input/output (I/O1-I/O4)

The common input/output terminals are used for both read and write operations. During a write cycle, data must be set up a minimum time before R/$\overline{W}$ goes to the read state (high) to ensure that correct data will enter the addressed memory cell. Also, input data must be held valid a minimum time after the rise of R/$\overline{W}$.

The output buffers are three-state and are controlled by $\overline{OE}$, $\overline{CE}1$, and $\overline{CE}2$. The input buffers are controlled by R/$\overline{W}$, $\overline{CE}1$, and $\overline{CE}2$. To read data, $\overline{CE}1$, $\overline{CE}2$, and $\overline{OE}$ must be low. If any one of these three inputs goes to the high level, the output terminals are forced to the high-impedance state. The common I/O terminals can be driven directly by Series 74 TTL and the buffers can drive Series 74 TTL circuits without external resistors.

functional block diagram



FUNCTION TABLE

R/$\overline{W}$	$\overline{CE}1$	$\overline{CE}2$	$\overline{OE}$	OPERATION
L	L	L	L	Not recommended
L	L	L	H	Write (I/O = Z)
H	L	L	L	Read
X	H	X	X	Device Disabled (I/O = Z)
X	X	H	X	Device Disabled (I/O = Z)
H	X	X	H	Device Disabled (I/O = Z)

H = High
L = Low
X = Irrelevant
Z = High Impedance

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{CC} (see Note 1) . . . . . −0.5 to 7 V
Input voltage (any input) (see Note 1) . . . . . −0.5 to 7 V
Continuous power dissipation . . . . . 1 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to the ground terminal.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

PARAMETER	TMS 4042			TMS 4042-1			TMS 4042-2			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	V
High-level input voltage, V_{IH}	2.2		V_{CC}	2.2		V_{CC}	2.2		V_{CC}	V
Low-level input voltage, V_{IL} (see Note 2)	−0.5		0.65	−0.5		0.65	−0.5		0.65	V
Read cycle time, $t_{c(rd)}$	1000			650			450			ns
Write cycle time, $t_{c(wr)}$	1000			650			450			ns
Write pulse width, $t_{w(wr)}$	800			450			300			ns
Address setup time, $t_{su(ad)}$	150			150			100			ns
Chip enable setup time, $t_{su(\overline{CE})}$	900			550			400			ns
Data setup time, $t_{su(da)}$	700			400			280			ns
Address hold time, $t_{h(ad)}$	50			50			50			ns
Data hold time, $t_{h(da)}$	100			100			100			ns
Operating free-air temperature, T_A	0		70	0		70	0		70	°C

NOTE 2: The algebraic convention where the most negative limit is designated as minimum is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −150 μA,	V_{CC} = 4.75 V	2.2			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA,	V_{CC} = 5.25 V			0.45	V
I_I	Input current	V_I = 0 to 5.25 V				±10	μA
I_{OZH}	Off-state output current, high-level voltage applied	$\overline{CE}$ at 2.2 V,	V_O = 4 V			15	μA
I_{OZL}	Off-state output current, low-level voltage applied	$\overline{CE}$ at 2.2 V,	V_O = 0.45 V			−50	μA
I_{CC}	Supply current from V_{CC}	V_{CC} = 5.25 V, I_O = 0 mA	T_A = 25°C			60	mA
			T_A = 0°C			70	
C_i	Input capacitance	V_I = 0 V, f = 1 MHz	T_A = 25°C,		4	8	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		10	15	pF

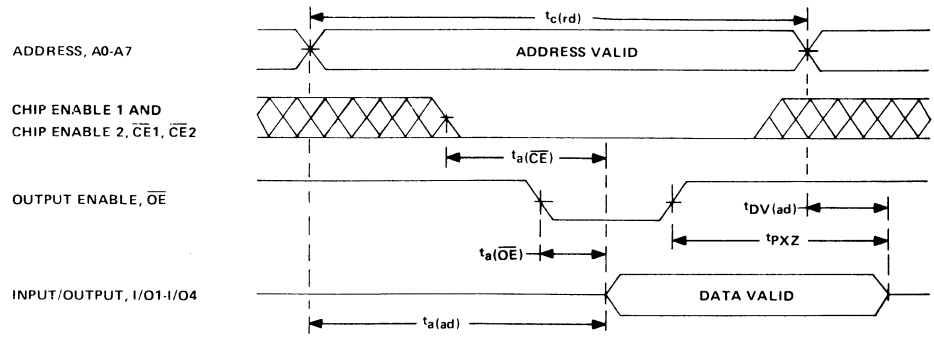
†All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended supply voltage range, T_A = 0°C to 70°C, 1 Series 74 TTL load, C_L = 100 pF

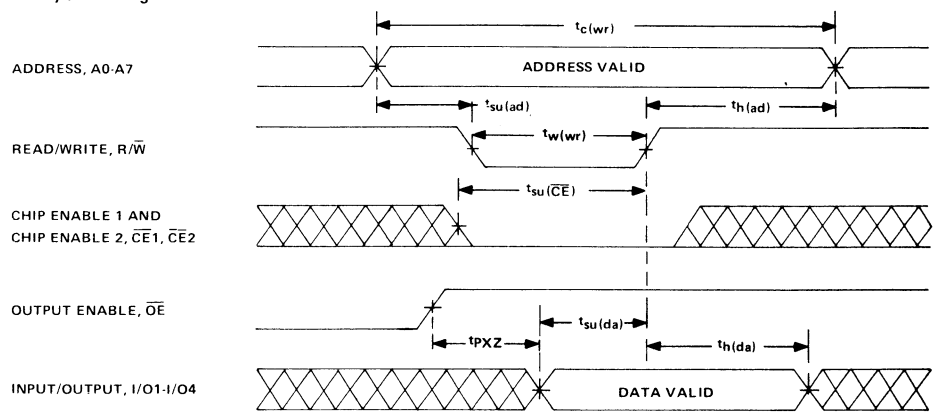
PARAMETER		TMS 4042		TMS 4042-1		TMS 4042-2		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(ad)}$	Access time from address		1000		650		450	ns
$t_{a(\overline{CE})}$	Access time from chip enable $\overline{CE}1$ or $\overline{CE}2$		800		400		350	ns
$t_{a(\overline{OE})}$	Access time from output enable		700		350		300	ns
$t_{DV(ad)}$	Previous output data valid after address change	40		40		40		ns
t_{PXZ}	Output disable time from output enable (see Note 3)	0	200	0	150	0	150	ns

NOTE 3: This parameter defines the delay for the I/O bus to enter the input mode.

read cycle timing



write cycle timing



NOTE: For measuring timing requirements and characteristics, V_{IH} = 2.2 V, V_{IL} = 0.65 V, t_r = t_f = 20 ns and all timing points are 50% points.

TMS 4043 JL, NL; TMS 4043-1 JL, NL; TMS 4043-2 JL, NL
256-WORD BY 4-BIT STATIC RANDOM-ACCESS MEMORIES

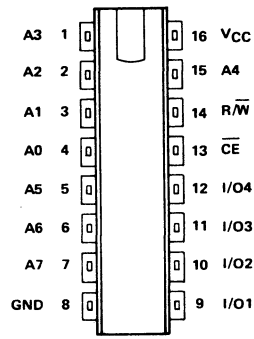
BULLETIN NO. DL-S 7512270, MAY 1975

- 256 x 4 Organization
- Common I/O
- 16-Pin Package
- Static Operation (No Clocks, No Refresh)
- 3 Performance Ranges:

	ACCESS TIME (MAX)	READ OR WRITE CYCLE (MIN)
TMS 4043	1000 ns	1000 ns
TMS 4043-1	650 ns	650 ns
TMS 4043-2	450 ns	450 ns

- Input Interface
  - Fully Decoded
  - TTL-Compatible
  - Static Charge Protection
- Output Interface
  - Chip-Enable Input and 3-State Outputs for OR-Tie Capability in Common I/O Data Bus Systems
  - Fan-out to 1 Series 74 TTL Load
- Power Dissipation . . . 175 mW Typical
- Organized for Microprocessor-Based Systems
- TMS 4043 and TMS 4043-1 Are Interchangeable with Intel 2112 and 2112-2, Respectively

16-PIN CERAMIC AND PLASTIC DUAL-IN-LINE PACKAGES
(TOP VIEW)



description

This series of static random-access memories is organized as 256 words of 4 bits. Static design results in reduced overhead costs by elimination of refresh-clocking circuitry and by simplification of timing requirements. The use of common input/output terminals, controlled by the chip enable and read/write terminals, allows the use of a 16-pin package and saves board space in comparison to the TMS 4039 or TMS 4042. The common input/outputs are fully compatible with Series 74 TTL. The device requires a single 5-volt power supply. The TMS 4043 series is manufactured using TI's reliable N-channel enhancement-type silicon-gate technology to optimize the cost/performance relationship. Readout is nondestructive and output data is not inverted from data in.

The TMS 4043 series is offered in 16-pin dual-in-line ceramic (JL suffix) and plastic (NL suffix) packages designed for insertion in mounting-hole rows on 300-mil centers. The series is characterized for operation from 0°C to 70°C.

operation

addresses (A0-A7)

The eight address inputs select one of 256 4-bit words. The address inputs can be driven directly from standard Series 54/74 TTL with no external pull-up resistors.

chip enable ($\overline{CE}$)

To enable the device, $\overline{CE}$ must be low. When the memory is disabled, data cannot be entered and the outputs are in the high-impedance state.

operation (continued)

read/write (R/$\overline{W}$)

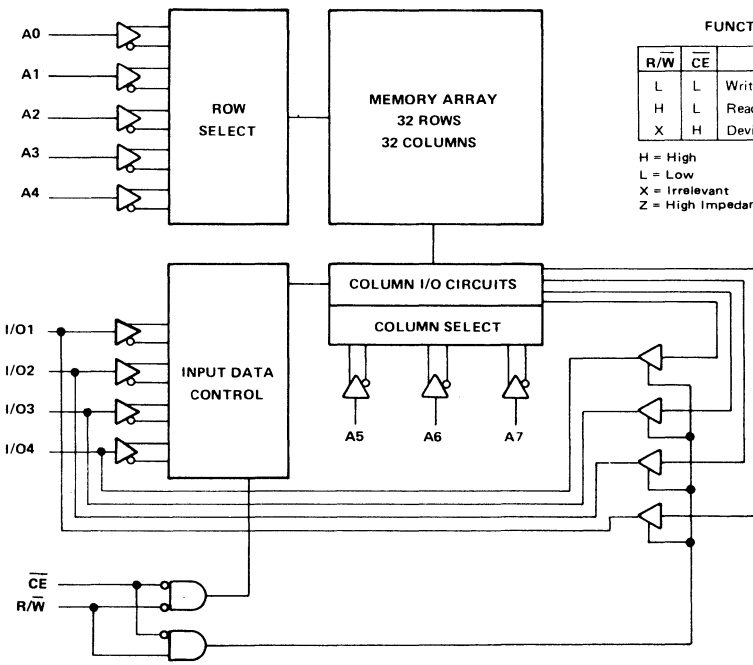
The R/$\overline{W}$ input must be high during read and low during write operations. Prior to an address change, R/$\overline{W}$ must be in the read state and must remain in that state for a minimum period to eliminate the possibility of data being written into an unwanted position. The R/$\overline{W}$ input is TTL-compatible and does not require external resistors.

input/output (I/O1-I/O4)

The common input/output terminals are used for both read and write operations. During a write cycle, data must be set up a minimum time before R/$\overline{W}$ goes to the read state (high) to ensure that correct data will enter the addressed memory cell. Also, input data must be held valid a minimum time after the rise of R/$\overline{W}$.

The output buffers are three-state and they are controlled by $\overline{CE}$ and R/$\overline{W}$. If $\overline{CE}$ goes high or R/$\overline{W}$ goes low, the output terminals are forced to the high-impedance state. The input buffers are also controlled by $\overline{CE}$ and R/$\overline{W}$. To read data, $\overline{CE}$ must be low and R/$\overline{W}$ high. The common I/O terminals can be driven directly by Series 74 TTL and the buffers can drive Series 74 TTL circuits without external resistors.

functional block diagram



FUNCTION TABLE

R/$\overline{W}$	$\overline{CE}$	OPERATION
L	L	Write (I/O = Z)
H	L	Read
X	H	Device disabled (I/O = Z)

H = High
L = Low
X = Irrelevant
Z = High Impedance

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{CC} (see Note 1) . . . . . −0.5 to 7 V
Input voltage (any input) (see Note 1) . . . . . −0.5 to 7 V
Continuous power dissipation . . . . . 1 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to the ground terminal.
*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

PARAMETER	TMS 4043			TMS 4043-1			TMS 4043-2			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	V
High-level input voltage, V_{IH}	2.2		V_{CC}	2.2		V_{CC}	2.2		V_{CC}	V
Low-level input voltage, V_{IL} (see Note 2)	−0.5		0.65	−0.5		0.65	−0.5		0.65	V
Read cycle time, $t_{c(rd)}$	1000			650			450			ns
Write cycle time, $t_{c(wr)}$	1000			650			450			ns
Address setup time, $t_{su(ad)}$	150			100			50			ns
Chip-enable setup time, $t_{su(\overline{CE})}$	0			0			0			ns
Data setup time, $t_{su(da)}$	600			300			150			ns
Address hold time, $t_{h(ad)}$	50			50			50			ns
Chip-enable hold time, $t_{h(\overline{CE})}$	0			0			0			ns
Data hold time, $t_{h(da)}$	100			50			50			ns
Operating free-air temperature, T_A	0		70	0		70	0		70	C

NOTE 2: The algebraic convention where the most negative limit is designated as minimum is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −150 μA,	V_{CC} = 4.75 V	2.2			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA,	V_{CC} = 5.25 V			0.45	V
I_I	Input current	V_I = 0 to 5.25 V				±10	μA
I_{OZH}	Off-state output current, high-level voltage applied	$\overline{CE}$ at 2.2 V,	V_O = 4 V			15	μA
I_{OZL}	Off-state output current, low-level voltage applied	$\overline{CE}$ at 2.2 V,	V_O = 0.45 V			−50	μA
I_{CC}	Supply current from V_{CC}	V_{CC} = 5.25 V, I_O = 0 mA	T_A = 25°C			60	mA
			T_A = 0°C			70	
C_i	Input capacitance	V_I = 0 V, f = 1 MHz	T_A = 25°C,		4	8	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		10	15	pF

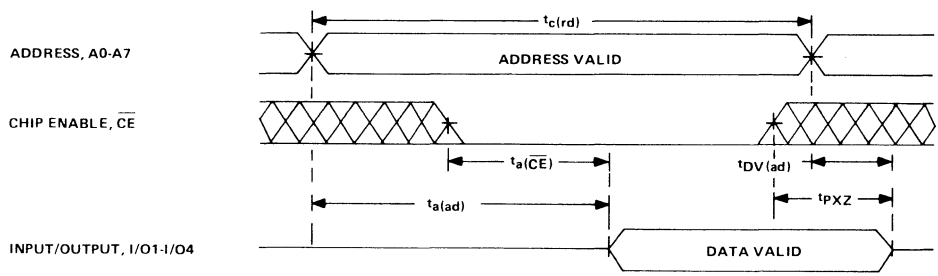
†All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended supply voltage range, T_A = 0°C to 70°C, 1 Series 74 TTL load, C_L = 100 pF

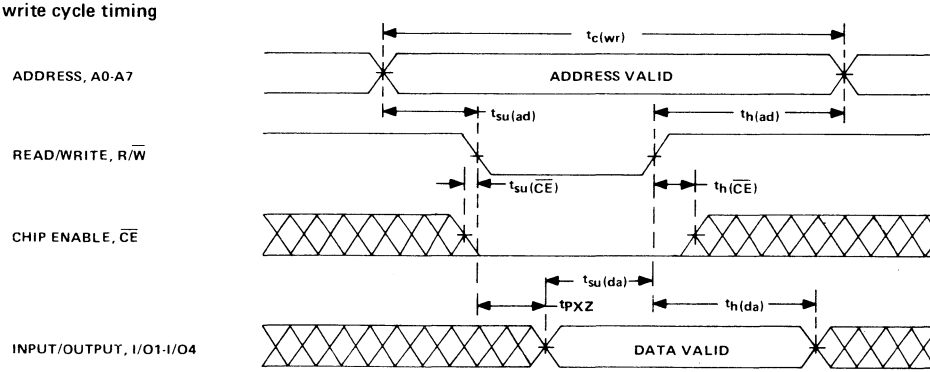
PARAMETER		TMS 4043		TMS 4043-1		TMS 4043-2		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(ad)}$	Access time from address		1000		650		450	ns
$t_{a(\overline{CE})}$	Access time from chip enable		800		500		350	ns
$t_{DV(ad)}$	Previous output data valid after address change	40		40		40		ns
t_{PXZ}	Output disable time from chip enable (see Note 3)	0	200	0	150	0	150	ns
t_{PXZ}	Output disable time from read/write (see Note 3)		200		200		200	ns

NOTE 3: This parameter defines the delay for the I/O bus to enter the input mode.

read cycle timing



write cycle timing



NOTE: For measuring timing requirements and characteristics, V_{IH} = 2.2 V, V_{IL} = 0.65 V, $t_r = t_f$ = 20 ns and all timing points are 50% points.

TMS 4044, -45, -30, -25, -20, -15 JL, NL
TMS 4046, -45, -30, -25, -20, -15 JL, NL
4096 WORD BY 1-BIT STATIC RAMs

MAY 1977

- 4096 x 1 Organization
- Single +5 V Supply (± 10% Tolerance)
- High Density 300-mil 18- and 20-Pin Packages
- Fully Static Operation (No Clocks, No Refresh, No Timing Strobe)
- 5 Performance Ranges:

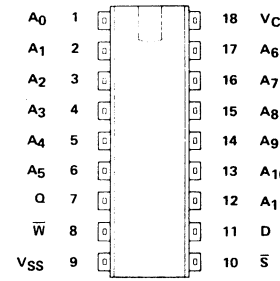
	ACCESS TIME (MAX)	READ OR WRITE CYCLE (MIN)
TMS 4044-45/4046-45	450 ns	450 ns
TMS 4044-30/4046-30	300 ns	300 ns
TMS 4044-25/4046-25	250 ns	250 ns
TMS 4044-20/4046-20	200 ns	200 ns
TMS 4044-15/4046-15	150 ns	150 ns

- All Inputs and Outputs Fully TTL-Compatible
- Common I/O Capability
- Output Interface
  3-State Outputs and Chip Select Control for OR-Tie Capability
  Fan-Out to 1 Series 74 or 74S TTL Load
- Power Dissipation

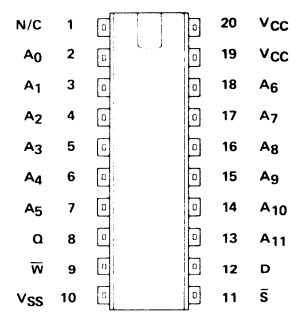
	TYPICAL	MAX
TMS 4044/46-25, -30, -45	250 mW	495 mW
TMS 4044/46-20, -15	400 mW	649 mW

- 400 mV Guaranteed d.c. Noise Immunity with Standard TTL Loads – No Pull-Up Resistors Required

TMS 4044
18-PIN CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGES
(TOP VIEW)



TMS 4046
20-PIN CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGES
(TOP VIEW)



PIN NAMES	
A_0-A_{11}	Addresses
D	Data In
Q	Data Out
$\overline{S}$	Chip Select
V_{CC}	+5 V Supply
V_{CC1}	+5 V Supply (array only)
V_{CC2}	+5 V Supply (periphery only)
V_{SS}	Ground
$\overline{W}$	Write Enable

description

This series of static random-access memories is organized as 4096 words of 1 bit. Static design results in reduced overhead costs by elimination of refresh-clocking circuitry and by simplification of timing requirements. Because this series is fully static, chip select may be tied low to further simplify system timing. Output data is always available during a read cycle.

All inputs and outputs are fully compatible with Series 74 or 74S TTL. No pull-up resistors are required. The TMS 4044/4046 series is manufactured using TI's reliable N-channel silicon-gate technology to optimize the cost/performance relationship. The single 5-volt power supply is also used to retain data in a reduced power standby mode. For the TMS 4046, V_{CC2} powers only the periphery circuitry. Consequently it is not required to maintain data during standby operation.

STANDBY OPERATION
(TYPICAL SUPPLY VALUES)

DEVICE	SUPPLY	OPERATING	STANDBY
TMS 4044	V_{CC}	+5 V	+2.4 V
TMS 4046	V_{CC1}	+5 V	+2.4 V
	V_{CC2}	+5 V	0 V

The TMS 4044 series and the TMS 4046 series are offered in 18-pin and 20-pin respectively dual-in-line ceramic (JL suffix) and plastic (NL suffix) packages designed for insertion in mounting-hole rows on 300-mil centers. The series is guaranteed for operation from 0°C to 70°C.

operation

addresses (A0-A11)
The twelve address inputs select one of the 4096 storage locations in the RAM. The address inputs must be stable for the duration of a write cycle. The address inputs can be driven directly from standard Series 54/74 TTL with no external pull-up resistors.

chip select ($\overline{S}$)
The chip-select terminal, which can be driven directly from standard TTL circuits, affects the data-in and data-out terminals. When chip select is a logic low, both terminals are enabled. When chip select is a logic high, data-in is inhibited and data-out is in the floating or high-impedance state.

write enable ($\overline{W}$)
The read or write mode is selected through the write enable terminal. A logic high selects the read mode; a logic low selects the write mode. $\overline{W}$ must be a logic high when changing addresses to prevent erroneously writing data into a memory location. The $\overline{W}$ input can be driven directly from standard TTL circuits.

data-in (D)
Data can be written into a selected device when the write enable input is a logic low. The data-in terminal can be driven directly from standard TTL circuits.

data-out (Q)
The three-state output buffer provides direct TTL compatibility with a fan-out of one Series 74 TTL gate or one Series 74S TTL gate. The output is in the high-impedance state when chip select ($\overline{S}$) is high or whenever a write operation is being performed, facilitating device operation in common I/O systems. Data-out is the same polarity as data-in.

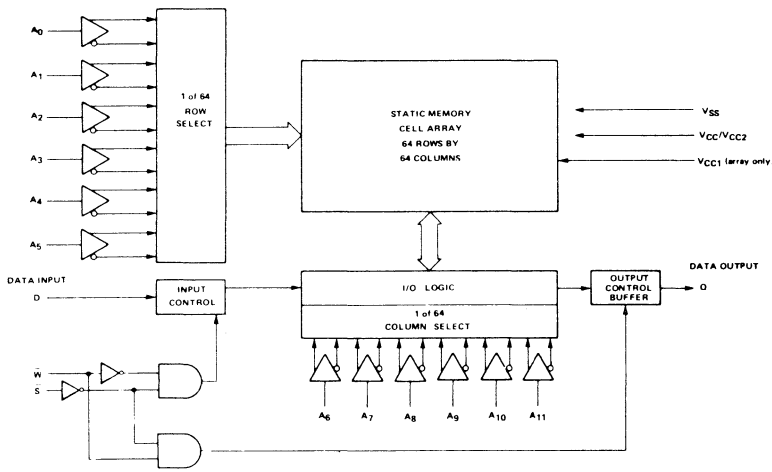
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{CC} (see Note 1) . . . . . −0.5 to 7 V
Input voltage (any input) (see Note 1) . . . . . −0.5 to 7 V
Continuous power dissipation . . . . . 1 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 150°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values are with respect to the ground terminal.

functional block diagram



$\overline{S}$	$\overline{W}$	D	Q	MODE
H	X	X	HI-Z	Not Selected
L	L	L	HI-Z	Write "0"
L	L	H	HI-Z	Write "1"
L	H	X	DATA OUT	Read

recommended operating conditions

PARAMETER		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	Operating	4.5	5	5.5	V
	Standby	2.4	5	5.5	
Supply voltage (array only), V_{CC1}	Operating	4.5	5	5.5	V
	Standby	2.4	5	5.5	
Supply voltage (periphery only), V_{CC2}	Operating	4.5	5	5.5	V
	Standby	0	0	5.5	
Supply voltage, V_{SS}			0		V
High-level input voltage, V_{IH}		2.0		5.5	V
Low-level input voltage, V_{IL}		−0.5		0.8	V
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended operating free air temperature ranges (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{OH}	High level voltage	I_{OH} = −200 μA	V_{CC} = 4.5 V		2.4			V
V_{OL}	Low level voltage	I_{OL} = 2 mA	V_{CC} = 4.5 V				0.4	V
I_I	Input current	V_I 0 to 5.5 V					10	μA
I_{OZH}	Off-state output current, high level voltage applied	$\overline{S}$ @ 2.0 V or $\overline{W}$ at 0.8 V	V_O = 5.5 V				10	μA
I_{OZL}	Off-state output current, low level voltage applied	$\overline{S}$ at 2.0 V or $\overline{W}$ at 0.8 V	V_O = 0.4 V				10	μA
I_{CC}	Supply current from V_{CC}	V_{CC} = 5.5 V I_O = 0 mA (worst case dynamic conditions)	T_A = 0°C	4044/46-45, -30, -25		50	90	mA
				4044/46-20, -15		80	118	mA
I_{CC1}	Supply current from V_{CC1} (array only)	V_{CC1} = 5.5 V I_O = 0 mA T_A = 70°C				5		mA
I_{CC2}	Supply current from V_{CC2} (periphery only)	V_{CC2} = 5.5 V I_O = 0 mA T_A = 0°C		4044/46-45, -30, -25		45		mA
				4044/46-20, -15		75		mA
C_i	Input capacitance	V_I = 0 V f = 1 MHz					8	pF
C_o	Output capacitance	V_O = 0 V f = 1 MHz					12	pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

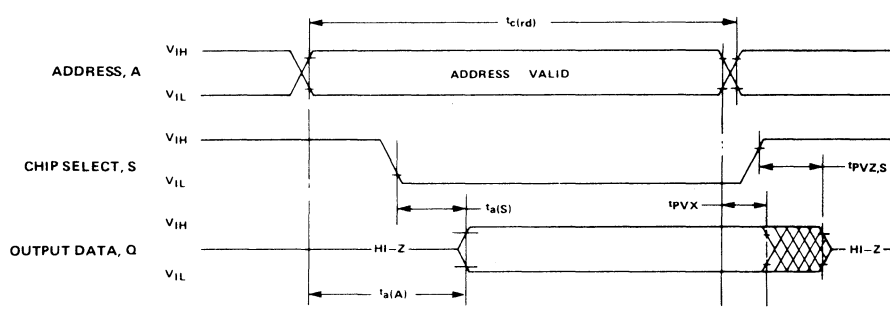
timing requirements over recommended supply voltage range and operating free-air temperature range

PARAMETER		TMS 4044-15 TMS 4046-15		TMS 4044-20 TMS 4046-20		TMS 4044-25 TMS 4046-25		TMS 4044-30 TMS 4046-30		TMS 4044-45 TMS 4046-45		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time	150		200		250		300		450		ns
$t_{c(wr)}$	Write cycle time	150		200		250		300		450		ns
$t_{c(RW)}$	Read, modify-write cycle time	250		320		370		450		650		ns
$t_{w(W)}$	Write pulse width	80		100		100		150		200		ns
$t_{su(A)}$	Address set up time	0		0		0		0		0		ns
$t_{su(S)}$	Chip select set up time	60		100		100		150		200		ns
$t_{su(D)}$	Data set up time	60		100		100		150		200		ns
$t_{h(D)}$	Data hold time	0		0		0		0		0		ns
$t_{h(A)}$	Address hold time	20		20		20		0		0		ns

switching characteristics over recommended voltage range, T_A = 0°C to 70°C,
1 series 74 TTL load, C_L = 100 pF

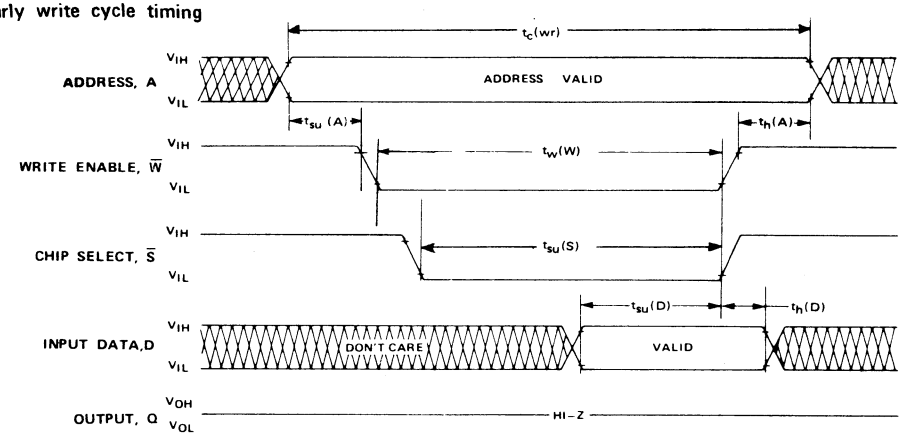
PARAMETER		TMS 4044-15 TMS 4046-15			TMS 4044-20 TMS 4046-20		TMS 4044-25 TMS 4046-25		TMS 4044-30 TMS 4046-30		TMS 4044-45 TMS 4046-45		UNIT
		MIN	NOM	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address			150		200		250		300		450	ns
$t_{a(S)}$	Access time from chip select low			70		70		70		100		100	ns
$t_{a(W)}$	Access time from write enable high			70		70		70		100		100	ns
t_{PVX}	Output data valid after address change	10			10		10		10		10		ns
$t_{PVZ,S}$	Output disable time after chip select high			50		60		60		80		100	ns
$t_{PVZ,W}$	Output disable time after write enable low			50		60		60		80		100	ns

read cycle timing**

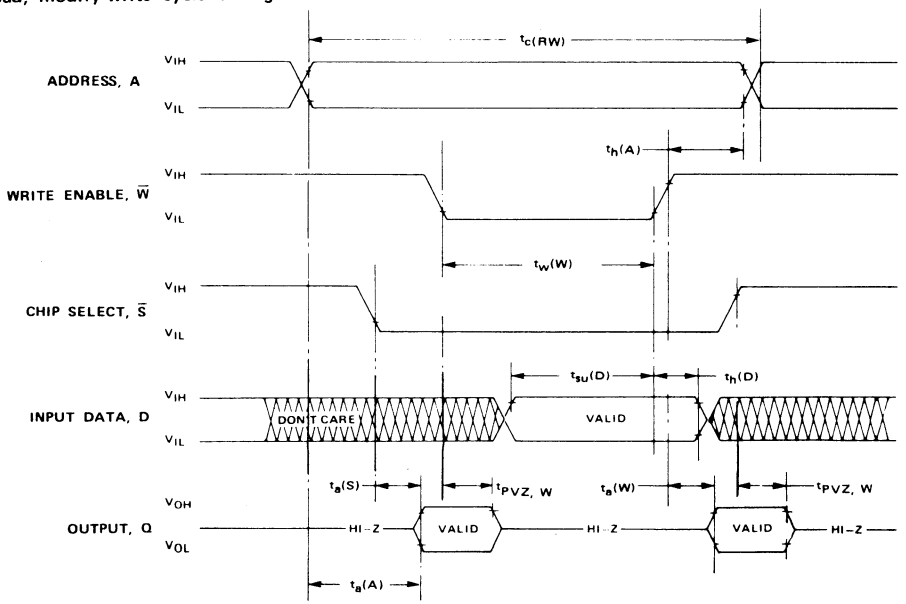


** Write enable is high for a read cycle.

early write cycle timing



read, modify-write cycle timing



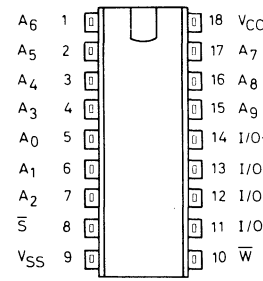
TMS 4045, -45,-30,-25,-20,-15JL, NL; TMS 4047,-45,-30,-25,-20,-15JL, NL
1024 WORD BY 4-BIT STATIC RANDOM-ACCESS MEMORIES

- 1024 x 4 Organization
- Single 10% Tolerance +5 V Supply
- High Density 300-mil 18- and 20-Pin Packages
- Fully Static Operation (No Clocks, No Refresh, No Timing Strobe)
- 4 Performance Ranges:

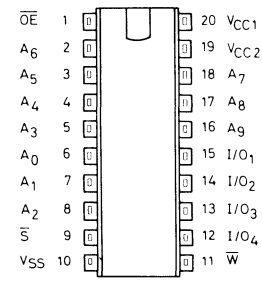
	ACCESS TIME (MAX)	READ OR WRITE CYCLE (MIN)
TMS 4045-45/4047-45	450 ns	450 ns
TMS 4045-30/4047-30	300 ns	300 ns
TMS 4045-25/4047-25	250 ns	250 ns
TMS 4045-20/4047-20	200 ns	200 ns
TMS 4045-15/4047-15	150 ns	150 ns

- 400 mV Guaranteed d.c. Noise Immunity With Standard TTL Loads – No Pull-Up Resistors Required
- Common I/O With Three-State Outputs and Chip Select Control for OR-Tie Capability
- Fan-Out to 1 Series 74 or 74S TTL Load – No Pull-Up Resistors Required
- Power Dissipation for TMS 4045-20/4047-20 Less Than 400 mW (Typical)
- Standby Power Dissipation Less Than:
  12 mW (Typical) for TMS 4047-20
  192 mW (Typical) for TMS 4045-20

TMS 4045
18-PIN CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGES
(TOP VIEW)



TMS 4047
20-PIN CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGES
(TOP VIEW)



description

This series of static random-access memories is organized as 1024 words of 4 bits. Static design results in reduced overhead costs by elimination of refresh-clocking circuitry and by simplification of timing requirements. Because this series is fully static, chip select may be tied low to further simplify system timing. Output data is always available during a read cycle.

All inputs and outputs are fully compatible with Serie 74 or 74S TTL. No pull-up resistors are required.
The TMS 4045/4047 series is manufactured using TI's reliable N-channel silicon-gate technology to optimize the cost/performance relationship. The single 5-volt power supply is also used to retain data in a reduced power standby mode. For the TMS 4047, V_{CC2} powers only the periphery circuitry. Consequently it is not required to maintain data during standby operation.

PIN NAMES	
A0 - A9	Addresses
I/O1 - I/O4	Data input/output
$\overline{OE}$	Output Enable
$\overline{S}$	Chip Select
V_{CC}	+5 V Supply
V_{CC1}	+5 V Supply (array only
V_{CC2}	+5 V Supply (periphery only)
V_{SS}	Ground
$\overline{W}$	Write Enable

PRELIMINARY DATA SHEET:
Supplementary data may be published at a later date.

STANDBY OPERATION
(TYPICAL SUPPLY VALUES)

DEVICE	SUPPLY	OPERATING	STANDBY
TMS 4045	V_{CC}	+5 V	+2.4 V
TMS 4047	V_{CC1} V_{CC2}	+5 V +5 V	+2.4 V 0 V

The TMS 4045 series and the TMS 4047 series are offered in 18-pin and 20-pin respectively dual-in-line ceramic (JL suffix) and plastic (NL suffix) packages designed for insertion in mounting-hole rows on 300-mil centers. The series is designed for operation from 0 °C to 70 °C.

operation

addresses (A0 - A9)

The ten address inputs select one of the 1024 4-bit words stored in the RAM. The address-inputs must be stable for the duration of a write cycle. The address inputs can be driven directly from standard Series 54/74 TTL with no external pull-up resistors.

output enable ($\overline{OE}$)

The output enable terminal, which can be driven directly from standard TTL circuits, affects only the data-in/Data-out terminals. When output enable is a logic high, the I/O terminals are disabled to the high-impedance state. Output enable provides greater output control flexibility, simplifying data bus design.

chip select ($\overline{S}$)

The chip-select terminal, which can be driven directly from standard TTL circuits, affects the data-in/data-out terminals. When chip select and output enable are a logic low, the I/O terminals are enabled. When chip select is a logic high, the I/O terminals are in the floating or high-impedance state and the input is inhibited.

write enable ($\overline{W}$)

The read or write mode is selected through the write enable terminal. A logic high selects the read mode; a logic low selects the write mode. The W input can be driven directly from standard TTL circuits.

data-in/data-out (I/O_1 - I/O_4)

Data can be written into a selected device when the write enable input is a logic low. The I/O terminal can be driven directly from standard tTL circuits. The three-state output buffer provides direct TTL compatibility with a fan-out of one Series 74 TTL gate or one Series 74S TTL gate. The I/O terminals are in the high-impedance state when chip select ($\overline{S}$) is high or whenever a write operation is being performed. Data-out is the same polarity as data-in.

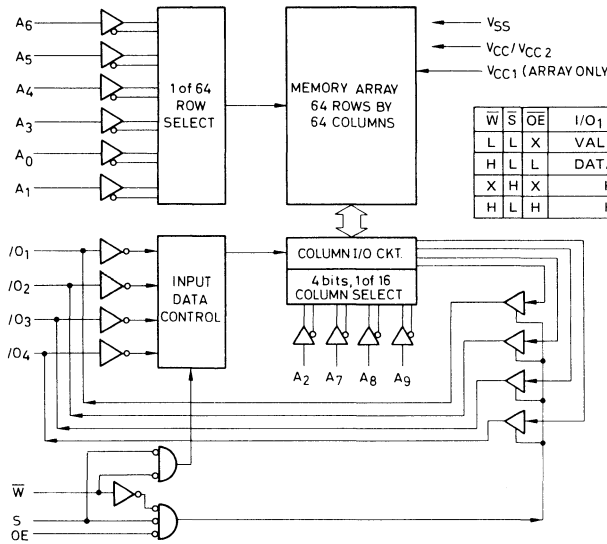
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{CC} (see Note 1) . . . . . −0.5 to 7 V
Input voltage (any input) (see Note 1) . . . . . −0.5 to 7 V
Continuous power dissipation . . . . . 1 W
Operating free-air temperature range . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −55 °C to 150 °C

NOTE 1: Voltage values are with respect to the ground terminal.

* Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

functional block diagram



$\overline{W}$	S	$\overline{OE}$	$I/O_1 - I/O_4$	
L	L	X	VALID DATA	WRITE
H	L	L	DATA OUTPUT	READ
X	H	X	HI-Z	DEVICE DISABLED
H	L	H	HI-Z	OUTPUT DISABLED

recommended operating conditions

PARAMETER		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	Operating	4.5	5	5.5	V
	Standby	2.4	5	5.5	
Supply voltage (array only), V_{CC1}	Operating	4.5	5	5.5	V
	Standby	2.4	5	5.5	
Supply voltage, V_{SS}	Operating	4.5	5	5.5	V
	Standby	0	0	5.5	
Supply voltage, V_{SS}			0		V
High-level input voltage, V_{IH}		2.0		V_{CC}	V
Low-level input voltage, V_{IL}		0.4		0.8	V
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP*	MAX	UNIT
V_{OH}	High level voltage	I_{OH} = −200 μA	V_{CC} = 4.75 V		2.4			V
			V_{CC} = 4.5 V		2.2			
V_{OL}	Low level voltage	I_{OL} = 2 mA	V_{CC} = 4.5 V				0.4	V
I_I	Input current	V_I 0 to 5.5 V					10	μA
I_{OZH}	Off-state output current, high level voltage applied	$\overline{S}$ or $\overline{OE}$ @ 2.0 V or $\overline{W}$ at 0.8 V	V_O = 4 V				10	μA
I_{OZL}	Off-state output current, low level voltage applied	$\overline{S}$ or $\overline{OE}$ at 2.0 V or $\overline{W}$ at 0.8 V	V_O = 0.4 V				10	μA
I_{CC}	Supply current from V_{CC}	V_{CC} = 5.5 V, I_O = 0 mA (worst case)	T_A = 0 °C	4045/47 -45, -30		75	100	mA
				4045/47 -20, -15		TBD		mA
I_{CC1}	Supply current from V_{CC1} (array only)	V_{CC1} = 5.5 V, I_O = 0 mA, T_A = 70 °C				5		mA
I_{CC2}	Supply current from V_{CC2} (periphery only)	V_{CC2} = 5.5 V, I_O = 0 mA, T_A = 0 °C				70		mA
C_i	Input capacitance	V_I = 0 V, f = 1 MHz					8	pF
C_O	Output capacitance	V_O = 0 V, f = 1 MHz					12	pF

All typical values are at V_{CC} = 5 V, T_A = 25 °C

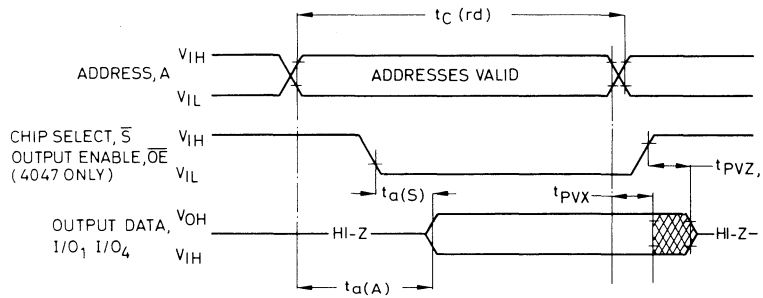
timing requirements over recommended supply voltage range and operating free-air temperature range

PARAMETER		TMS 4045-15 TMS 4047-15		TMS 4045-20 TMS 4047-20		TMS 4045-25 TMS 4047-25		TMS 4045-30 TMS 4047-30		TMS 4045-45 TMS 4047-45		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time		150		200	250			300		450	ns
$t_{c(wr)}$	Write cycle time		150		200	250			300		450	ns
$t_{w(W)}$	Write pulse width	TBD		100		100		150		200		ns
$t_{su(A)}$	Address set up time	0		0		0		0		0		ns
$t_{su(S)}$	Chip select set up time	TBD		100		100		150		200		ns
$t_{su(D)}$	Data set up time	TBD		100		100		150		200		ns
$t_{h(D)}$	Data hold time	0		0		0		0		0		ns
$t_{h(A)}$	Address hold time	TBD		20		20		0		0		ns

switching characteristics over recommended voltage range, T_A = 0 °C to 70 °C, 1 serie 74 TTL load, C_L = 50 pF

PARAMETER		TMS 4045-15 TMS 4047-15		TMS 4045-20 TMS 4047-20		TMS 4045-25 TMS 4047-25		TMS 4045-30 TMS 4047-30		TMS 4045-45 TMS 4047-45		UNIT
		NOM	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address		150		200		250		300		450	ns
$t_{a(S)}$	Access time from chip select (or output enable low)		TBD		TBD		100		100		120	ns
$t_{a(W)}$	Access time from write enable high		TBD		TBD		100		100		120	ns
t_{PVX}	Output data valid after address change	10		10		10		10		10		ns
$t_{PVZ,S}$	Output disable time after chip select (or output enable) high	40			40		40		80		100	ns
$t_{PVZ,W}$	Output disable time after write enable high	40			40		40		80		100	ns

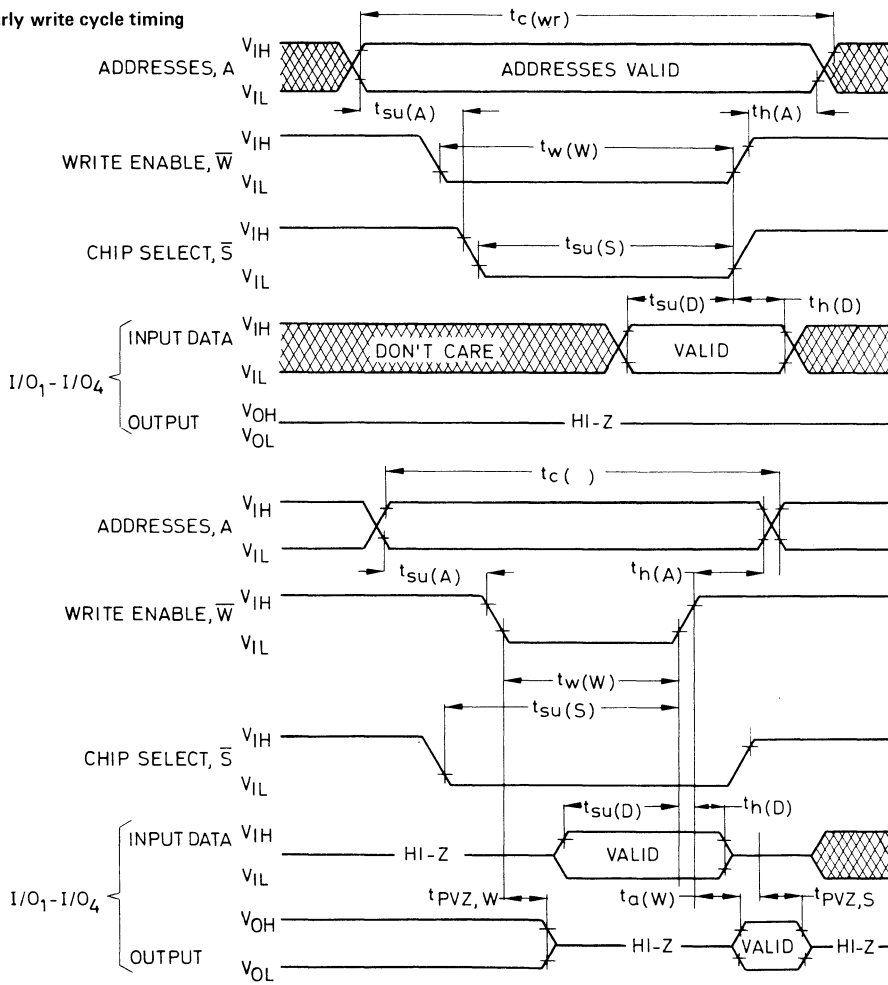
read cycle timing**



** Write enable is high for a read cycle

All timing reference points are 10% and 90%.
Input rise and fall times 10 ns.

early write cycle timing



applications data

Early write cycle avoids I/O conflicts by controlling the write time with $\overline{S}$. In the diagram above, the write operation will be controlled by the leading edge of $\overline{S}$ not $\overline{W}$. Data can only be written into the array when both $\overline{S}$ and $\overline{W}$ are logic low. Either $\overline{S}$ or $\overline{W}$ being logic high inhibits the write operation and data stored will not be affected by the address. To prevent erroneous data being written into the array care must be taken to ensure that the addresses are stable during the entire write cycle defined as $t_{su(A)}$, $t_{w(W)}$ and $t_{h(A)}$.

TMS 4027-15, TMS 4027-20, TMS 4027-25 JL, NL
4096 BIT DYNAMIC RANDOM-ACCESS MEMORY

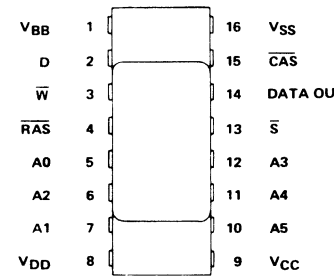
MARCH 1977

- 4096 X 1 Organization
- Industry Standard 16-Pin 300-Mil Package Configuration
- 10% Tolerance on All Supplies
- All Inputs Including Clocks TTL Compatible
- Three-State Fully TTL-Compatible Output Latched and Valid Into Next Cycle
- 3 Performance Ranges:

	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	READ, MODIFY-WRITE† CYCLE (MIN)
TMS 4027-15	150 ns	100 ns	320 ns	330 ns
TMS 4027-20	200 ns	135 ns	375 ns	420 ns
TMS 4027-25	250 ns	165 ns	375 ns	480 ns

- Page-Mode Operation for Faster Access Time
- Low-Power Dissipation
  - Operating 460 mW (max)
  - Standby 27 mW (max)
- 1-T Cell Design, N-Channel Silicon-Gate Technology

16-PIN CERAMIC
DUAL-IN-LINE PACKAGE
(TOP VIEW)



PIN NAMES

A0–A5	Address Inputs
$\overline{CAS}$	Column address strobe
D	Data input
DATA OUT	Data output
$\overline{RAS}$	Row address strobe
$\overline{S}$	Chip select
$\overline{W}$	Write enable
V_{BB}	−5 V power supply
V_{CC}	+5 V power supply
V_{DD}	+12 V power supply
V_{SS}	0 V ground

description

The TMS 4027 JL series is composed of monolithic high-speed dynamic 4096-bit MOS random-access memories, organized as 4096 one-bit words, employing single-transistor storage cells and N-channel silicon-gate technology.

All inputs and outputs are compatible with Series 74 TTL circuits including clocks: Row Address Strobe ($\overline{RAS}$) or ($\overline{R}$) and Column Address Strobe ($\overline{CAS}$) or ($\overline{C}$). All address lines (A0 through A5) and data-in (D) are latched on chip to simplify system design. Data out is latched and available until the negative edge of $\overline{CAS}$ in the next memory cycle returns the output to the high-impedance state.

Typical power dissipation is less than 300 milliwatts active and 14 milliwatts during standby (V_{CC} is not required during standby operation). To retain data, only 20 milliwatts average power is required which includes the power consumed to refresh the contents of the memory.

The TMS 4027 JL, NL series is offered in a 16-pin dual-in-line package and is guaranteed for operation from 0°C to 70°C. Packages are designed for insertion in mounting-hole rows on 300-mil centers.

operation

address (A0 through A5)

Twelve address bits are required to decode 1 of 4096 storage cell locations. Six row-address bits are set up on pins A0 through A5 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the six column-address bits are set up on

† The term "read-write cycle" is sometimes used as an alternative title to "read-modify-write cycle".

pins A0 through A5 and latched onto the chip by the column-address strobe ($\overline{CAS}$). $\overline{RAS}$ activates the sense amplifiers as well as the row decoder, and $\overline{CAS}$ activates the column decoder and the input and output buffers.

chip select ($\overline{S}$)

When the chip select ($\overline{S}$) input is high, the column decode and the input and output buffers are disabled. However, the row decode is unaffected by chip select so that row addresses are latched and refresh can continue to take place.

write enable ($\overline{W}$)

The read or write mode is selected through the write enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data-out will contain the data written into the selected cell.

data-in (D)

Data is written during a write or read modify-write cycle. The latter falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. This latch can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read-modify write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data-out

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan-out of two Series 74 TTL loads. Data-out is the same polarity as data-in. The output goes into the high-impedance state after the negative transition of $\overline{CAS}$. The output becomes valid after the access time has elapsed, and it remains valid into the next memory cycle before $\overline{CAS}$ going low returns it to a high-impedance state.

refresh

A refresh operation must be performed at least every two milliseconds to retain data. Since the output buffer is in the high-impedance state unless $\overline{CAS}$ is applied, the $\overline{RAS}$ only refresh sequence avoids any output during refresh. Strobing each of the 64 row addresses (A0 through A5) with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ remains high (inactive) for this refresh sequence, thus conserving power.

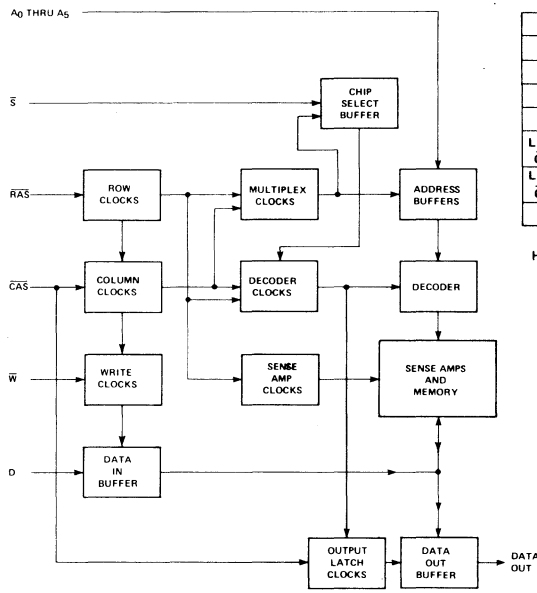
page mode

Page mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the chip. Thus, the time required to setup and strobe the row addresses is eliminated. To extend beyond the 64 column locations on a single RAM, apply the row address and $\overline{RAS}$ to multiple 4K RAMs, then decode chip select to select the proper RAM. (A RAM need not be selected during the first page mode cycles to have the row address latched on chip.)

power-up

No particular power-up sequence is required; however, to assure compliance with the "absolute maximum ratings", it is good engineering practice to apply V_{BB} first (and remove V_{BB} last in power-down). This prevents any forward junction bias conditions that could arise if other supplies are applied first. After power-up, one memory cycle must be performed to achieve proper device operation.

functional block diagram



W	S	RAS	CAS	OUTPUT	MODE
H	H	L	L	Hi-Z	Not selected
L	H	L	L	Hi-Z	No write will occur
X	X	L	H	Hi-Z	RAS only cycle
X	X	H	L	Hi-Z	CAS only cycle
L Before CASL	L	L	L	Input data	Early write
L After CASL	L	L	L	Valid data	Write or read/ write cycle
H	L	L	L	Data out	Read

H=High; L=Low; X-Don't Care; Hi-Z=High impedance.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{CC} (see Note 1) . . . . . −0.3 to 20 V
Supply voltage, V_{DD} (see Note 1) . . . . . −0.3 to 20 V
Supply voltage, V_{SS} (see Note 1) . . . . . −0.3 to 20 V
All input voltages (see Note 1) . . . . . −0.3 to 20 V
Output voltage (operating, with respect to V_{SS}) . . . . . −2 to 10 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 150°C

NOTE 1: Under absolute maximum ratings, voltage values are with respect to the most-negative supply voltage, V_{BB} (substrate), unless otherwise noted. Throughout the remainder of this data sheet, voltage values are with respect to V_{SS}.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{BB}	−4.5	−5	−5.5	V
Supply voltage, V_{CC}	4.5	5	5.5	V
Supply voltage, V_{DD}	10.8	12	13.2	V
Supply voltage, V_{SS}		0		V
High-level input voltage, except RAS, CAS, and WRITE, V_{IH}	2.2	3.5	7.0	V
High-level input voltage, RAS, CAS, and WRITE, $V_{IH(R)}$	2.4	3.5	7.0	V
Low-level input voltage, V_{IL}	−1.0	0	0.8	V
Refresh time, $t_{refresh}$			2	ms
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 3.2 mA, C_L = 50 pF			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 10 V, All other pins = 0 V except V_{BB} = −5 V			10	μA
I_O	Output current (leakage)	V_O = 0 to 10 V, $\overline{RAS}$ and $\overline{CAS}$ high, Output Disabled, after 1 memory cycle			10	μA
$I_{BB(av)}$	Average operating current	Minimum cycle time		90	150	μA
$I_{CC(av)}$*	during read or write					
$I_{DD(av)}$	cycle	Minimum cycle time		25	35	mA
I_{DD}	Standby current, $\overline{RAS}$ and $\overline{CAS}$ high	After 1 memory cycle		0.85	2	mA
$I_{DD(av)}$	Average refresh current, $\overline{RAS}$ cycling, $\overline{CAS}$ high	Minimum cycle time		15	25	mA

*V_{CC} is applied only to the output buffer, so I_{CC} depends on output loading.

capacitance over recommended supply voltage range and operating free-air temperature range f = 1 MHz

PARAMETER		TYP†	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs	4	5	pF
$C_{i(D)}$	Input capacitance, data input	4	5	pF
$C_{i(RC)}$	Input capacitance, strobe inputs	8	10	pF
$C_{i(W)}$	Input capacitance, write enable input	8	10	pF
C_o	Output capacitance	5	7	pF

†All typical values are at T_A = 25°C and nominal supply voltages.

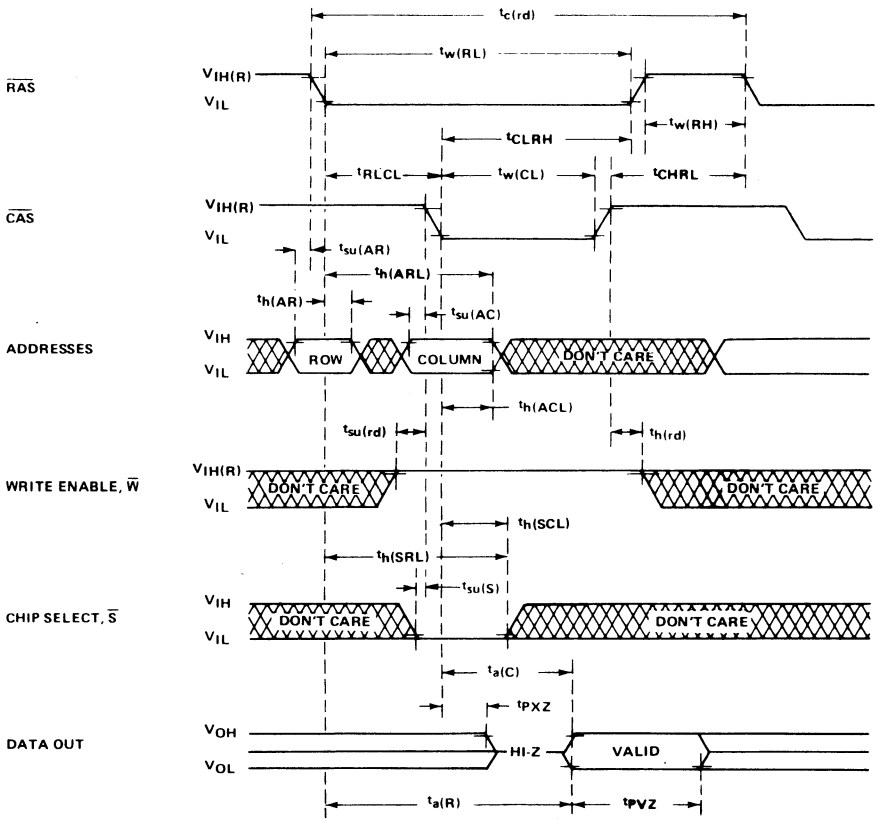
switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	TMS 4027-15		TMS 4027-20		TMS 4027-25		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from column address strobe	C_L = 50 pF, $t_{r(C)}$ and $t_{r(R)}$ = 5 ns,		100		135		165	ns
$t_{a(R)}$	Access time from row address strobe	$t_{RL,CL}$ = MAX, Load = 2 Series 74 TTL gates		150		200		250	ns
t_{PVZ}	Output valid time	C_L = 50 pF, Load = 2 Series 74 TTL gates	10		10		10		μs
t_{PXZ}	Output disable time		0	40	0	50	0	60	ns

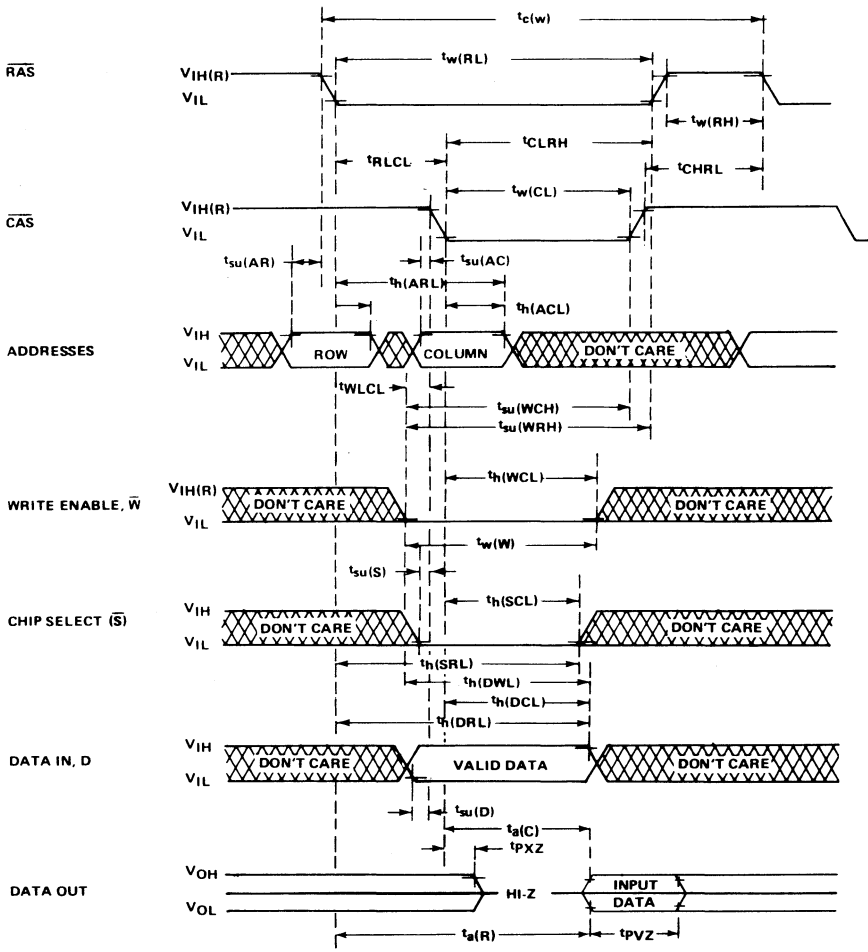
timing requirements over recommended supply voltage range and operating free-air temperature range

PARAMETER		TMS 4027-15		TMS 4027-20		TMS 4027-25		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time	320		375		375		ns
$t_{c(W)}$	Write cycle time	320		375		375		ns
$t_{c(RW)}$	Read, modify-write cycle time	330		420		480		ns
$t_{w(CH)}$	Pulse width, column address strobe high (precharge time)	60		80		110		ns
$t_{w(CL)}$	Pulse width, column address strobe low	100		135		165		ns
$t_{w(RH)}$	Pulse width, row address strobe high (precharge time)	100		120		120		ns
$t_{w(RL)}$	Pulse width, row address strobe low	150	10,000	200	10,000	250	10,000	ns
$t_{w(W)}$	Write pulse width	45		55		75		ns
t_T	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	3	35	3	50	3	50	ns
$t_{su(AC)}$	Column address setup time	−10		−10		−10		ns
$t_{su(AR)}$	Row address setup time	0		0		0		ns
$t_{su(D)}$	Data setup time	0		0		0		ns
$t_{su(S)}$	Chip select setup time	−10		−10		−10		ns
$t_{su(rd)}$	Read command setup time	0		0		0		ns
$t_{su(WCH)}$	Write command setup time before $\overline{CAS}$ high	50		70		85		ns
$t_{su(WRH)}$	Write command setup time before $\overline{RAS}$ high	50		70		85		ns
$t_{h(ACL)}$	Column address hold time after $\overline{CAS}$ low	45		55		75		ns
$t_{h(AR)}$	Row address hold time	20		25		35		ns
$t_{h(ARL)}$	Column address hold time after $\overline{RAS}$ low	95		120		160		ns
$t_{h(DCL)}$	Data hold time after $\overline{CAS}$ low	45		55		75		ns
$t_{h(DRL)}$	Data hold time after $\overline{RAS}$ low	95		120		160		ns
$t_{h(DWL)}$	Data hold time after $\overline{W}$ low	45		55		75		ns
$t_{h(rd)}$	Read command hold time	0		0		0		ns
$t_{h(SCL)}$	Chip select hold time after $\overline{CAS}$ low	45		55		75		ns
$t_{h(SRL)}$	Chip select hold time after $\overline{RAS}$ low	95		120		160		ns
$t_{h(WCL)}$	Write command hold time after $\overline{CAS}$ low	45		55		75		ns
t_{CHRL}	Delay time, column address strobe high to row address strobe low	0		0		0		ns
t_{CLRH}	Delay time, column address strobe low to row address strobe high	100		135		165		ns
t_{CLWL}	Delay time, column address strobe low to $\overline{W}$ low (read, modify-write cycle only)	60		80		90		ns
t_{REF}	Refresh period		2		2		2	ms
t_{RLCL}	Delay time, row address strobe low to column address strobe low (maximum value specified only to guarantee access time)	20	50	25	65	35	85	ns
t_{RLWL}	Delay time, row address strobe low to $\overline{W}$ low (read, modify-write cycle only)	110		145		175		ns
t_{WLCL}	Delay time, $\overline{W}$ low to column address strobe low (early write cycle)	0		0		0		ns

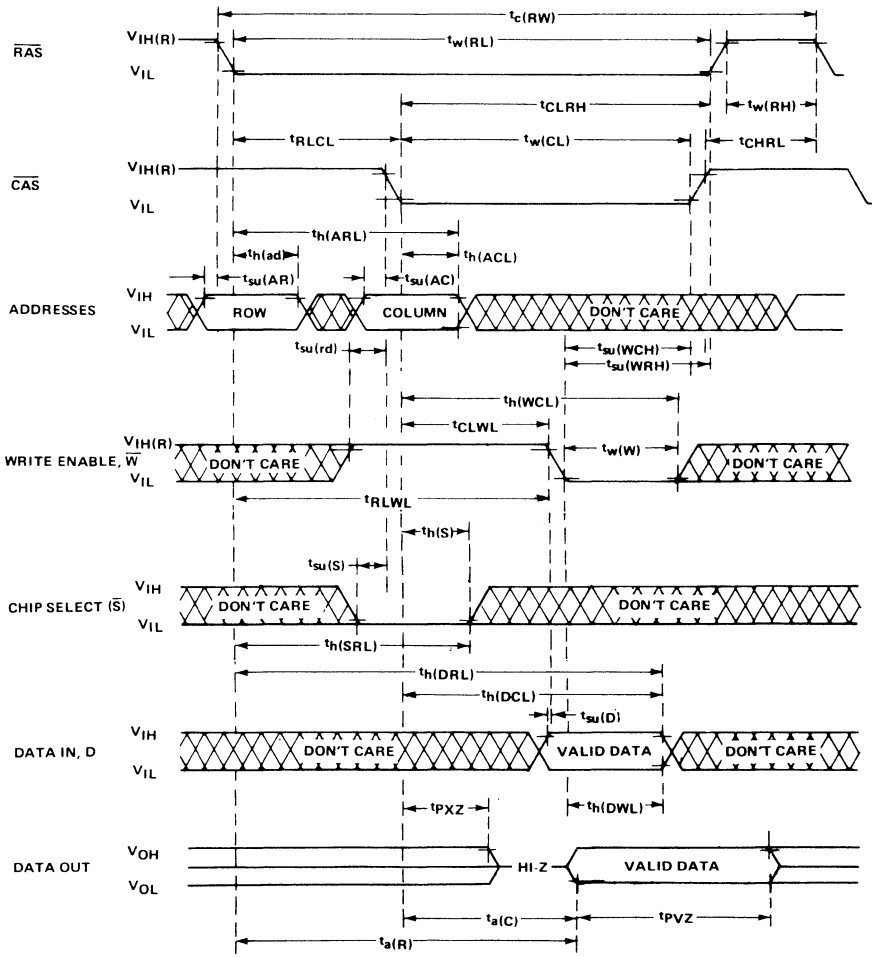
read cycle timing



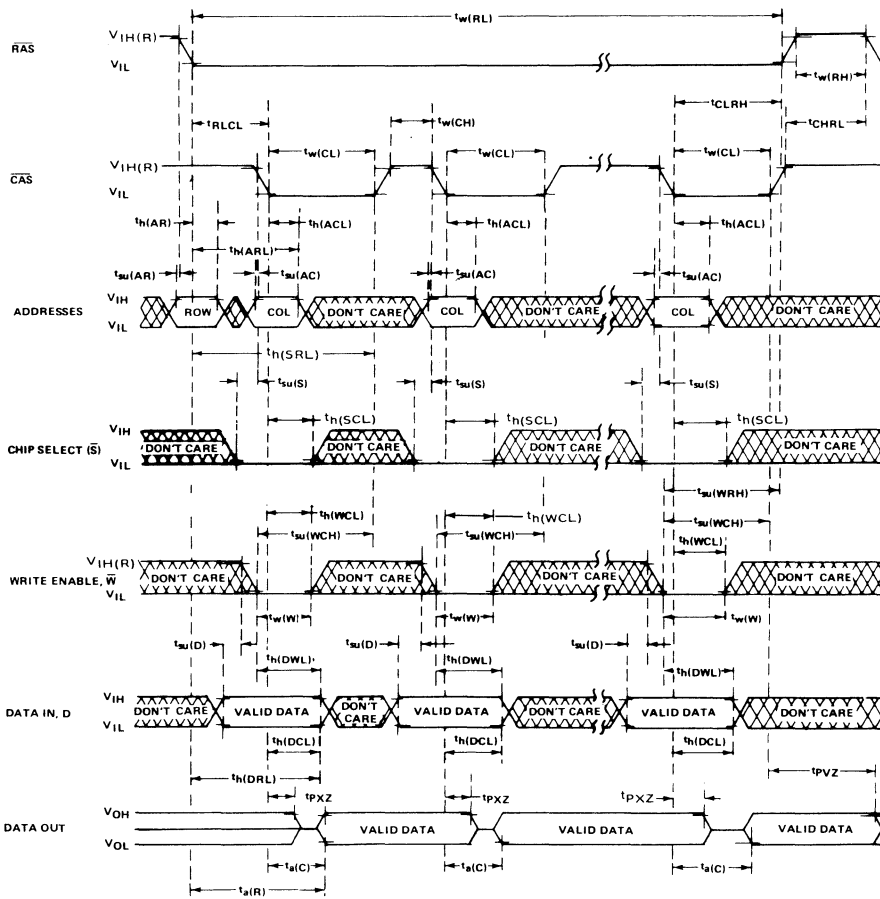
early write cycle timing



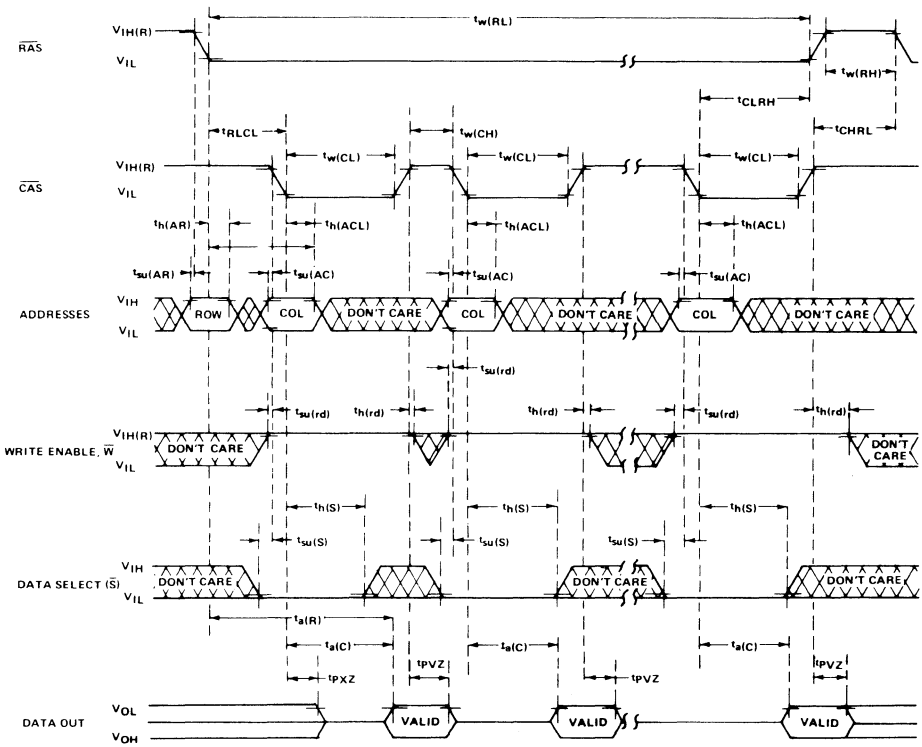
read-write/read-modify-write cycle timing



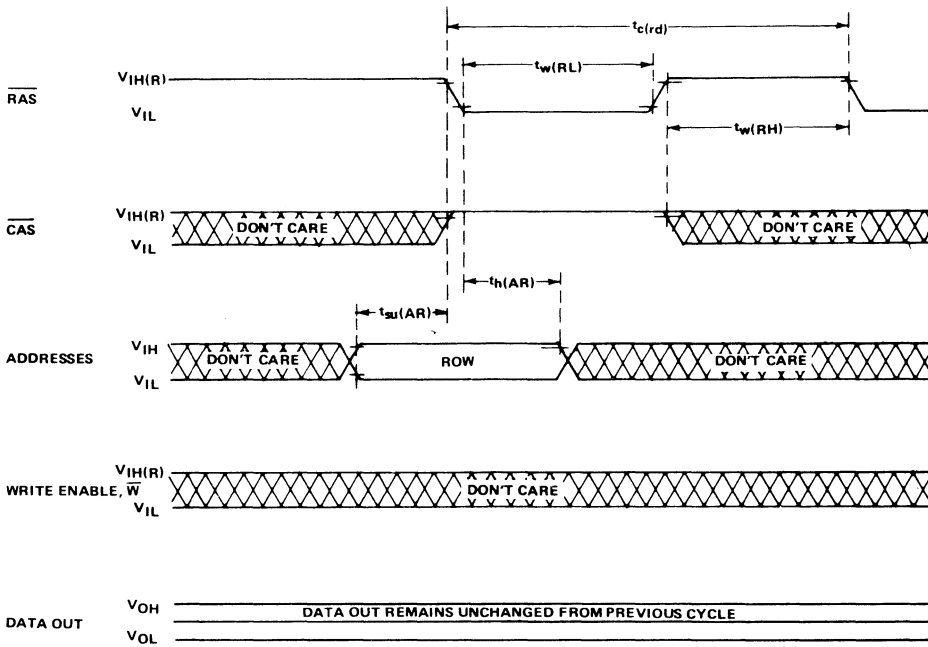
page mode write cycle timing



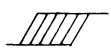
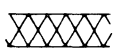
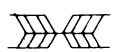
page mode read cycle timing



$\overline{RAS}$ only refresh timing



timing diagram conventions

TIMING DIAGRAM SYMBOL	MEANING: INPUT FORCING FUNCTIONS	MEANING: OUTPUT RESPONSE FUNCTIONS
———	Must be steady high or low	Will be steady high or low
	High-to-low changes permitted	Will be changing from high to low sometime during designated interval
	Low-to-high changes permitted	Will be changing from low to high sometime during designated interval
	Don't Care	State unknown or changing
	(Does not apply)	Center line is high-impedance off-state

TMS 4051 JL, NL; TMS 4051-1 JL, NL
4096-BIT DYNAMIC RANDOM-ACCESS MEMORIES

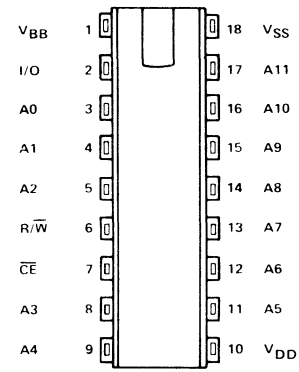
BULLETIN NO. DL-S 7512256, MAY 1975

- 4096 x 1 Organization
- 18-Pin 300-Mil Package Configuration
- Single Low-Capacitance TTL-Compatible Clock
- Multiplexed Data Input/Output
- 2 Performance Ranges:

	ACCESS TIME (MAX)	READ OR WRITE CYCLE (MIN)	READ, MODIFY WRITE CYCLE (MIN)
TMS 4051	300 ns	470 ns	730 ns
TMS 4051-1	250 ns	430 ns	660 ns

- Full TTL Compatibility on All Inputs (No Pull-up Resistors Needed Except with $\overline{CE}$)
- Registers for Addresses Provided on Chip
- Open-Drain Output Buffer
- Low-Power Dissipation
  - 460 mW Operating (Typical)
  - 60 mW Standby (Typical)
- N-Channel Silicon-Gate Technology

18-PIN CERAMIC AND PLASTIC DUAL-IN-LINE PACKAGES (TOP VIEW)



description

The TMS 4051 series is composed of high-speed dynamic 4096-bit MOS random-access memories, organized as 4096 one-bit words. N-channel silicon-gate technology is employed to optimize the speed/power/density trade-off. Two performance options are offered: 300 ns access for the TMS 4051 and 250 ns access for the TMS 4051-1. These options allow the system designer to more closely match the memory performance to the capability of the arithmetic processor.

The address, data input/output, and read/write inputs can be driven directly from Series 74 TTL circuits. A 200-mV noise margin is guaranteed in this configuration, which eliminates the need for specialized drivers. The chip-enable input is TTL-compatible and can interface with a Series 74 TTL circuit as long as a pull-up resistor to V_{CC} is employed in order to provide a high-level input voltage of 3 V minimum. The data input and output are multiplexed to facilitate compatibility with a common bus system. A 12-line address is available, which minimizes external control logic and optimizes system performance.

The typical power dissipation of these RAM's is 460 mW active and 60 mW standby. To retain data only 70 mW average power is required, which includes the power consumed to refresh the contents of the memory.

The TMS 4051 series is offered in both 18-pin ceramic (JL suffix) and plastic (NL suffix) dual-in-line packages. The series is guaranteed for operation from 0°C to 70°C. Packages are designed for insertion in mounting-hole rows on 300-mil centers.

operation

chip enable ($\overline{CE}$)

A single external clock input is required. All read, write, and read, modify write operations take place when the chip enable input is low. When the chip enable is high, the memory is in the low-power standby mode and is not selected. No read/write operations can take place during the standby mode because the chip is deselected and is automatically precharging. The $\overline{CE}$ input can be driven by a standard TTL circuit with a pull-up resistor.

operation (continued)

mode select (R/$\overline{W}$)

The read or write mode is selected through the read/write (R/$\overline{W}$) input. A logic high on the R/$\overline{W}$ input selects the read mode and a logic low selects the write mode. The read/write terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected and the data output is disabled when the write mode is selected.

address (A0–A11)

All addresses must be stable on or before the falling edge of the chip-enable pulse. All address inputs can be driven from standard TTL circuits without pull-up resistors. Address registers are provided on chip to reduce overhead and simplify system design.

data input/output (I/O)

Data input and output are multiplexed on a common input/output terminal, which is controlled by the R/$\overline{W}$ input. Data is written during a write or read, modify write cycle while the chip enable is low. The I/O terminal requires connection to an external pull-up resistor since the output buffer has an open-drain configuration. The open-drain output buffer provides direct TTL sink compatibility with a fan-out of one Series 74 TTL gate. A low logic level results from conduction in the open-drain output buffer while a high level occurs with the buffer in its high-impedance state. Data written into the memory is read out in its true form.

refresh

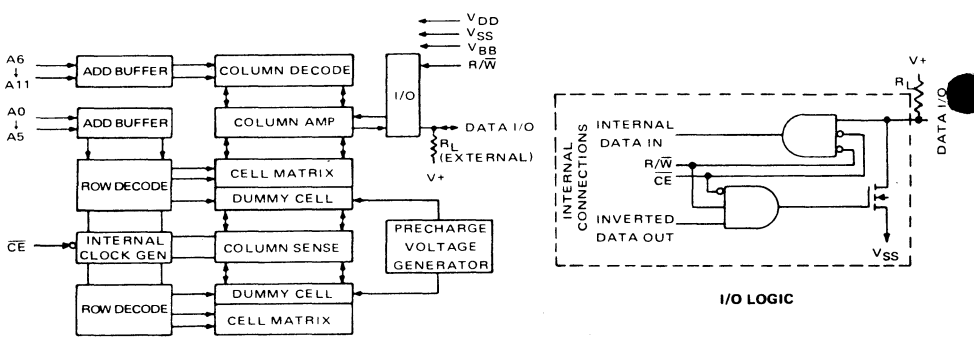
Refresh of the cell matrix is accomplished by performing a memory cycle at each of the 64 row addresses (A0 through A5) every 2 milliseconds or less. Addressing any row refreshes all 64 bits in that row. The column addresses (A6 through A11) can be indeterminate during refresh.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1)	−0.3 to 20 V
Supply voltage, V_{SS} (see Note 1)	−0.3 to 20 V
All input voltages (see Note 1)	−0.3 to 20 V
Chip-enable voltage (see Note 1)	−0.3 to 20 V
Output voltage (operating, with respect to V_{SS})	−2 to 7 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−55°C to 150°C

NOTE: 1. Under absolute maximum ratings, voltage values are with respect to the most-negative supply voltage, V_{BB} (substrate), unless otherwise noted. Throughout the remainder of this data sheet, voltage values are with respect to V_{SS}.

functional block diagram



I/O LOGIC

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	11.4	12	12.6	V
Supply voltage, V_{SS}		0		V
Supply voltage, V_{BB}	−4.5	−5	−5.5	V
High-level input voltage, V_{IH} (all inputs except chip enable)	2.2		5.5	V
High-level chip enable input voltage, $V_{IH(\overline{CE})}$	3		5.5	V
Low-level input voltage, V_{IL} (all inputs except chip enable) (see Note 2)	−0.6		0.6	V
Low-level chip enable input voltage, $V_{IL(\overline{CE})}$ (see Note 2)	−0.6		0.6	V
Refresh time, $t_{refresh}$			2	ms
Operating free-air temperature, T_A	0		70	°C

NOTE 2: The algebraic convention where the most negative limit is designated as minimum is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions, T_A = 0°C to 70°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	t_a = guaranteed maximum access time, R_L = 2.2 kΩ to 5.5 V, C_L = 50 pF, Load = 1 Series 74 TTL gate		2.4			V
V_{OL}	Low-level output voltage			V_{SS}		0.4	V
I_{OL}	Low-level output current	t_a = guaranteed maximum access time, C_L = 50 pF, V_{OL} = 0.4 V		5			mA
I_I	Input current (all inputs including I/O except chip enable)	V_I = −0.6 to 5.5 V				10	μA
$I_{I(\overline{CE})}$	Chip enable input current	V_I = −0.6 to 5.5 V				10	μA
I_{DD}	Supply current from V_{DD}	$V_{IL(\overline{CE})}$ = 0.6 V			37	70	mA
I_{DD}	Supply current from V_{DD}, standby	$V_{IH(\overline{CE})}$ = 3.5 V			5	8	mA
$I_{DD(av)}$	Average supply current from V_{DD} during read or write cycle	Minimum cycle timing	TMS 4051		45		mA
			TMS 4051-1		47		
$I_{DD(av)}$	Average supply current from V_{DD} during read, modify write cycle		TMS 4051		50		mA
			TMS 4051-1		54		
I_{BB}	Supply current from V_{BB}	V_{BB} = −5.5 V, V_{DD} = 12.6 V, V_{SS} = 0 V			5	100	μA

†All typical values are at T_A = 25°C.

capacitance at V_{DD} = 12 V, V_{SS} = 0 V, V_{BB} = −5 V, $V_{I(\overline{CE})}$ = 0 V, V_I = 0 V, f = 1 MHz, = 0°C to 70°C (unless otherwise noted)

PARAMETER		MIN	TYP†	MAX	UNIT
$C_{i(ad)}$	Input capacitance address inputs		5	7	pF
$C_{i(\overline{CE})}$	Input capacitance clock input		5	7	pF
$C_{i(R/\overline{W})}$	Input capacitance read/write input		5	7	pF
$C_{(I/O)}$	I/O terminal capacitance		7	9	pF

†All typical values are at T_A = 25°C.

read cycle timing requirements over recommended supply voltage range, T_A = 0°C to 70°C

PARAMETER		TMS 4051		TMS 4051-1		UNIT
		MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time	470		430		ns
$t_{w(\overline{CE}H)}$	Pulse width, chip enable high	130		130		ns
$t_{w(\overline{CE}L)}$	Pulse width, chip enable low	300	4000	260	4000	ns
$t_{r(\overline{CE})}$	Chip-enable rise time		40		40	ns
$t_{f(\overline{CE})}$	Chip-enable fall time		40		40	ns
$t_{su(ad)}$	Address setup time	0↓		0↓		ns
$t_{su(rd)}$	Read setup time	0↓		0↓		ns
$t_{h(ad)}$	Address hold time	180↓		165↓		ns
$t_{h(rd)}$	Read hold time	80↑		80↑		

↑↓The arrow indicates the edge of the chip-enable pulse used for reference: ↑for the rising edge, ↓for the falling edge.

read cycle switching characteristics over recommended supply voltage range, T_A = 0°C to 70°C

PARAMETER		TMS 4051		TMS 4051-1		UNIT
		TYP†	MAX	TYP†	MAX	
$t_{a(\overline{CE})}$	Access time from chip enable‡		280		230	ns
$t_{a(ad)}$	Access time from addresses*		300		250	ns
t_{PLH}	Propagation delay time, low-to-high level output from chip enable‡	60		60		ns

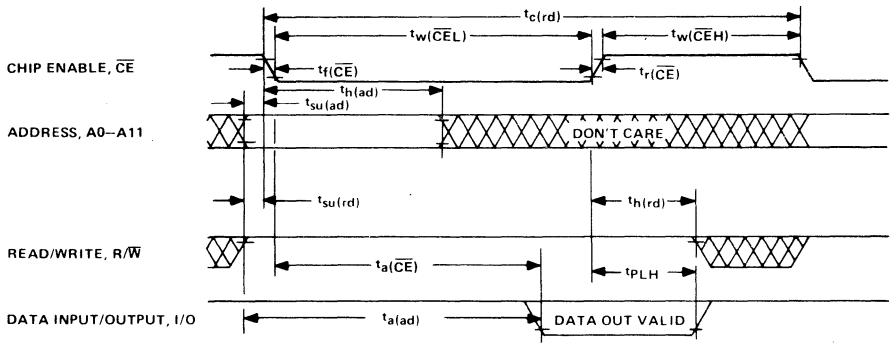
†All typical values are at T_A = 25°C.
‡Test conditions: C_L = 50 pF, R_L = 2.2 kΩ to 5.5 V, Load = 1 Series 74 TTL gate.
*Test conditions: C_L = 50 pF, R_L = 2.2 kΩ to 5.5 V, Load = 1 Series 74 TTL gate, $t_{f(\overline{CE})}$ = 20 ns.

write cycle timing requirements over recommended supply voltage range, T_A = 0°C to 70°C

PARAMETER		TMS 4051		TMS 4051-1		UNIT
		MIN	MAX	MIN	MAX	
$t_{c(wr)}$	Write cycle time	470		430		ns
$t_{w(\overline{CE}H)}$	Pulse width, chip enable high	130		130		ns
$t_{w(\overline{CE}L)}$	Pulse width, chip enable low	300	4000	260	4000	ns
$t_{w(wr)}$	Write pulse width	200		190		ns
$t_{r(\overline{CE})}$	Chip-enable rise time		40		40	ns
$t_{f(\overline{CE})}$	Chip-enable fall time		40		40	ns
$t_{su(ad)}$	Address setup time	0↓		0↓		ns
$t_{su(da\text{-}wr)}$	Data-to-write setup time*	0		0		ns
$t_{su(wr)}$	Write-pulse setup time	240↑		220↑		ns
$t_{d(\overline{CE}L\text{-}wr)}$	Chip-enable-low-to-write delay time†		60↓		60↓	ns
$t_{h(ad)}$	Address hold time	180↓		165↓		ns
$t_{h(da)}$	Data hold time	80↑		80↑		ns

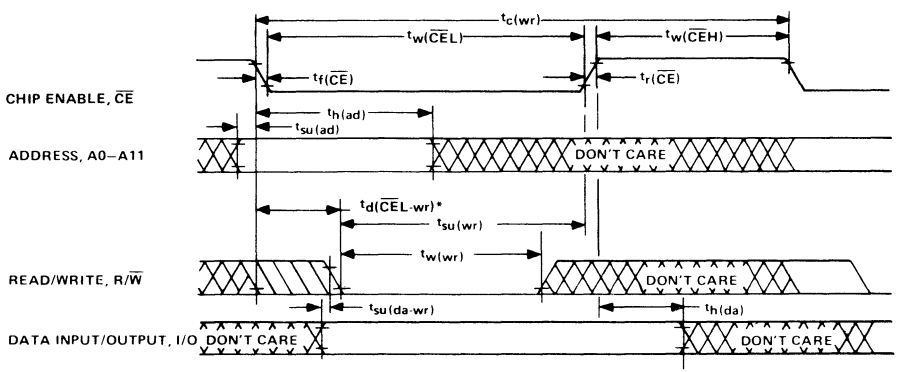
↑↓The arrow indicates the edge of the chip-enable pulse used for reference: ↑for the rising edge, ↓for the falling edge.
*If R/$\overline{W}$ is low before $\overline{CE}$ goes low, then I/O (data in) must be valid when $\overline{CE}$ goes low.
†The write pulse must go low at least $t_{su(wr)}$ minimum before $\overline{CE}$ goes high. If R/$\overline{W}$ remains high more than $t_{d(\overline{CE}L\text{-}wr)}$ maximum (60 ns) after $\overline{CE}$ goes low, the data-in driver must be disabled until R/$\overline{W}$ goes low since additional power to overcome the output buffer may be required when writing in a high with some of the faster devices (see comments on Region 1 under read, modify write timing diagram).

read or refresh cycle timing



NOTE: For the chip-enable input, high and low timing points are 3.0 V (high) and 1.0 V (low). Other input timing points are 0.6 V (low) and 2.2 V (high). Output timing points are 0.4 V (low) and 2.4 V (high).
For minimum cycle, $t_{r(\overline{CE})}$ and $t_{f(\overline{CE})}$ are equal to 20 ns.

write cycle timing



NOTE: For the chip-enable input, high and low timing points are 3.0 V (high) and 1.0 V (low). Other timing points are 0.6 V (low) and 2.2 V (high). Output timing points are 0.4 V (low) and 2.4 V (high).
*The write pulse must go low at least $t_{su(wr)}$ minimum before $\overline{CE}$ goes high. If R/$\overline{W}$ remains high more than $t_{d(\overline{CE}L\text{-}wr)}$ maximum (60 ns) after $\overline{CE}$ goes low, the data-in driver must be disabled until R/$\overline{W}$ goes low since additional power to overcome the output buffer may be required when writing in a high with some of the faster devices. During $t_{d(\overline{CE}L\text{-}wr)}$, R/$\overline{W}$ is permitted to change from high to low only.

read, modify write cycle timing requirements over recommended supply voltage range, T_A = 0°C to 70°C

PARAMETER		TMS 4051		TMS 4051-1		UNIT
		MIN	MAX	MIN	MAX	
$t_{c(RMW)}$	Read, modify write cycle time†	730		660		ns
$t_{w(\overline{CE}H)}$	Pulse width, chip enable high†	130		130		ns
$t_{w(\overline{CE}L)}$	Pulse width, chip enable low	560	4000	490	4000	ns
$t_{w(wr)}$	Write pulse width	200		190		ns
$t_{r(\overline{CE})}$	Chip-enable rise time		40		40	ns
$t_{f(\overline{CE})}$	Chip-enable fall time		40		40	ns
$t_{d(wr\text{-}daL)}$	Write to data-in-low delay time		20		20	ns
$t_{su(ad)}$	Address setup time	0↓		0↓		ns
$t_{su(daH)}$	Data-in-high setup time	240↑		220↑		ns
$t_{su(rd)}$	Read-pulse setup time	0↓		0↓		ns
$t_{su(wr)}$	Write-pulse setup time	240↑		220↑		ns
$t_{h(ad)}$	Address hold time	180↓		165↓		ns
$t_{h(rd)}$	Read hold time	320↓		270↓		ns
$t_{h(da)}$	Data hold time	80↑		80↑		ns

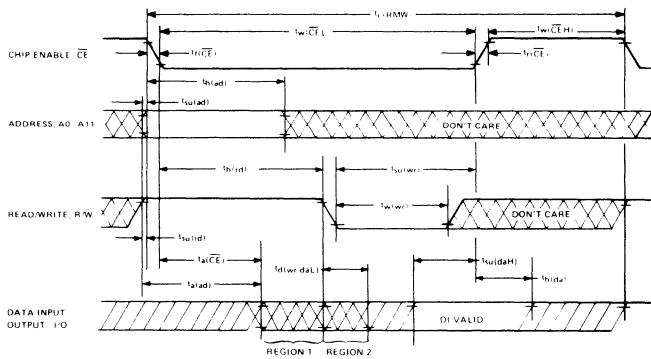
↑↓The arrow indicates the edge of the chip-enable pulse for reference: ↑for the rising edge; ↓for the falling edge.
†Test conditions: $t_{f(rd)}$ = 20 ns.

read, modify write cycle swithcing characteristics over recommended supply voltage range, T_A = 0°C to 70°C

PARAMETER		TMS 4051		TMS 4051-1		UNIT
		MIN	MAX	MIN	MAX	
$t_{a(\overline{CE})}$	Access time from chip enable*		280		230	ns
$t_{a(ad)}$	Access time from addresses†		300		250	ns

*Test conditions: C_L = 50 pF, R_L = 2.2 kΩ, Load = 1 Series 74 TTL gate.
†Test conditions: C_L = 50 pF, R_L = 2.2 kΩ, Load = 1 Series 74 TTL gate, $t_{f(\overline{CE})}$ = 20 ns.

read, modify write cycle timing

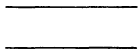
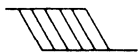
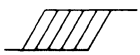
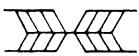


REGION 1 - In region 1 data out is valid until the I/O terminal is forced high or low by the data in driver. A transition from low to high is permissible but additional power to overcome the output buffer will be required. A transition from high to low is permitted without power penalty.

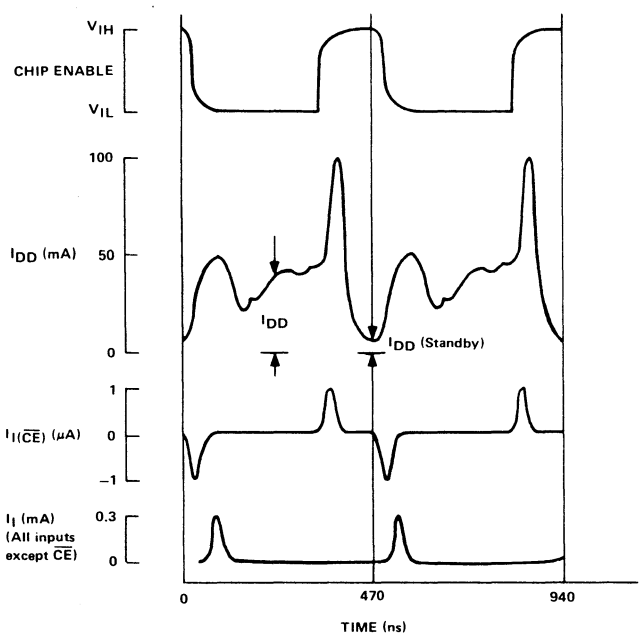
REGION 2 - In region 2 a single transition is permitted. It is NOT a true "Don't Care" region. If a low is to be written it must be valid by the end of region 2.

NOTE: For the chip enable input high and low timing points are 3.0 V (high) and 1.0 V (low). Other input timing points are 0.6 V (low) and 2.2 V (high). Output timing points are 0.4 V (low) and 2.4 V (high).
For minimum cycle, $t_{r(\overline{CE})}$ and $t_{f(\overline{CE})}$ are equal to 20 ns.

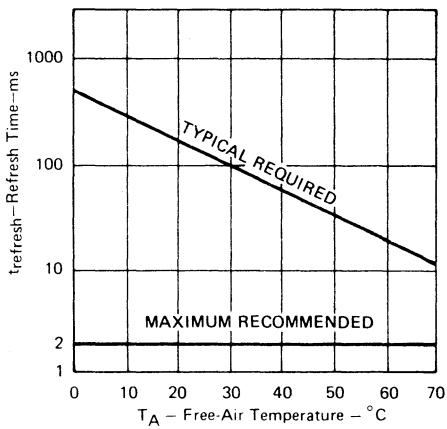
timing diagram conventions

TIMING DIAGRAM SYMBOL	MEANING: INPUT FORCING FUNCTIONS	MEANING: OUTPUT RESPONSE FUNCTIONS
	Must be steady high or low	Will be steady high or low
	High-to-low changes permitted	Will be changing from high to low sometime during designated interval
	Low-to-high changes permitted	Will be changing from low to high sometime during designated interval
	Don't Care	State unknown or changing
	(Does not apply)	Center line is high-impedance off-state

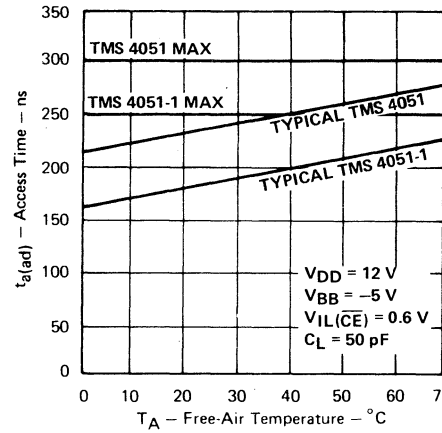
TYPICAL WAVEFORMS



REFRESH TIME vs TEMPERATURE



ACCESS TIMES vs TEMPERATURE



TMS 4116-25 JL, TMS 4116-20 JL, TMS 4116-15 JL
16,384-BIT DYNAMIC RANDOM-ACCESS MEMORY

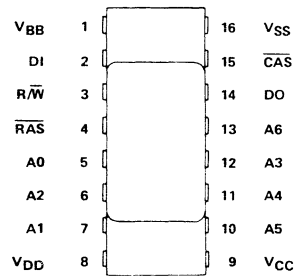
1977

- 16,384 X 1 Organization
- 16-Pin 300-Mil Package Configuration
- 10% Tolerance on all Supplies
- All Inputs Including Clocks TTL Compatible
- Three-State Fully TTL-Compatible Output
- One-Chip Latches for Addresses and Data Input
- 3 Performance Ranges:

	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)
TMS 4116-25	250 ns	165 ns	410 ns
TMS 4116-20	200 ns	135 ns	375 ns
TMS 4116-15	150 ns	100 ns	375 ns

- Page-Mode Operation for Faster Access Time
- Common I/O Capability
- Low Power Dissipation
- 1-T Cell Design, N-Channel Silicon-Gate Technologie

16-PIN CERAMIC
DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

The TMS 4116 JL series is composed of monolithic high-speed dynamic 16,384-bit MOS random-access memories, organized as 16,384 one-bit words, employing single-transistor storage cells and N-channel silicon-gate technology.

All inputs and outputs are compatible with Series 74 TTL circuits including clocks: Row Address Strobe ($\overline{RAS}$) and Column Address Strobe ($\overline{CAS}$). All address lines (A0 through A6) and data-in (DI) are latched on chip to simplify system design. Data out (DO) is unlatched to allow greater system flexibility.

Typical power dissipation is less than 600 milliwatts active and 10 milliwatts during standby (V_{CC} is not required during standby operation). To retain data, only 18 milliwatts average power is required which includes the power consumed to refresh the contents of the memory.

The TMS 4116 JL series is offered in a 16-pin dual-in-line package and is guaranteed for operation from 0°C to 70°C. Packages are designed for insertion in mounting-hole rows on 300-mil centers.

operation

address (A0 through A6)

Fourteen address bits are required to decode 1 of 16,384 storage cell locations. Seven row-address bits are set up on pins A0 through A6 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the seven column-address bits are set up on pins A0 through A6 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

† The term "read-write cycle" is sometimes used as an alternative title to "read-modify-write cycle".

mode select (R/$\overline{W}$)

The read or write mode is selected through the read/write (R/$\overline{W}$) input. A logic high on the R/$\overline{W}$ input selects the read mode and a logic low selects the write mode. The read/write terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When R/$\overline{W}$ goes low prior to $\overline{CAS}$, data-out will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data-in (DI)

Data is written during a write or read-modify write cycle. The latter falling edge of $\overline{CAS}$ or R/$\overline{W}$ strobes data into the on-chip data latch. This latch can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle R/$\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read-modify write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by R/$\overline{W}$ with setup and hold times referenced to this signal.

data-out (DO)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan-out of two Series 74 TTL loads. Data-out is the same polarity as data-in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output goes active after the enable time interval that begins with the negative transition of $\overline{CAS}$. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low before $\overline{CAS}$ going high returns it to a high-impedance state. In an early write cycle the output is always in the high-impedance state. In a delayed write or read-modify write cycle the output will follow the sequence for the read cycle.

refresh

A refresh operation must be performed at least every two milliseconds to retain data. Since the output buffer is in the high-impedance state unless $\overline{CAS}$ is applied, the $\overline{RAS}$ only refresh sequence avoids any output during refresh. Strobing each of the 128 row addresses (A0 through A6) with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ remains high (inactive) for this refresh sequence, thus conserving power.

page mode

Page mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the chip. Thus, the time required to setup and strobe the row addresses is eliminated. To extend beyond the 128 column locations on a single RAM, apply the row address and $\overline{RAS}$ to multiple 16K RAMs, then decode $\overline{CAS}$ to select the proper RAM.

TMS 4070 JL, TMS 4070-1 JL, TMS 4070-2 JL
16,384-BIT DYNAMIC RANDOM-ACCESS MEMORY

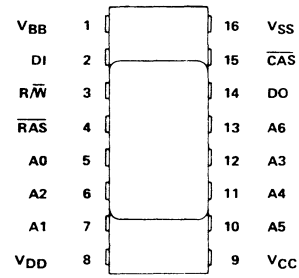
OCTOBER 1976

- 16,384 X 1 Organization
- 16-Pin 300-Mil Package Configuration
- All Inputs Including Clocks TTL Compatible
- Three-State Fully TTL-Compatible Output
- On-Chip Latches for Addresses and Data Input
- 3 Performance Ranges:

	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	READ-MODIFY WRITE† CYCLE (MIN)
TMS 4070	350 ns	255 ns	500 ns	730 ns
TMS 4070-1	300 ns	210 ns	450 ns	660 ns
TMS 4070-2	250 ns	165 ns	400 ns	590 ns

- Page-Mode Operation for Faster Access Time
- Common I/O Capability
- Low-Power Dissipation
  - Less than 600 mW Operating (Typical)
  - 10 mW Standby (Typical)
- 1-T Cell Design, N-Channel Silicon-Gate Technology

16-PIN CERAMIC
DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

The TMS 4070 JL series is composed of monolithic high-speed dynamic 16,384-bit MOS random-access memories, organized as 16,384 one-bit words, employing single-transistor storage cells and N-channel silicon-gate technology.

All inputs and outputs are compatible with Series 74 TTL circuits including clocks: Row Address Strobe ($\overline{RAS}$) and Column Address Strobe ($\overline{CAS}$). All address lines (A0 through A6) and data-in (DI) are latched on chip to simplify system design. Data out (DO) is unlatched to allow greater system flexibility.

Typical power dissipation is less than 600 milliwatts active and 10 milliwatts during standby (V_{CC} is not required during standby operation). To retain data, only 18 milliwatts average power is required which includes the power consumed to refresh the contents of the memory.

The TMS 4070 JL series is offered in a 16-pin dual-in-line package and is guaranteed for operation from 0°C to 70°C. Packages are designed for insertion in mounting-hole rows on 300-mil centers.

operation

address (A0 through A6)

Fourteen address bits are required to decode 1 of 16,384 storage cell locations. Seven row-address bits are set up on pins A0 through A6 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the seven column-address bits are set up on pins A0 through A6 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

† The term "read-write cycle" is sometimes used as an alternative title to "read-modify-write cycle".

mode select (R/$\overline{W}$)

The read or write mode is selected through the read/write (R/$\overline{W}$) input. A logic high on the R/$\overline{W}$ input selects the read mode and a logic low selects the write mode. The read/write terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When R/$\overline{W}$ goes low prior to $\overline{CAS}$, data-out will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data-in (DI)

Data is written during a write or read-modify write cycle. The latter falling edge of $\overline{CAS}$ or R/$\overline{W}$ strobes data into the on-chip data latch. This latch can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle R/$\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read-modify write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by R/$\overline{W}$ with setup and hold times referenced to this signal.

data-out (DO)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan-out of two Series 74 TTL loads. Data-out is the same polarity as data-in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output goes active after the enable time interval that begins with the negative transition of $\overline{CAS}$. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low before $\overline{CAS}$ going high returns it to a high-impedance state. In an early write cycle the output is always in the high-impedance state. In a delayed write or read-modify write cycle the output will follow the sequence for the read cycle.

refresh

A refresh operation must be performed at least every two milliseconds to retain data. Since the output buffer is in the high-impedance state unless $\overline{CAS}$ is applied, the $\overline{RAS}$ only refresh sequence avoids any output during refresh. Strobing each of the 128 row addresses (A0 through A6) with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ remains high (inactive) for this refresh sequence, thus conserving power.

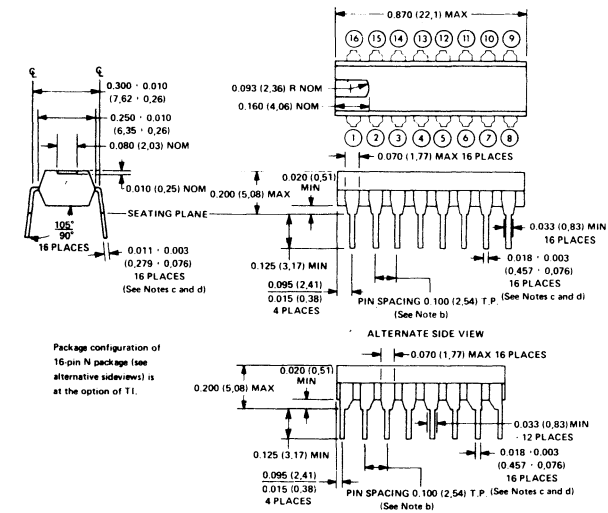
page mode

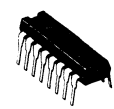
Page mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the chip. Thus, the time required to setup and strobe the row addresses is eliminated. To extend beyond the 128 column locations on a single RAM, apply the row address and $\overline{RAS}$ to multiple 16K RAMs, then decode $\overline{CAS}$ to select the proper RAM.

N plastic dual-in-line packages

These dual-in-line packages consist of a circuit mounted on a 14-, 16-, 20-, or 28-lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. The packages are intended for insertion in mounting hole rows on 0.300 (7,62) or 0.600 (15,24) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

16-PIN N PLASTIC

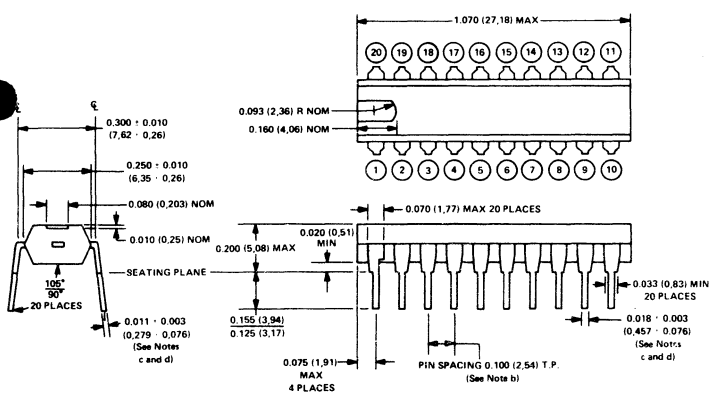


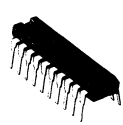


ALTERNATE SIDE VIEW

Package configuration of 16-pin N package (see alternative sideviews) is at the option of TI.

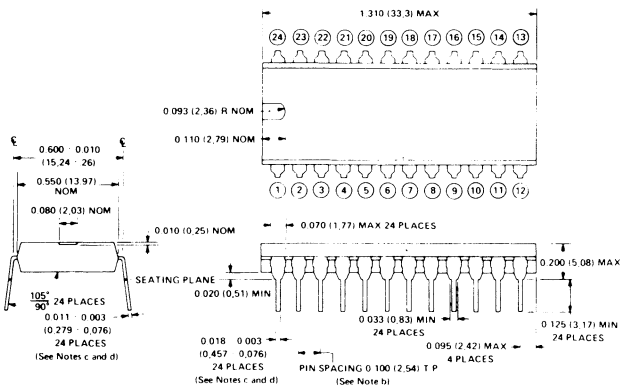
20-PIN N PLASTIC

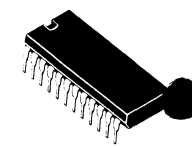




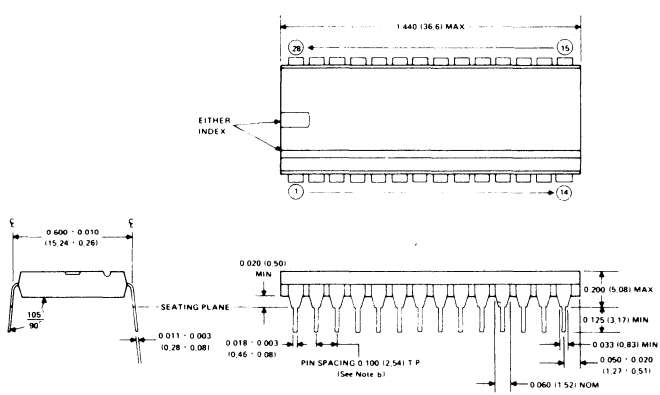
N plastic dual-in-line packages (continued)

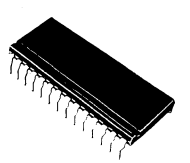
24-PIN N PLASTIC





28-PIN N PLASTIC





NOTES: a. All dimensions are shown in inches (and parenthetically in millimeters for reference only). Inch dimensions govern.
b. Each pin centerline is located within 0.010 (0,26) of its true longitudinal position.
c. This dimension does not apply for solder dipped leads.
d. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0.020 (0,50) above the seating plane.

general

Electrical characteristics presented in this catalog, unless otherwise noted, apply for circuit type(s) listed in the page heading, regardless of package. Factory orders for circuits described should include the complete part-type numbers listed on each page.

MOS NUMBERING SYSTEM

EXAMPLE: TM S 4030 N L

1. TI MOS Prefix
2. Product Status
   - S Standard devices
   - X Prototype or experimental
   - C Custom design
   - T High reliability
3. Unique Product Identification Number
4. Package
   - F Flat
   - J Ceramic dual-in-line
   - N Plastic dual-in-line
   - L Metal can
   - U Unencapsulated (beam lead, etc.)
5. Temperature Range
   - C -25°C to 85°C
   - L 0°C to 70°C
   - M -55°C to 125°C
   - R -55°C to 85°C
   - S Special range

manufacturing information

Alloying is performed in an inert atmosphere. A silicon gold eutectic is formed during the alloying operation.

Thermal compression bonding is used. Typical bond strength is 5 grams. Bond strength is monitored on a lot-to-lot basis. Any bond strength of less than 2 grams causes rejection of the entire lot of devices.

TI uses a low-temperature alloy brazing to seal ceramic packages. Metal-can packages are welded. Glass leaks are eliminated by testing in a fluorocarbon solution heated to 150°C. Fine-leak elimination is performed through mass spectrometer techniques. All MOS LSI devices produced by TI are capable of withstanding 5×10^{-7} ppm fine-leak inspection, and may be screened to 5×10^{-8} ppm fine leak, if desired by the customer, for special applications.

All packages are capable of withstanding a shock of 3,000 G. All packages are capable of passing a 20,000-G acceleration (centrifuge) test in the Y axis. Pin strength is measured by a pin-shearing test. All pins are able to withstand the application of a force of 6 pounds at 45° in the peel-off direction.

dual-in-line packages

A pin-to-pin spacing of 100 mils has been selected for all dual-in-line packages.

TI uses several hermetically sealed ceramic dual-in-line packages, each of which consist of a ceramic base, plated metal cap, and tin-plated leads.

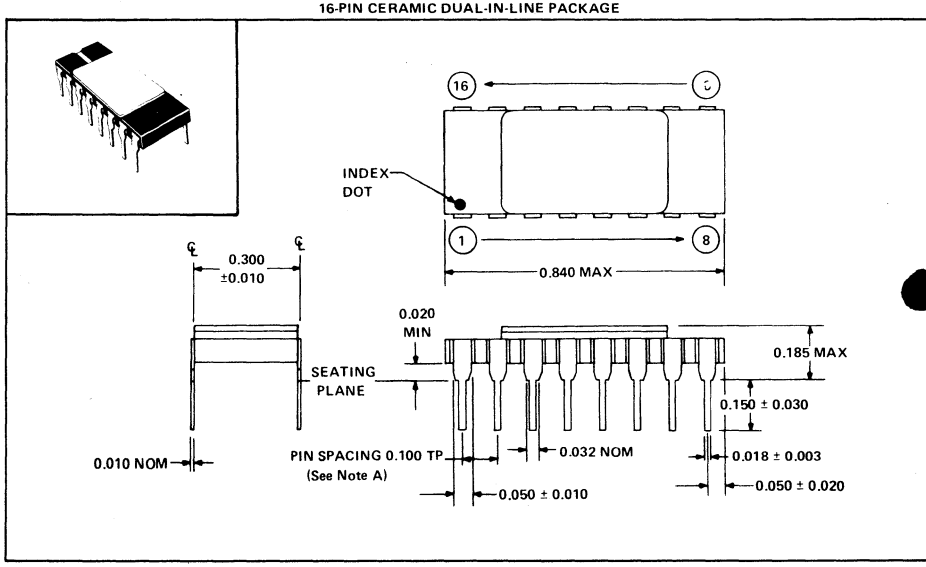
The following dual-in-line packages are available in plastic or ceramic:

	8 PIN	10 PIN	16 PIN	18 PIN	22 PIN	24 PIN	28 PIN	40 PIN
300 mils between rows	X†	X†	X	X				
400 mils between rows					X	X†		
600 mils between rows						X	X	X

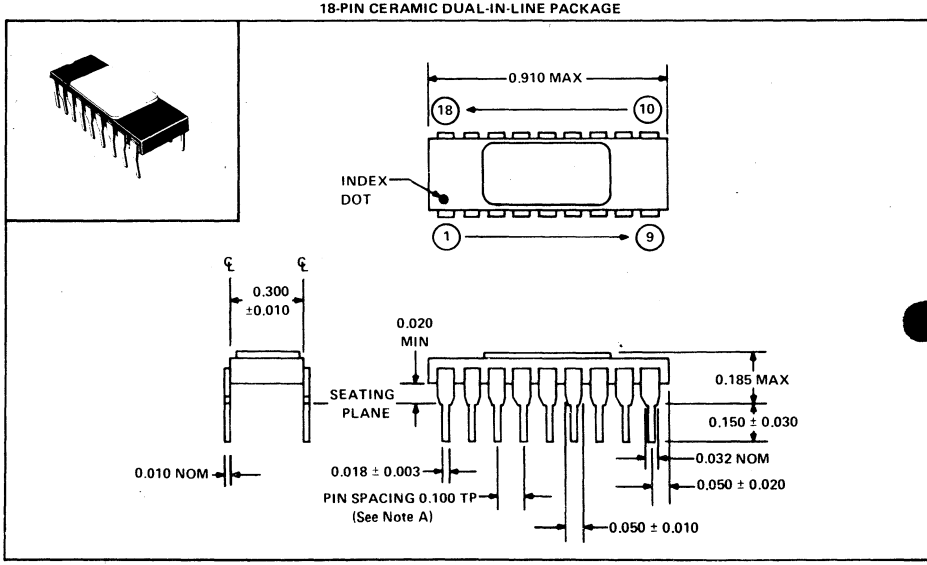
† There are no products shown in this data book in the 8 pin ceramic package or the ceramic or plastic 10 pin or 24 pin, 400 mil package.

MOS LSI MECHANICAL DATA

16-PIN CERAMIC DUAL-IN-LINE PACKAGE

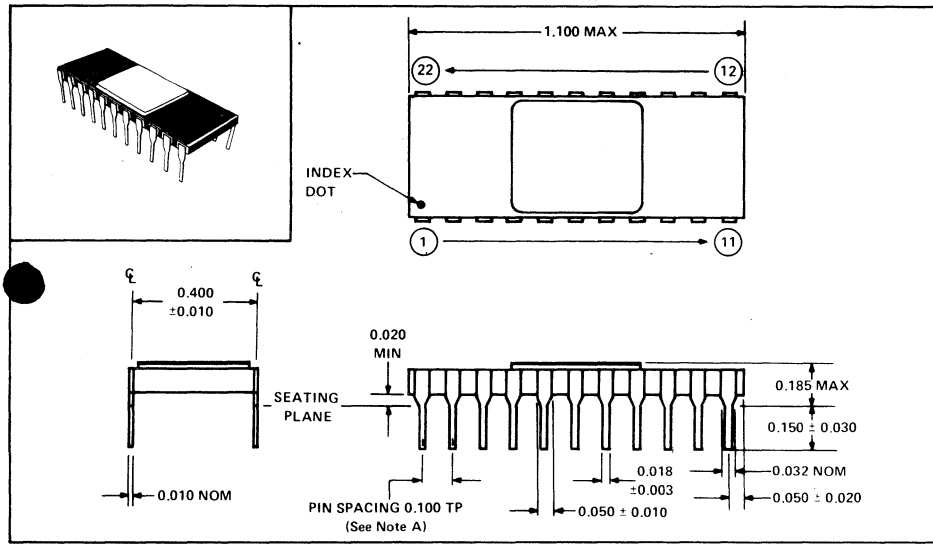


18-PIN CERAMIC DUAL-IN-LINE PACKAGE

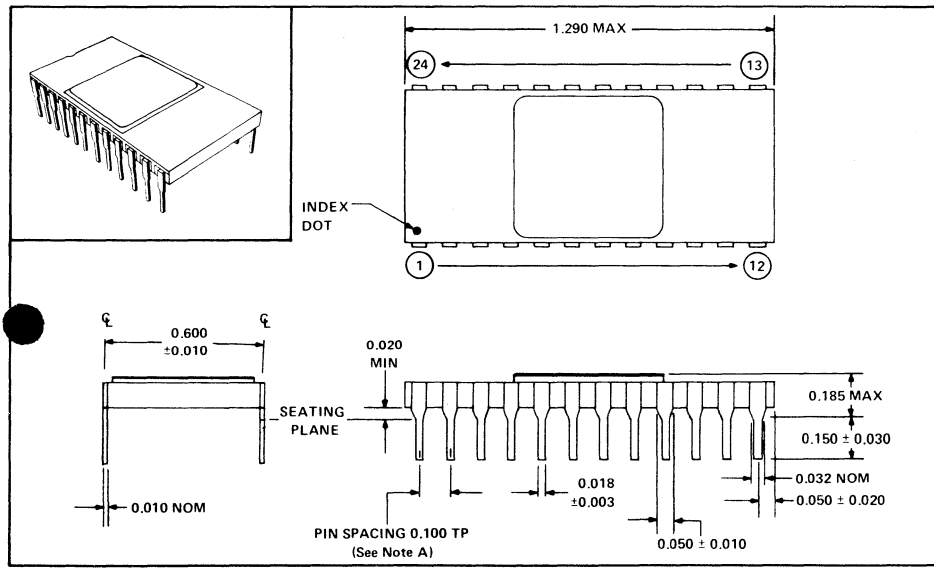


NOTES: A. Each pin centerline is located within 0.010 of its true longitudinal position.
B. All linear dimensions are in inches.

22-PIN CERAMIC DUAL-IN-LINE PACKAGE

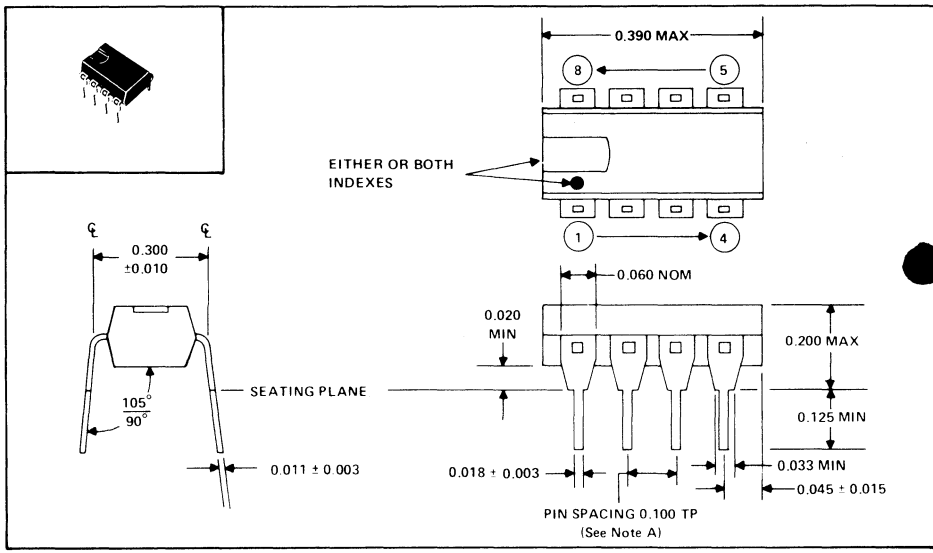


24-PIN CERAMIC DUAL-IN-LINE PACKAGE

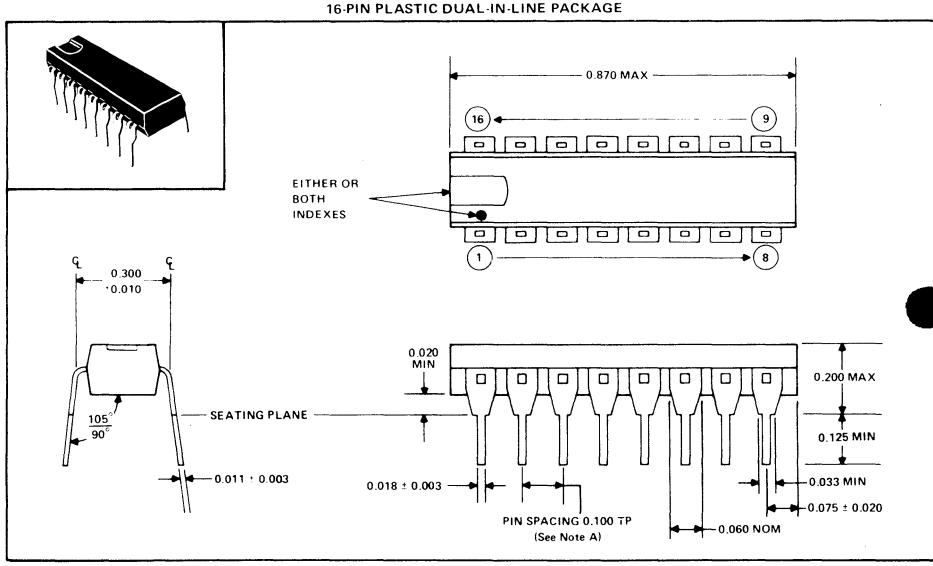


NOTES: A. Each pin centerline is located within 0.010 of its true longitudinal position.
B. All linear dimensions are in inches.

8-PIN PLASTIC DUAL-IN-LINE PACKAGE

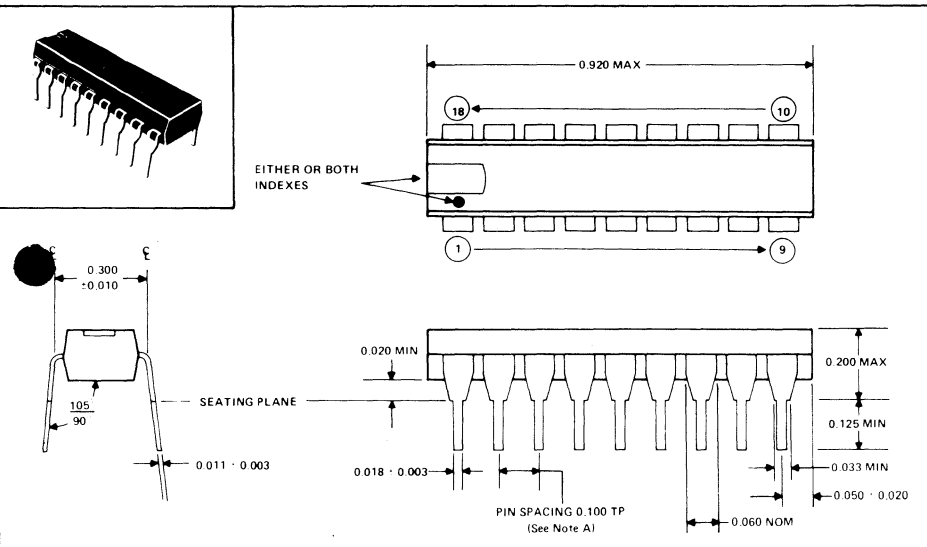


16-PIN PLASTIC DUAL-IN-LINE PACKAGE

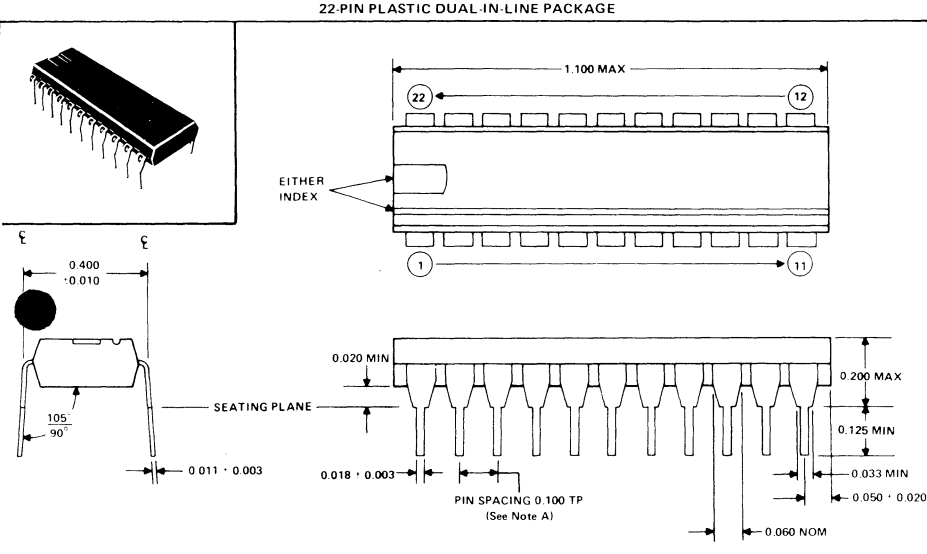


NOTES: A. Each pin centerline is located within 0.010 of its true longitudinal position.
B. All linear dimensions are in inches.

18-PIN PLASTIC DUAL-IN-LINE PACKAGE

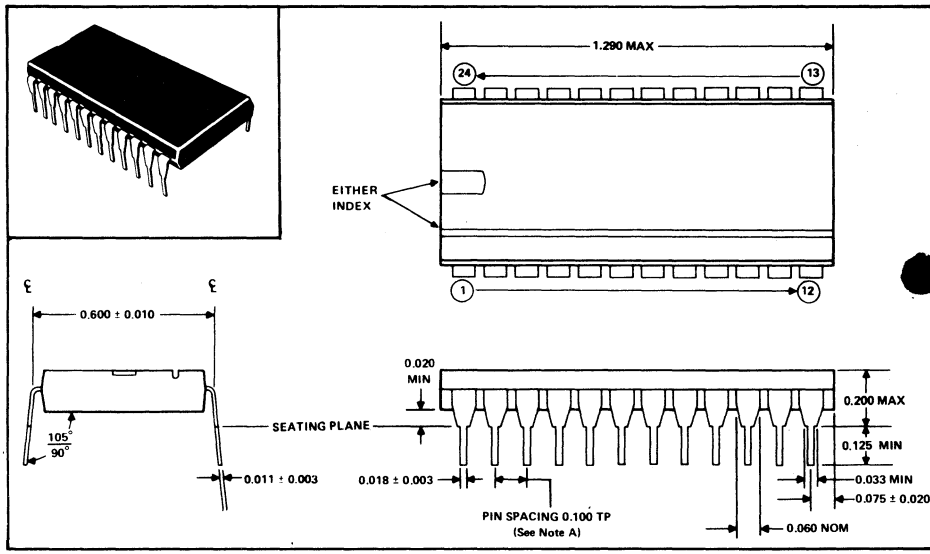


22-PIN PLASTIC DUAL-IN-LINE PACKAGE

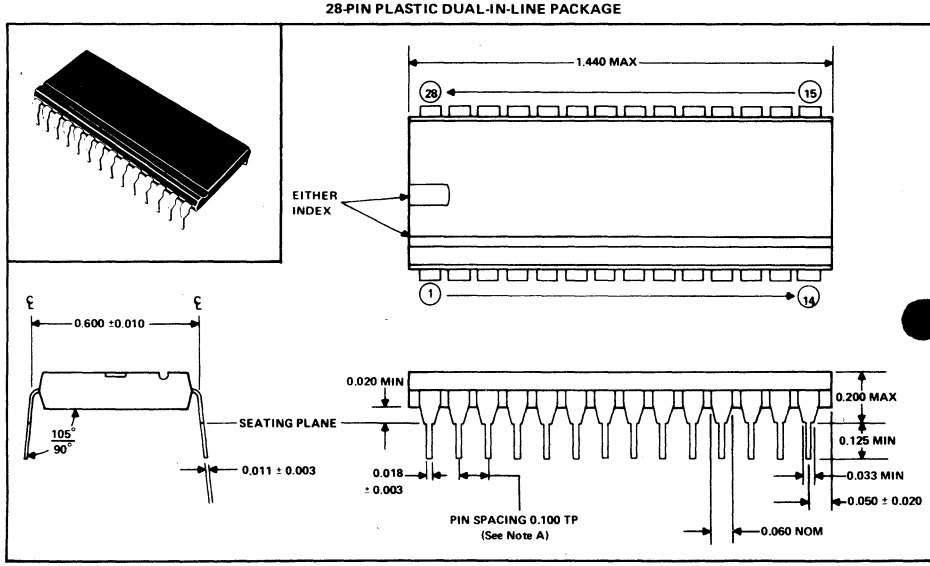


NOTES: A. Each pin centerline is located within 0.010 of its true longitudinal position.
B. All linear dimensions are in inches.

24-PIN PLASTIC DUAL-IN-LINE PACKAGE



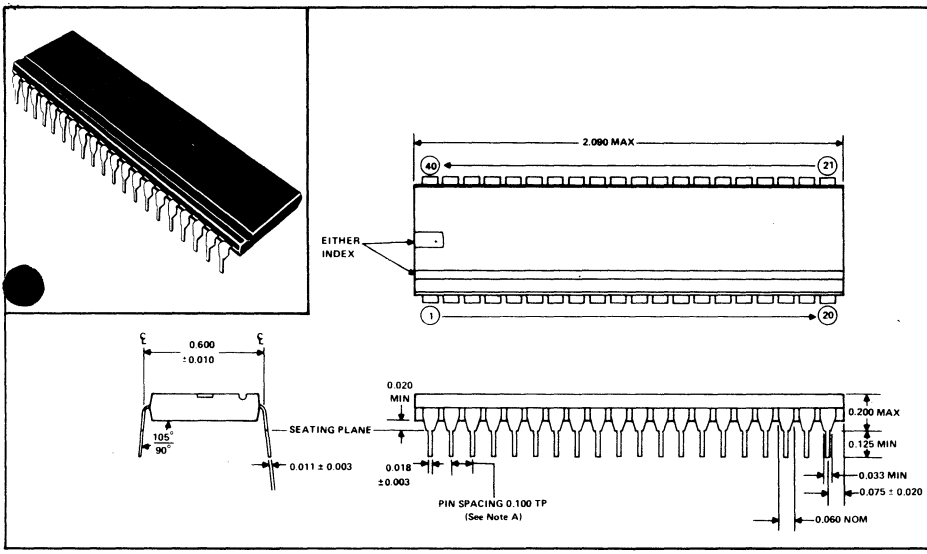
28-PIN PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. Each pin centerline is located within 0.010 of its true longitudinal position.
B. All linear dimensions are in inches.

MOS LSI MECHANICAL DATA

40-PIN PLASTIC DUAL-IN-LINE PACKAGE



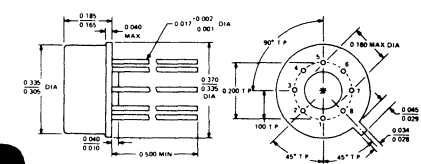
NOTES: A. Each pin centerline is located within 0.010 of its true longitudinal position.

B. All linear dimensions are in inches.

metal-can

For devices such as shift registers requiring few inputs and outputs, TI uses two metal-can packages.

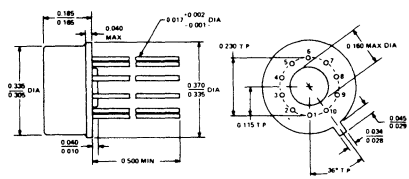
8-PIN METAL CAN



ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED

Same as JEDEC TO-99 and MO-002AK except for diameter of standoff

10-PIN METAL CAN



ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED

Same as JEDEC TO-100 and MO-006AD except for diameter of standoff

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DMP 003 N-1