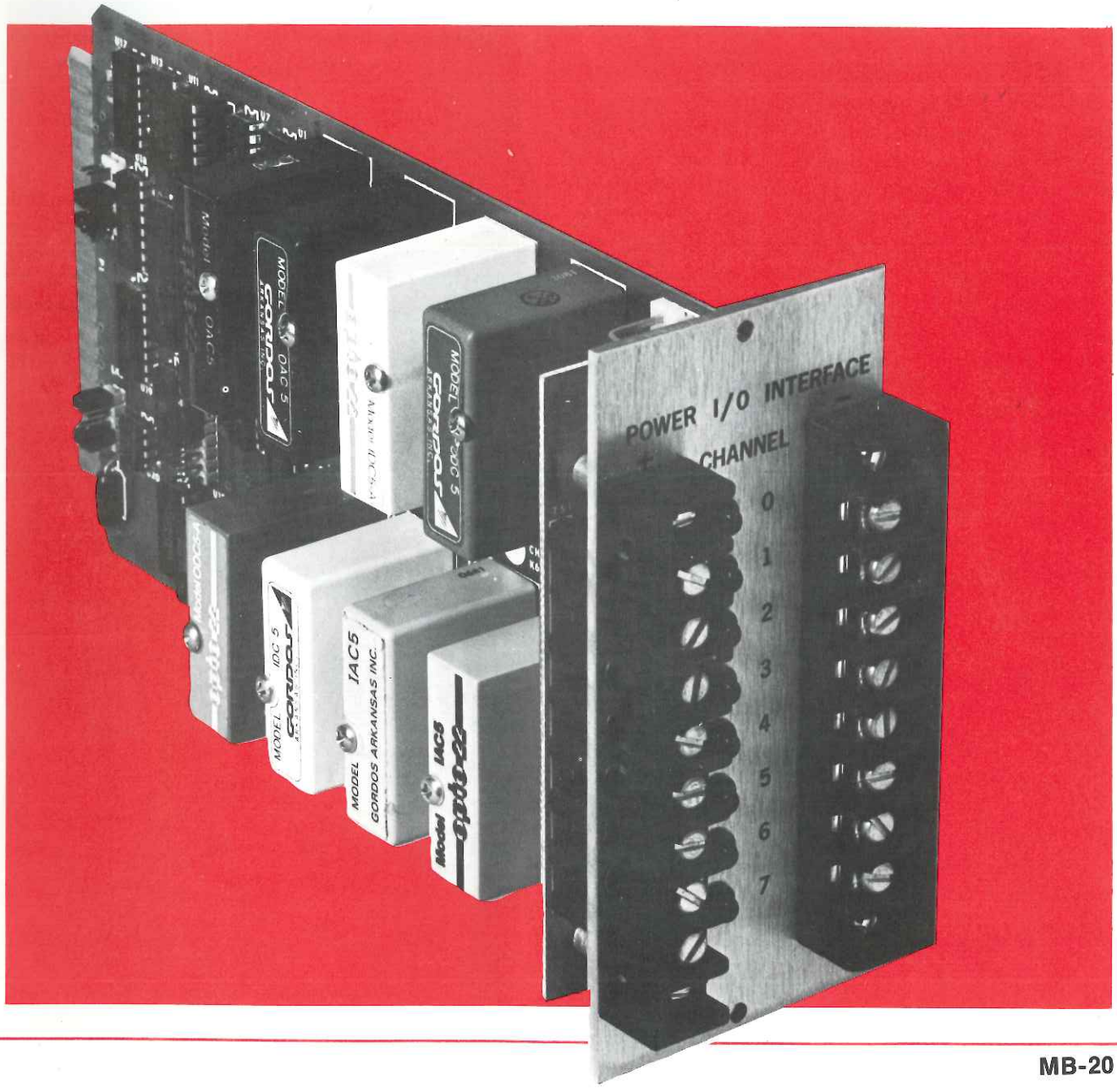
RCA Solid State

RCA Microboard Power I/O Interface

MSIM 20



Power I/O Interface
MSIM 20

The MSIM 20 Power I/O Interface provides a rugged, compact, and extremely flexible way to interface power input or output signals to a Microboard computer system. The MSIM 20 accepts eight industry- standard optically isolated interface modules in any mix of input or output and provides barrier strips with captive clamps for wiring connections. The MSIM 20 occupies only 2.4 inches of front panel space (4 board slots) on an RCA Industrial Chassis and is firmly secured to the chassis. It has eight status LED's visible from the front and eight clip-mounted fuses inside.

The direction, input or output, of each channel is determined only by the module that is plugged in; no changes of any kind are required on the MSIM 20. The status of all channels can be read at any time. A versatile interrupt circuit is provided that senses a change of state of any or all channels. The interrupt mask is set under software control. I/O addresses and flag assignments are set by push-on links; no cutting or soldering is required.

All CMOS circuitry is employed, resulting in high noise immunity, a wide (-40 to +85° C) operating range, and low power consumption. The MSIM 20 is compatible with the broad line of RCA Microboards.

Features

- **Flexible:** Accepts eight channels of industry standard I/O modules in any combination of input or output, AC or DC; no changes of any kind are required. Interfaces with any of the broad line of RCA Microboards.
- **Powerful:** Controls eight channels of up to 3A, 240 V AC each.
- **Rugged:** 1/8" thick aluminum front panel mounts barrier strips with captive screw clamp connections: takes wire sizes up to #12. Operates over a wide temperature range, -40 to +85°C.
- **Compact:** Takes only 2.4" of front panel space 5.25" high, mounted in a MSI 800 or 8800 series chassis.
- **Convenient:** Wiring trough (MSIA 10) and protective see-through front panel guards (MSIA 400 series) are available (See RCA Microboard Industrial Chassis Series, publication MB-8). Fuses (clip mounted) and I/O modules (socketed) may be changed without unwiring the front panel.
- **Easy to Program:** I/O address set by a few links. Standard Microboard I/O conventions apply and are supported in several high-level languages such as Pascal, PLM, and BASIC.
- **Versatile Interrupts:** Any channel may be unmasked (under program control) to give an interrupt when it changes state. Interrupts are automatically reset when the board is read.

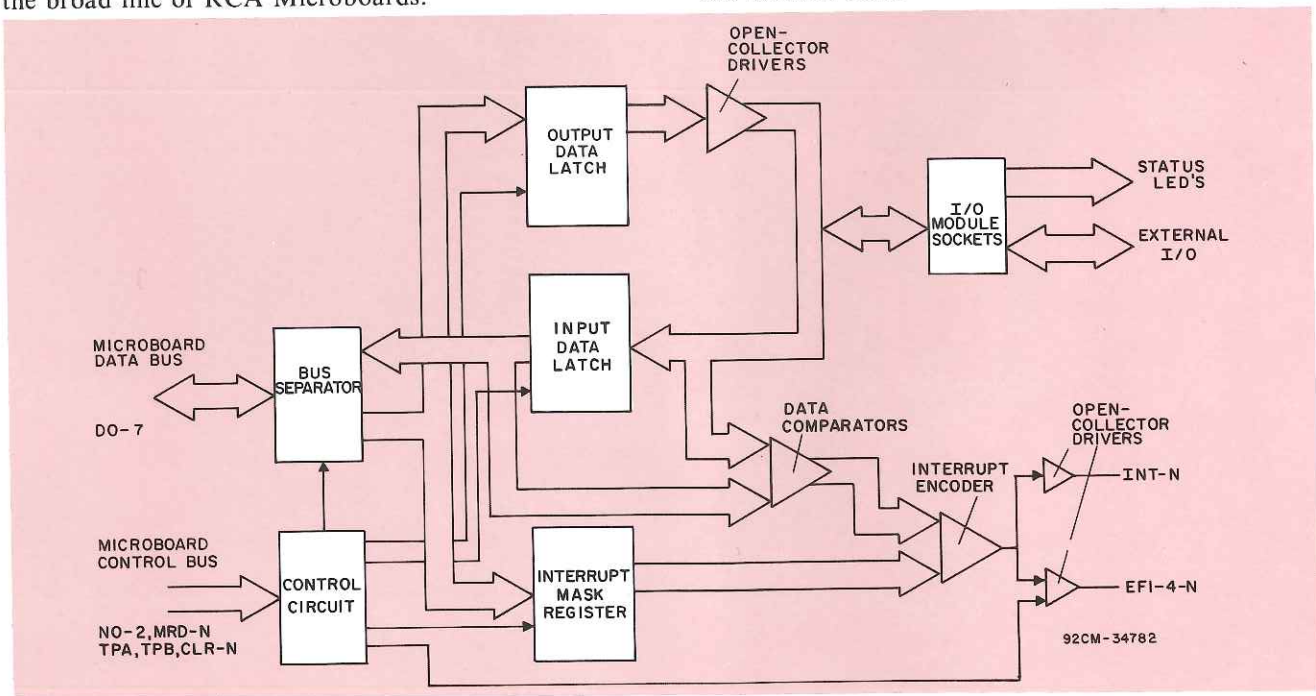


Fig. 1 - Block diagram of MSIM 20 Power I/O Interface.

Printed in USA/5-82

Specifications:

Operating Temperature Range:
-40°C to +85°C

Drive Current:
(Current available to drive I/O module.)
Sink (on drive): 14 mA min.
Source (off leakage): 20 μA max.

Drive Voltage:
(Voltage available to drive I/O module.)
3 V min. (nominal 5-V supply; includes drop across status-indicator LED)

Input Impedance:
3.3-kilohm pullup to 5-volt supply

Input Threshold:
"0" input: 1.5 V max.
"1" input: 3.5 V min.

Voltage Requirements:
+ 5 volts ± 10 %

Current Requirements:
See discussion under system power requirements.

Dimensions:
See Fig. 2

Fusing:
(8 fuses provided in spring clips)
4 A; 250 V rating, 5 X 20 mm
Littlefuse No. 212 004,
Bussman No. GMA4, or equivalent

Isolation:
1.5 KV rms AC minimum, input (output) to logic or channel to channel

Wire Capacity:
#12 - #22 AWG

Wiring Connections:
Two barrier blocks with 8 captive clamps each

Weight:
11 ounces (312 grams) with no modules mounted; modules weight approximately 1.25 ounces (35 grams) each.

Introduction

The MSIM 20 Power I/O Interface consists of two sections: (1) a logic/power board that plugs into a Microboard backplane and (2) a front panel assembly that mounts to the front of any Microboard Industrial Chassis (MSI 804 - 825 or MSI 8804 - 8825). The two parts plug together with heavy right-angle connectors.

The **logic/power board** contains the interface between the Microboard backplane and the power I/O modules, as well as interrupt-generating logic. Spring sockets and press in nuts are provided to mount up to eight modules. Fuses (5 x 20 mm) are provided mounted in spring clips.

The **front panel assembly** holds two eight-position barrier strips for external wiring and eight LED'S driven by the modules. It mounts in place of a MSIA 08 four-card

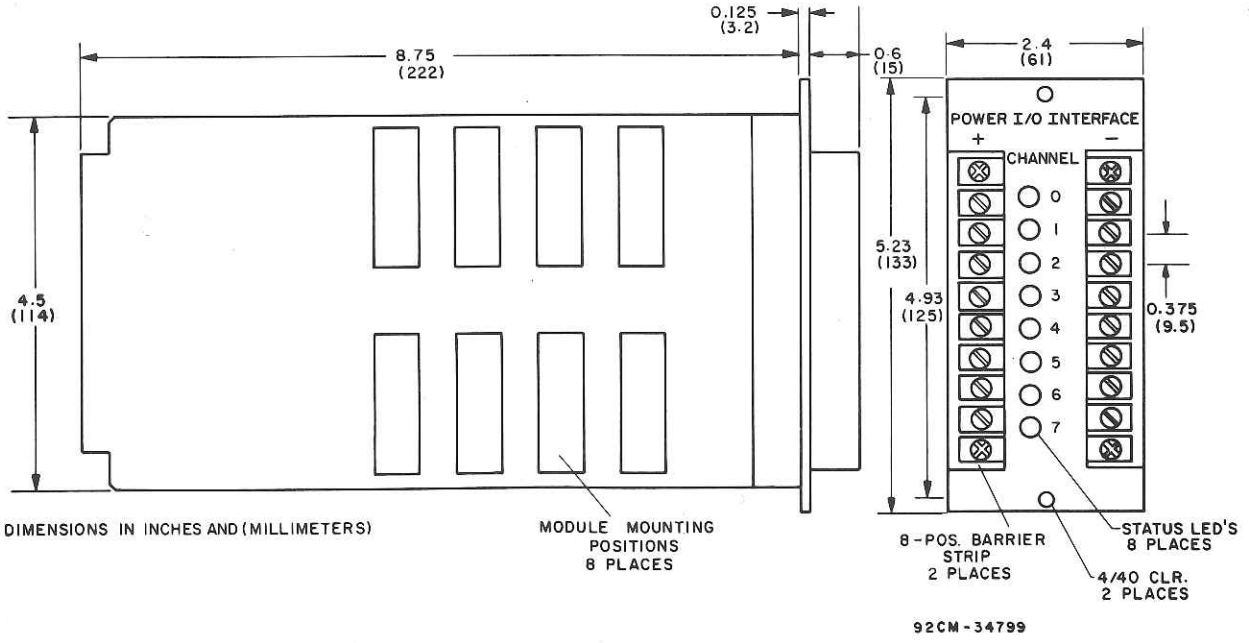


Fig. 2 - Dimensions of MSIM 20 Power I/O Interface.

Power I/O Interface
MSIM 20

front panel to the chassis front extrusions. The barrier strips are marked channels 0 - 7 (corresponding to bit positions 0 - 7), and + and - are indicated for use when DC modules are installed.

RCA does not supply the power modules for use in the MSIM 20. See Table I for a representative list of functionally equivalent modules that should work with the MSIM 20. Fig. 3 gives the dimensions for the module mounting positions.

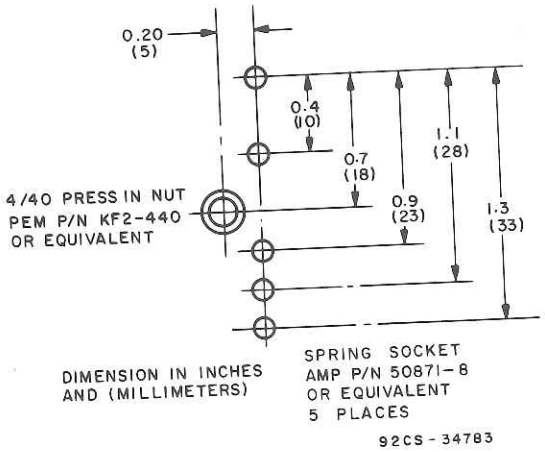


Fig. 3 - Dimensions of MSIM 20 module mounting positions.

Microboard Backplane

The Microboard Backplane consists of a 44-pin bus that is common to all sockets. Table II gives assignments for the backplane interface with the signals that are of interest to the MSIM 20 marked with an asterisk (*). Refer to published data on the CDP1802A microprocessor (File No. 1305) or to the **User Manual For the CDP1802 COSMAC Microprocessor,** MPM-201, for detailed information on CDP1802 bus signals. Following is a brief discussion of the signals that apply to the MSIM 20.

DB0-DB7: The 8 bit bidirectional bus through which input or output data is passed between the Microboard system and the MSIM 20. Bit 0 through bit 7 correspond to channels 0 - 7. They are driven by three-state drivers.

N0-N2: The three I/O address lines from the microprocessor used to indicate that an input or output is in progress and to which address (1 through 7).

Table I - Industry Modules that Mount in the MSIM 20 Power I/O Interface

Module Number				Vendor Name and Address
DC Input	DC Output	AC Input	AC Output	
IDC5	ODC5	IAC5	OAC5	AMF Inc. (Potter & Brumfeld Div.) 200 Richland Creek Drive Princeton, Ind. 47671
IDC5	ODC5	IAC5 IAC5A	OAC5 OAC5A	GORDOS Arkansas Inc. 1000 North Second Street Rogers, Ark. 72756
IDC-01 IDC-11 IDC-21	ODC-01 ODC-11	IAC-01 IAC-11	OAC-01 OAC-11	Guardian California 4050 West Spencer Street Torrance, Cal. 90503
IDC5	ODC5	IAC5 IAC5-A	OAC5 OAC5-A	International Rectifier (Crydom Div.) 1521 East Grand Avenue El Segundo, Cal. 90245
IDC5	ODC5	IAC5 IAC5-A	OAC5 OAC5-A	Opto 22 15461 Springdale St. Huntington Beach, Cal. 92649
IDC5	ODC5	IAC5 IAC5-A	OAC5 OAC5-A	Preferred Electronics, Inc. Main Line Drive, P.O.Box 954 Westfield, Mass. 01086

MRD: When low, MRD indicates a read from memory. If combined with active "N" lines, an output is in progress. (The CDP1802 transfers data between I/O and memory.) If high, combined with active "N" lines, an input is in progress. MRD originates at the microprocessor.

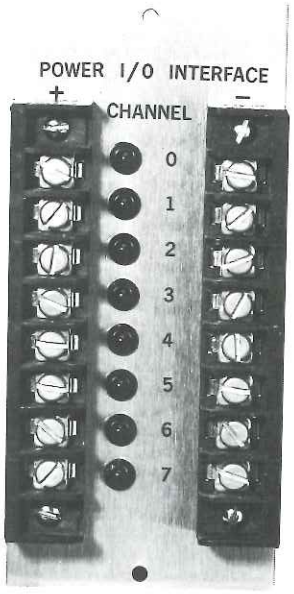
TPA,TPB: An input or output cycle starts at the falling edge of TPA and ends at the falling edge of TPB. It is during this window that "N" lines, MRD, and memory addresses are guaranteed stable. These lines also originate at the microprocessor.

EF1-EF4: These are four flag lines that may be sampled by the microprocessor. They are pulled high by resistors at the microprocessor and are pulled low by "open collector" drivers on I/O boards.

INT: This line, when pulled low, forces the microprocessor to jump to a specific program. It is also an "open collector" line, and it may be disabled internally under software control.

CLEAR: This line is an external input that, when low, resets boards to a known state.

+5V,GND: These lines are the normal system supplies.



Front panel showing barrier strips and LED's.

Table II - Pin Terminals and Signals for the RCA Microboard Universal Backplane

Component Side				Wire Side			
Pin	Mnemonic	Signal Flow	Description	Pin	Mnemonic	Signal Flow	Description
1	DMAI-N	In	DMA Input Request	A	TPA-P *	Out	System Timing Pulse 1
2	DMAO-N	In	DMA Output	B	TPB-P *	Out	System Timing Pulse 2
3	RNU-P	—	Run Utility Request	C	DB0-P *	In/Out	Data Bus
4	INT-N *	In	Interrupt Request	D	DB1-P *	In/Out	Data Bus
5	MRD-N *	Out	Memory Read	E	DB2-P *	In/Out	Data Bus
6	Q-P	Out	Programmed Output Latch	F	DB3-P *	In/Out	Data Bus
7	SC0-P	Out	State Code	H	DB4-P *	In/Out	Data Bus
8	SC1-P	Out	State Code	J	DB5-P *	In/Out	Data Bus
9	CLEAR-N *	In	Clear-Mode Request	K	DB6-P *	In/Out	Data Bus
10	WAIT-N	In	Wait-Mode Request	L	DB7-P *	In/Out	Data Bus
11	−15V	—	Auxiliary Power	M	A0-P	Out	Multiplexed Address Bus
12	SPARE	—	Not Assigned	N	A1-P	Out	Multiplexed Address Bus
13	CLOCK OUT	Out	Clock from CPU Osc.	P	A2-P	Out	Multiplexed Address Bus
14	N0-P *	Out	I/O Primary Address	R	A3-P	Out	Multiplexed Address Bus
15	N1-P *	Out	I/O Primary Address	S	A4-P	Out	Multiplexed Address Bus
16	N2-P *	Out	I/O Primary Address	T	A5-P	Out	Multiplexed Address Bus
17	EF1-N *	In	External Flag	U	A6-P	Out	Multiplexed Address Bus
18	EF2-N *	In	External Flag	V	A7-P	Out	Multiplexed Address Bus
19	EF3-N *	In	External Flag	W	MWR-N	Out	Memory Write Pulse
20	+15V	—	Auxiliary Power	X	EF4-N *	In	External Flag
21	+5 V *	In	+5 V dc	Y	+5 V *	In	+5 V dc
22	GND *	In	Digital Ground	Z	GND *	In	Digital Ground

Note: Signal flow direction is relative to CPU.
Signals marked with an asterisk (*) are used on the MSIM 20.

Power I/O Interface
MSIM 20

Setting I/O Addresses

There are seven possible input or output addresses on a CDP1802A microprocessor. In order to expand to a larger system, a two-level select addressing scheme has been adapted for RCA Microboards. The "OUT 1" (61) instruction has been reserved for outputting an 8-bit I/O address. I/O boards latch and compare that address to that set by links on each board. If they match, they are then free to respond to the remaining I/O instructions (62-67 or 6A-6F). Note that the "INP 1" (69) instruction is reserved so the processor can read back (where implemented) the last 61 instruction.

The eight bits that are output during a 61 instruction are divided into two groups of four. The four lower bits (D0 - D3) are usually used to select system functions such as a terminal or disk and are decoded linearly. The four upper bits (D4 - D7) are used for other I/O (such as this board) and are decoded in a binary manner (16 combinations).

LK1 is used to select the two-level address of the MSIM 20. A stick of push-on connectors is supplied (Amp P/N 531220-3 or equivalent) for setting the address and other links. Note that the end of the connector towards the break-off stick is the end to insert over the pins. See Table III for a list of two-level addresses and the corresponding LK1 connections. The low order bits, bits 0 - 3, are ignored. See Fig. 4 for link locations.

Note that the number of LK1 links installed affects standby current See discussion under system power requirements. Note also that TP1 shown on Fig. 4 is the output of the two-level select circuit. It will be high if the MSIM 20 is selected.

Table III — Two Level I/O Link Assignments for Link LK1

Two Level Address	LK1 Connector Pins			
	1-8	2-7	3-6	4-5
FX	C	C	C	C
EX	C	C	C	O
DX	C	C	O	C
CX	C	C	O	O
BX	C	O	C	C
AX	C	O	C	O
9X	C	O	O	C
8X	C	O	O	O
7X	O	C	C	C
6X	O	C	C	O
5X	O	C	O	C
4X	O	C	O	O
3X	O	O	C	C
2X	O	O	C	O
1X	O	O	O	C
0X	O	O	O	O

Notes: X = Don't Care, C = Closed, O = Open

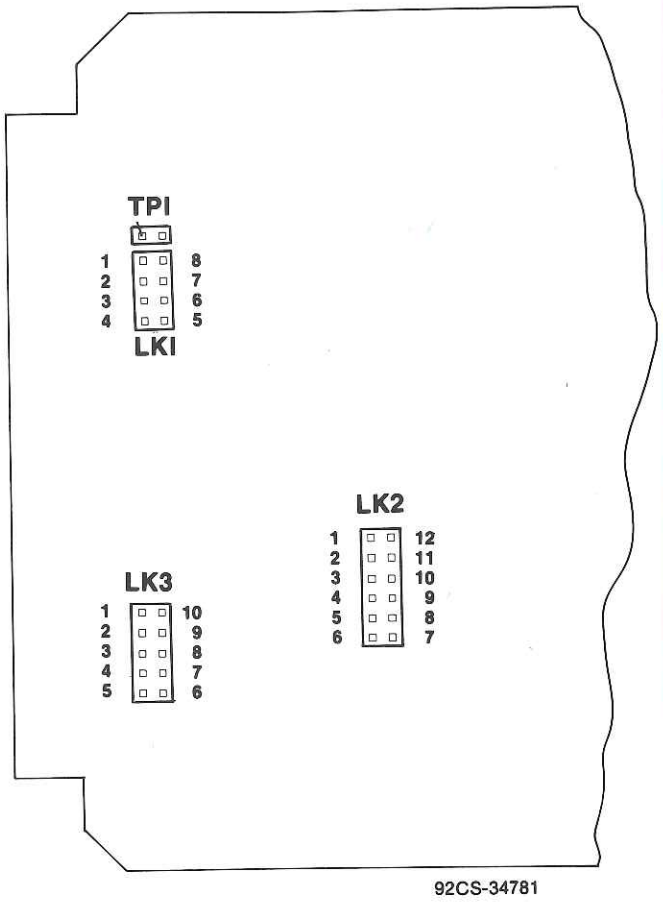


Fig. 4 - Location of links LK1, LK2, LK3, and Test Point TP1.

Once the specific MSIM 20 has been selected, there are six more output (62 - 67) and six more input (6A - 6F) addresses available for use. Link LK2 sets the choice of these addresses.

The MSIM 20 has two output ports: the main output port and the interrupt mask port (discussed later). It has one input port; this port occupies the same address as set for the main output port. If both the main and interrupt ports are to be used, three different pairs of addresses can be set on MSIM 20's occupying the same two-level select group. See Table IV for LK2 connections for this mode.

Table IV - I/O Address Assignments for Link LK2

LK2 Pin Connections	Corresponding I/O Instruction		
	Main Input	Main Output	Interrupt Mask
1 - 12	INP 2 (6A)	OUT 2 (62)	-
2 - 11	-	-	OUT 3 (63)
3 - 10	INP 4 (6C)	OUT 4 (64)	
4 - 9	-	-	OUT 5 (65)
5 - 8	INP 6 (6E)	OUT 6 (66)	
6 - 7	-	-	OUT 7 (67)

Note that the INP 3 (6B), INP 5 (6D), and INP 7 (6F) instructions are not used. If desired, they may be used by other boards occupying the same two-level select group.

If interrupts are not to be used on the MSIM 20, the three Interrupt Mask addresses can be used instead for the Main Input/Output Ports by linking the desired address (3, 5, or 7) and placing a second link across any adjacent higher-numbered LK2 positions (pins 7-8, 8-9, 9-10, etc). Fig. 5 demonstrates LK2 set for a main I/O address of 5. It is important to make sure that no LK3 links are in place because the interrupt circuit will still be active.

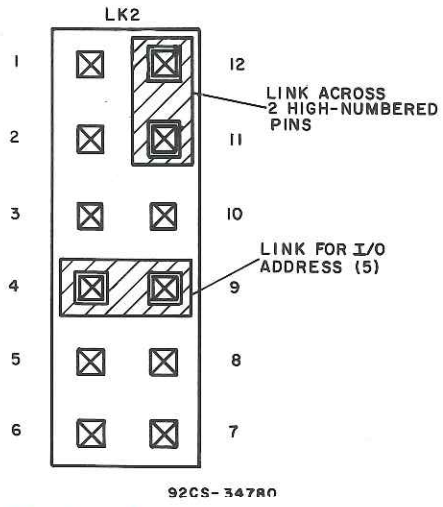


Fig. 5 - Setting of Link LK2 for I/O address of 5.

Setting Flag and Interrupt Links

If the interrupt circuit is to be used, LK3 pins 1 - 10 have to be connected. The interrupt line is an "open collector" line with a pull-up resistor on the CPU board (CDP18S601 - CDP18S610). Interrupts are active low and are given whether the board is two-level selected or not. In conjunction with the interrupt line, one of four flag lines, EF1 - EF4, can also be pulled low by the MSIM 20. These lines, also "open collector," are disabled when the MSIM 20 is not selected. By using a different flag line for each board that is in the same two-level group, the CPU can determine which board gave the interrupt. This subject is discussed further under "Interrupt Control." Table V gives the flag assignments for link LK3.

Table V - Flag Line Connections for Link LK3

LK3 Pin Connections	Flags Enabled
1 - 10	Interrupt
2 - 9	EF1
3 - 8	EF2
4 - 7	EF3
5 - 6	EF4

Mounting and Interfacing I/O Modules

As mentioned earlier, the MSIM 20 accepts any mix of industry-standard isolated I/O modules. In small systems it is likely that input and output modules will be mounted on the same MSIM 20. The modules are simply plugged into the spring socket locations on the board, and screwed down with 4/40 hardware normally supplied with the modules.

CAUTION: Some brands of I/O modules have plastic ears that keep the base from sitting flush with the board. Tightening the mounting screws excessively will deform the board and possibly damage it.

Modules are color coded by function as follows:

White: DC Input
Red: DC Output
Yellow: AC Input
Black: AC Output

The MSIM 20 is preprinted with a white dot at each I/O module location. Red, yellow, and black dots are

Power I/O Interface
MSIM 20

supplied as an aid in marking each socket for the type relay used.

The front panel holds two 8-position barrier blocks marked channels 0 - 7. The left block (marked "+") connects to pin 1 of module positions 0 - 7 on the main board. The right block (marked "-") connects through fuse positions 0 - 7 to pin 2 of module positions 0 - 7. The polarities correspond to those of DC modules and have no meaning for AC modules.

If it is desired to "common up" one side of several modules, jumper strips, part No. J6-N (where N is the number of positions to be shorted together), are available from:

RDI / Reed Devices Inc.
525 Randy Road
Carol Stream, Ill. 60187

The front panel LED'S will be lit if the corresponding input or output channel is on. If an output, a lit LED guarantees that continuity has been established through the internal optical isolator diode of the module, but it does not guarantee that the output circuit is live.

Fuses are clip mounted and are in series with pin 2 of each module. Four-ampere, 250-volt, 5 X 20 mm fuses are provided. A small screwdriver may be inserted between the end of a fuse and its clip to pop it out.

NEVER WORK ON A BOARD WHILE EXTERNAL CONNECTIONS ARE LIVE.

Mounting the MSIM 20

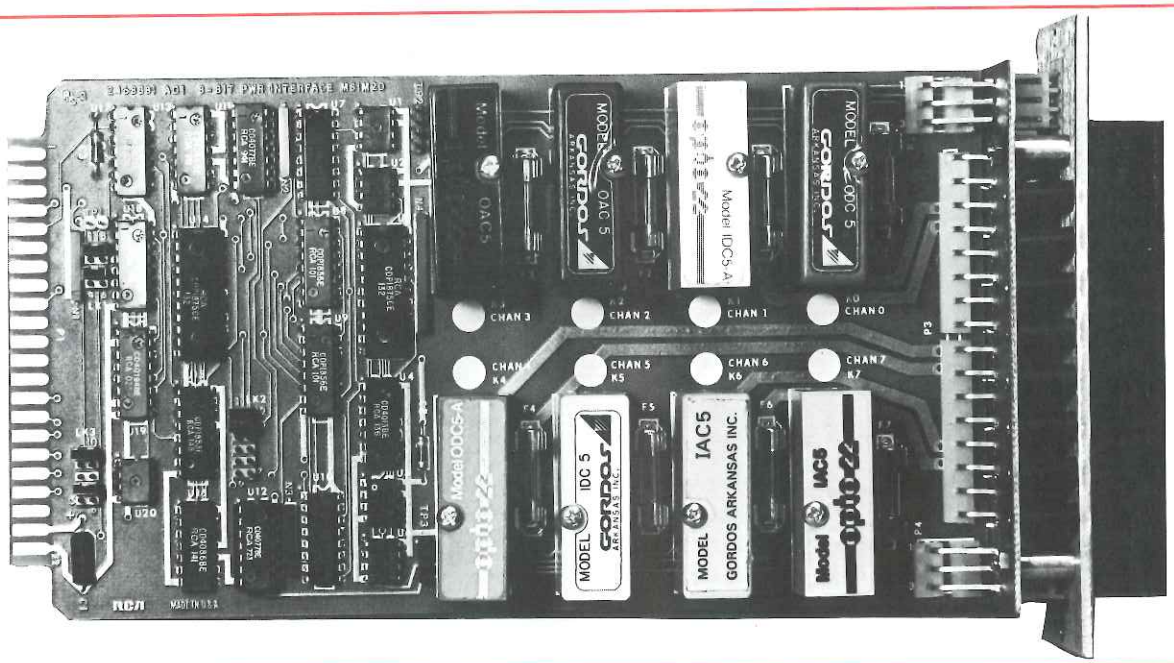
The MSIM 20 is only to be used in a MSI 800 series standard or a MSI 8800 series deluxe Industrial Chassis. It replaces exactly the MSIA 08 blank front panel (standard on the MSI 8800 series chassis), occupying four card slots. The MSIM 20 plugs into the second connector from the right of that space.

CAUTION: Although the rightmost slot will appear free, it should be left free for electrical clearance. The I/O module mounting spring sockets could touch conductive parts (such as crystal cases) of any board inserted there, causing an extreme shock hazard. (With extreme care, a CDP18S604B CPU Microboard can be mounted in this slot, thus allowing a complete eight-channel low-cost control system to fit into a four-card chassis such as the MSI 8804.)

After the front panel of the MSIM 20 is slid into place, it should be secured to the front of the chassis with two 4/40 by 3/8 inch screws. Solid or stranded wires, with or without terminations, can be secured under the captive clamps of the front barrier strips.

CAUTION: It is possible for finely stranded wire to "poke through" small slits in the rear of the barrier strips; care should be taken.

A MSIA 0400 series front panel guard should be used to safeguard the front panel wiring. For 19-inch rack mount applications, a MSIA 10 cable conduit guides and



Representative mix of I/O modules mounted on MSIM 20 Power I/O Interface.

protects wiring to the chassis. See publication **RCA Microboard Industrial Chassis Series,** MB-8, for details.

It is possible, if necessary for fuse or module replacement, to gain access to the board once the front wiring is in place. The wiring to the front panel must not be live and the Microboard system power must be off. The two 4/40 screws securing the front panel should be removed, and the board pulled slightly out of the chassis. With the board grasped securely, the front panel can be pulled off and swung down out of the way. Care must be taken when reconnecting the two parts of the board that the right-angle connectors are inserted properly into their holes; forcing an improperly mated connector will cause damage.

System Power Requirements

The MSIM 20 only requires + 5 volts from the Microboard Universal Backplane. The current required will vary according to how many and what types of active I/O modules are in place. Each "on" output module draws 10 to 12 mA from the logic supply; each "on" input module needs 4 to 6 mA.

The interface circuitry also requires some current. Each LK1 link inserted draws 0.5 mA. In addition, the circuitry typically draws 1 mA when selected, and 0.3 mA when not. With the system in reset (no active backplane signals), no LK1 links, and no "on" input signals, current consumption should drop below 0.1 mA.

Temperature Considerations

Although the MSIM 20 board is rated for a -40 to +85° C operating temperature range, most I/O modules do not meet this specification. Consult the manufacturer for temperature range and derating curves.

The ambient temperature rise inside a chassis is greatly affected by its configuration. A "worst case" test was done to find the maximum expected temperature rise. Eight AC output modules were placed on a MSIM 20 with each carrying 2.5 A continuously. The MSIM 20 was mounted in a MSI 8816 Industrial Chassis with solid top and bottom covers, and a Microboard was placed in the next slot to the left to block internal air circulation. The chassis was mounted on a flat surface. The temperature rise measured was 40° C. With MSIA 0216 perforated covers installed and the chassis raised to provide clearance underneath, the rise measured was 25° C. Placing the chassis vertically so that the MSIM 20 was horizontal increased this rise to 32° C.

Controlling I/O Modules

Before an input module can be read or an output module turned on or off, the MSIM 20 has to be selected (two-level select circuit). An OUT 1 instruction with the upper 4 bits of data matching the address set by LK1 will accomplish this selection. The other INP or OUT instructions as set by LK2 now apply.

Note that if two-level select is not desired (as, perhaps, for a small system), LK1 may be set for an address of 0. When the system is reset, either from power on or manually, the MSIM 20 is selected automatically. The OUT 1 instruction must still be avoided.

If output modules are in place, a data byte written with the selected output instruction controls all channels simultaneously. Every bit position containing a "1" will be on, and those containing a "0", off. The data is latched, and de-selecting the MSIM 20 will not then affect the channels. Note that a system reset signal will turn all output modules off.

If input modules are in place and the board selected, all channels are read simultaneously with the selected input instruction. Again, a "1" in a bit position indicates an "on" channel, and a "0", "off."

If a mix of input and output modules is placed on a board, they may be controlled or read in the same manner. The only constraint is to not write a "1" in a bit position that contains an input module: it will mask the input and show a "1" when read.

An input instruction may be used whether or not there are input modules present. It will show, on channels that are outputs or that have no modules at all, the last bit written to that channel. This feature can be a useful aid to software operation. Fig. 6 diagrams the module interface circuitry.

Interrupt Control

Interrupts can be generated by any selected input on the board changing state in either direction (On to Off, or Off to On). The interrupt mask must first be set to enable the desired channels. The board must be two-level enabled (as in the previous discussion), and a data byte written to the Interrupt Mask with the output instruction set by LK2. A "1" in any bit position enables the corresponding channel to generate interrupts. (After reset, the mask is all 0's.) LK3, pins 1 - 10, must also be in place.

Whenever a board is read, an internal latch stores the state of all channels. If an interrupt-enabled channel then changes state, an (open collector) interrupt signal is ap-

Power I/O Interface
MSIM 20

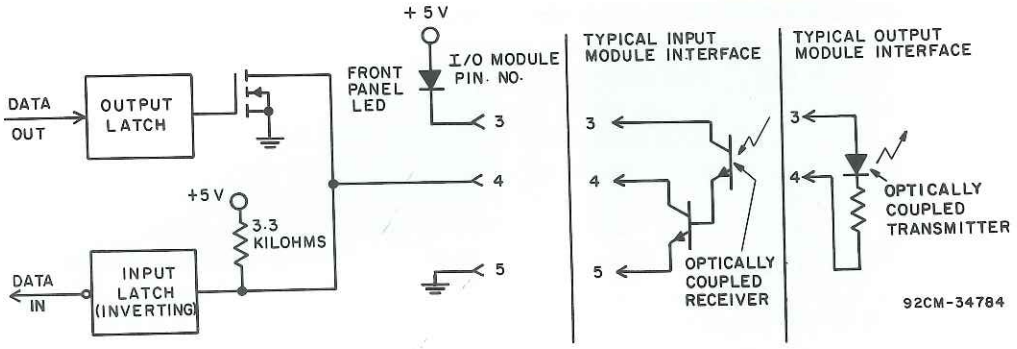


Fig. 6 - Diagrams of the module interface circuitry.

plied to the backplane. (Interrupts are not disabled with two-level select.) The interrupt signal remains until the board is read again (thus loading the latch with the new state), or until the affecting channel resorts back to its former state.

The latch circuit operates early in the read cycle, and the data read by the CPU is actually the output of the latch. This arrangement precludes having different data in the latch (upon which interrupts are based) than that input by the CPU.

The interrupt can also be dropped by changing the interrupt mask, but this change does not actually reset the interrupt request. If the bit is enabled again, the interrupt will still be active.

One of the four flag lines, EF1 - EF4, can also be linked to the interrupt circuit. These lines, however, are only enabled when the MSIM 20 is two-level-selected, and they allow the software to determine which MSIM 20 generated the interrupt. If, for instance, three MSIM 20's were in the same two-level group, they could have three separate flag lines linked up. The software would simply enable that group and check which flag line was active. As an alternate method, the MSIM 20's might be placed in different two-level-select groups, but have the same flag hooked up. The software could then enable one group at a time and check the one flag.

CAUTION: On the CDP18S601, 603, 606, or 608 CPU Microboard, EF3 or EF4 (Link Selected) are not conditioned by two-level-select circuitry. The flag in use on that Microboard should be avoided.

As supplied, the MSIM 20 contains two socketed IC's, U11 and U12. These IC's are CD4077BE Exclusive-NOR gates and generate interrupt request bits when a channel changes state in either direction. U11 controls channels 0 - 3, and U12, channels 4 - 7. The bits are then fed to the masking circuitry.

It is possible to change the MSIM 20 so that interrupts are only generated with "On to Off" or "Off to On" transitions. If CD4081BE AND Gates are inserted, only "On to Off" changes will give interrupts; CD4001BE NOR gates accomplish the opposite.

CAUTION: For the above-modified circuitry to work, the selected channels must be "armed". Arming is accomplished by reading the MSIM 20 at the time when the selected channel is in the "relaxed" state; that is, the state from which a change generates an interrupt.

Parts List

C1=22 μF, 15 V
C2,C3=0.1 μF, 50 V

CR1 - CR8=LED, Dialight 559-0101-001, or equivalent

F0 - F7=fuse, 4 A, 250 V, Bussman No. GMA4, Littlefuse No. 212 004, or equivalent

LK1=connector, 8 pin, double row
LK2=connector, 12 pin, double row
LK3=connector, 10 pin, double row

RN1=resistor network, 10 kilohms, 6 pins
RN2,RN3=resistor network, 3.3 kilohms, 6 pins
RN4=resistor network, 22 kilohms, 10 pins

T1,T2=RDI 6WWV-08, or equivalent

TP1=connector, 2 pin, single row
TP2,TP3=connector, 4 pin, single row

U1,U2,U5,U6,U20=CD40107BE
U3,U14=CDP1875CE
U4=CD4013BE
U7,U10=CD40175BE
U8,U9=CDP1856CE
U11,U12=CD4077BE
U13,U16=CD4086BE
U15=CDP1853CE
U17=CD4011UBE
U18=CD4585BE
U19=CD40194BE

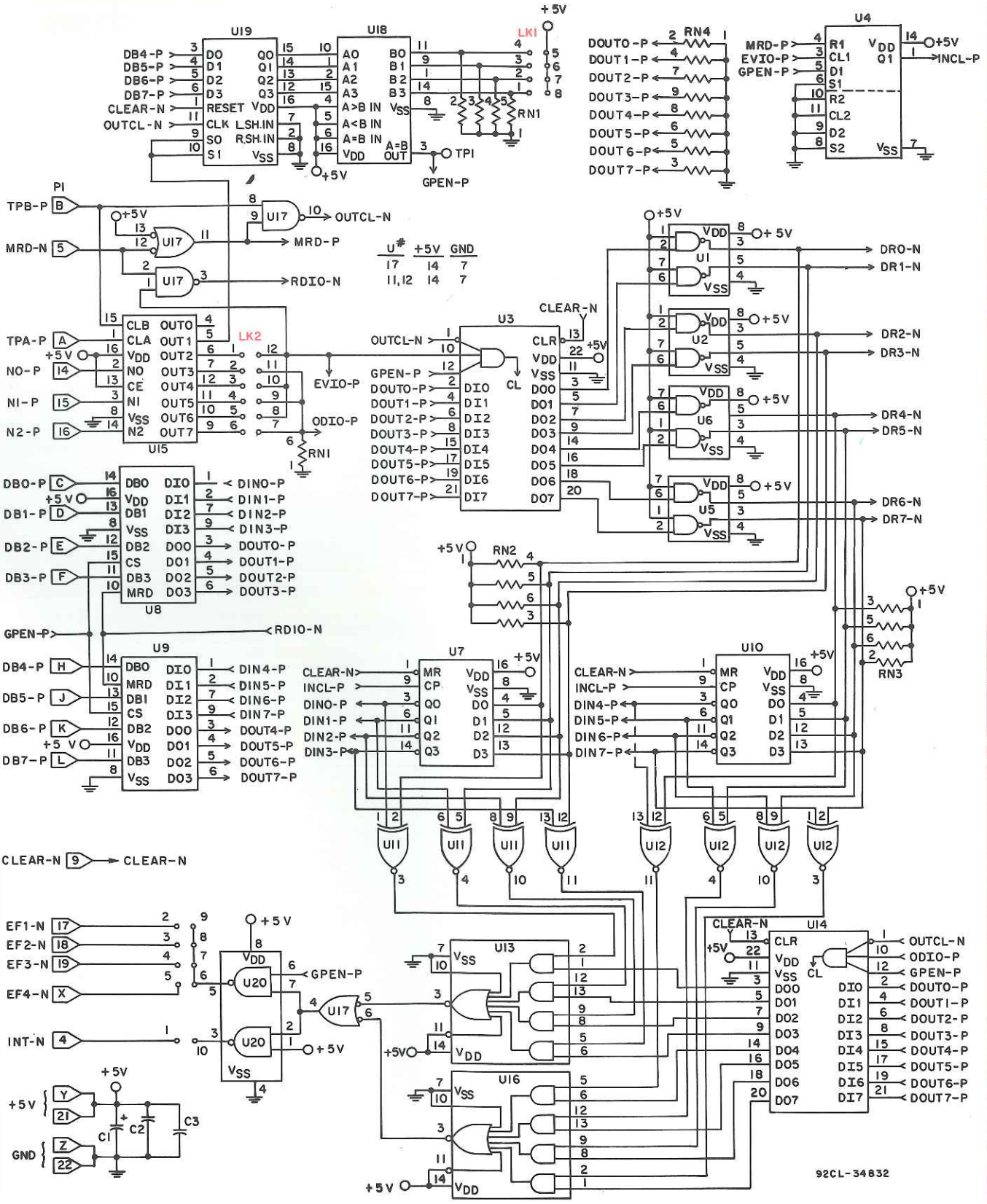


Fig. 7 - Logic diagram of MSIM 20 Power I/O Interface - control section.

Power I/O Interface
MSIM 20

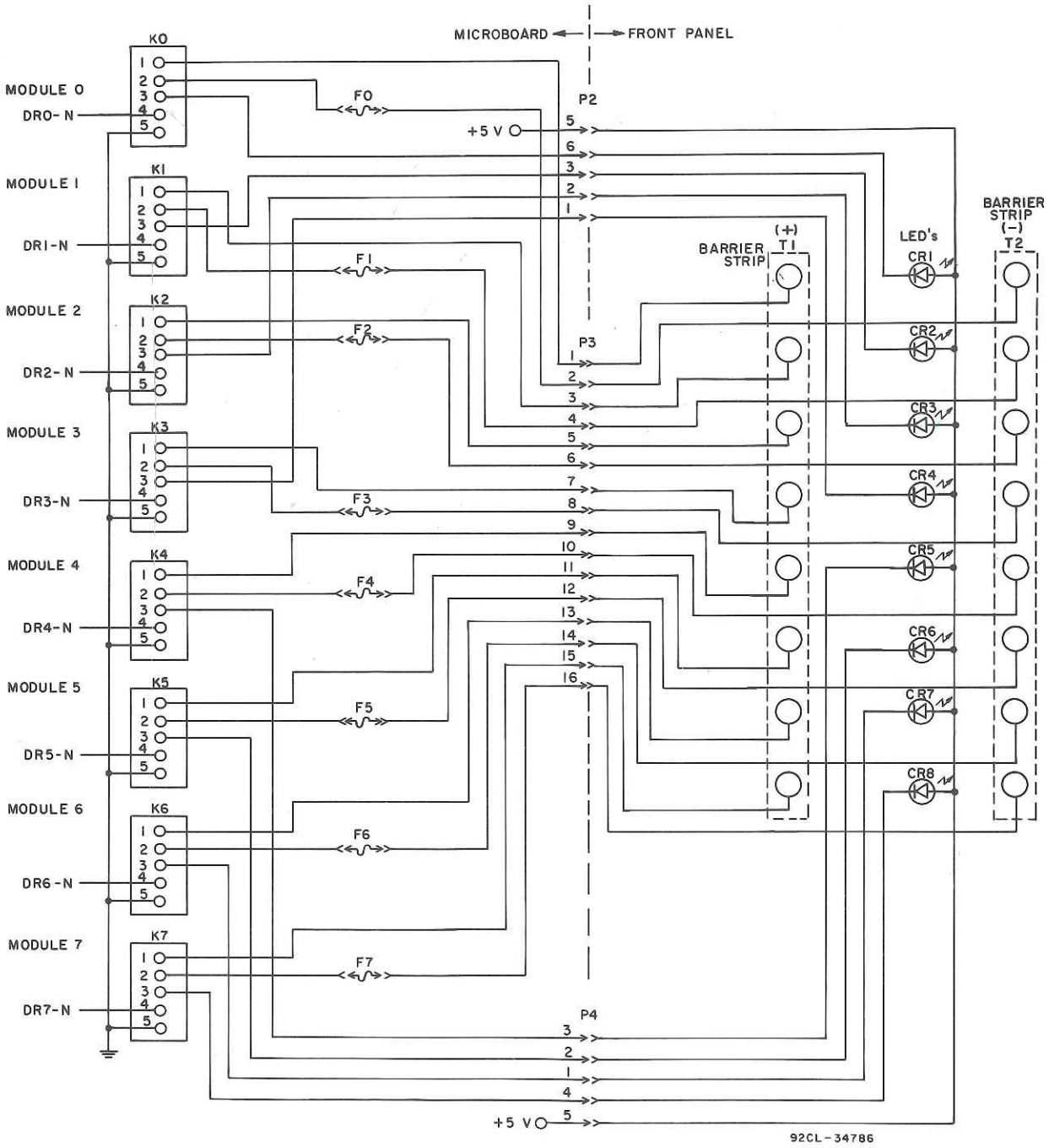


Fig. 8 - Logic diagram of MSIM 20 Power I/O Interface - front panel and module connections.

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