



Viper-N+ 64-Bit CPU Chipset

The OPTi Viper-N+ chipset is the leading solution for PCI-based mobile applications. Viper-N+ features leading edge power management capability and flexibility for Intel® Pentium™ 75/90/100/120 and Cyrix 6x86™ processor based notebooks. The chipset incorporates desktop-like performance features such as L1 and L2 cache support, a full 64-bit DRAM controller and an integrated PCI controller, in a highly integrated three chip set.

In terms of advanced power management, no chipset offers a more effective, comprehensive or flexible feature set, allowing for maximum performance with minimum power consumption for extended battery life. In fact, for typical applications, Viper-N+'s power management unit reduces power consumption by as much as 80%.

Viper-N+ offers the highest level of system integration, enabling the lowest system cost and real estate requirement for Pentium-PCI notebooks. A system without TTL is achievable with synchronous cache. And, PCI offers easy upgradeability to emerging standard interfaces, such as PCMCIA/CardBus and PCI docking stations. Viper-N+ also features an integrated local bus IDE controller to avoid ISA data bus bottlenecks.

OPTi coupled its expertise in mobile technology and PCI-based design to create its second generation 64-bit CPU mobile chipset. The result is Viper-N+, enabling the highest levels of performance, system integration and power management capability available for Pentium PCI-based mobile systems.

System

- 100% PC/AT® compatible
- Supports 3.3V Intel Pentium 75/90/100/120 processors at bus frequencies up to 66MHz
- Supports Cyrix 6x86 processor

DRAM

- Full 64-bit FPM/EDO DRAM controller
 - Supports 2-2-2 EDO pipeline at 66MHz bus speed
 - Supports 5V or 3.3V DRAM without buffers
 - Supports up to 512MB
 - Controls up to 6 banks
 - Post write buffer
- Selectable current drive for DRAM bus

Cache

- L1 Cache supports write-through and write-back modes
- Power managed L2 Cache
 - 64KB-2MB cache
 - Write-back or write-through modes



INNOVATIVE
CHIPSET
SOLUTIONS



- 2-1-1-1 synchronous cache cycles
- 3-1-1-1 pipelined synchronous cache cycles
- Combined tag/dirty SRAM option

ISA/VL/PCI Bus

- Integrated PCI bus with operation up to 33MHz; supports up to three masters
- CLKRUN# support for PCI
- Distributed DMA support (software-based)
- 100% AT-compatible ISA bus; 3.3V or 5V operation, also supports ISA bus masters
- VL bus support (slave only)
- Integrated Local Bus IDE supports four drives, which can be bus masters, modes 4 and 5 supported

Power Management

- Advanced Power Management Unit
- Full CPU System Management Mode (SMM) support
- Full CPU power control through “clock throttling”
- Full system clock control, even CPU clock can be stopped during APM doze mode
- Both hardware and software controlled power management

- Full peripheral power control
- 13 flexible peripheral timers
- Sixteen power control pins
- I/O trapping captures address and data
- Distributed DMA support (software-based)
- Full peripheral activity tracking
- Automatic peripheral power-up/power-down features
- Full suspend current leakage control
- 36 Power Management Interrupt (PMI) sources
- Eight external power management interrupt sources
- Supports SMBASE re-programmability that allows the cache to be maintained during system management mode, avoiding cache fills after returning from SMM
- Proprietary automatic internal pull-up/pull-down resistors activated only when needed to reduce power consumption

Thermal Management

- Advanced Thermal Management Unit

- Internal mechanism tracks CPU activity and initiates cool down mode before CPU temperature reaches a damaging level
- External sensor option

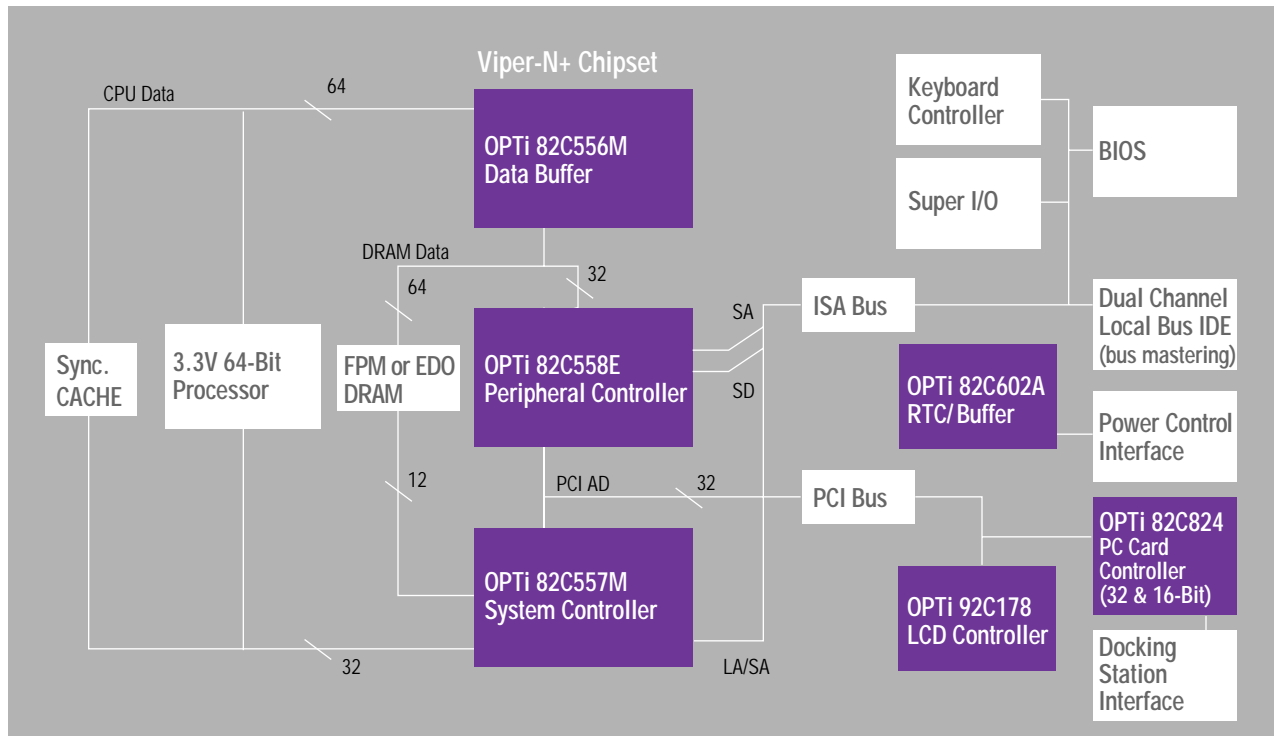
Packaging

- 82C556M Data Buffer
 - 176 pin TQFP (0.5mm pin spacing)
- 82C557M System Controller
 - 208 pin TQFP (0.5mm pin spacing)
- 82C558E Peripheral Controller
 - 208 pin TQFP (0.5mm pin spacing)

82C602A RTC/Buffer Companion Chip

- Integrated Real-Time Clock
- Based on Benchmark Bq3285
- 256 bytes battery-backed memory
- Integrates multiplexing/demultiplexing logic, latches, and buffers
- Eliminates most/all TTL in typical synchronous cache system
- 100 pin TQFP package (0.5mm pin spacing)
- Also available in 100 pin PQFP

System Block Diagram



82C557M System Controller (208 Pin TQFP)

CPU Interface State Machine	DRAM Controller (64-bit)
PCI Controller Host PCI Bridge	
Data Buffer Steering Logic Control	L1/L2 Cache Controller

82C558E Peripheral Controller (208 Pin TQFP)

PCI Data Bus Buffering & PCI AT Bus Interface	Arbitration Logic 8042 Emulation Reset/Init Gen.
Power Management Unit (PMU)	Integrated Peripheral Controller
Dual Channel Local Bus IDE	AT-Bus, VL-Bus Controller and ATCLK Generator
	AT Refresh Generator

82C556M Data Buffer (176 Pin TQFP)

64-Bit Data Bus Interface	Parity Generation and Detection Circuitry
Data Buffer Steering Logic	

About OPTi

Founded in 1989, OPTi is a leading supplier of core logic and multimedia chipsets to manufacturers of desktop and mobile computer products worldwide. OPTi's innovative chipset solutions enable our customers to get to market quickly with quality, state of the art products. In 1995, we shipped

more than eleven million chipsets to leading personal computer and board manufacturers worldwide.

Our headquarters are located in Milpitas, California and our stock is traded on NASDAQ under the symbol OPTi.

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