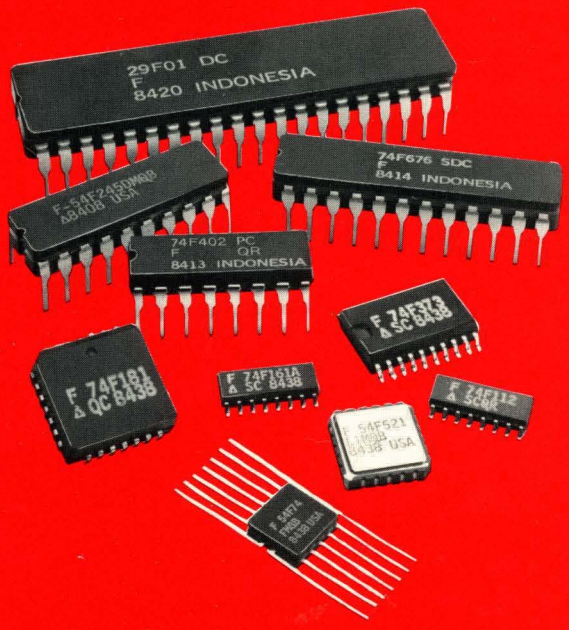

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Fairchild Advanced Schottky TTL

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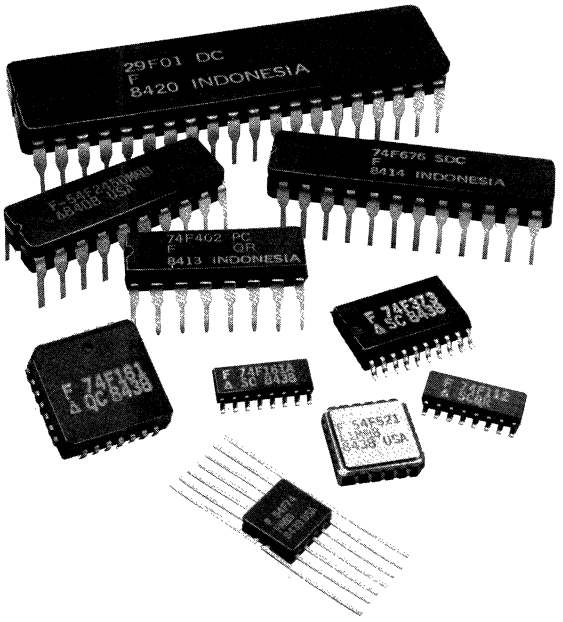

FAST™

Fairchild Advanced Schottky TTL

333 Western Ave. • So. Portland, Maine 04106
207/775-8700 • TWX 710-221-1980

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Introduction

Fairchild Advanced Schottky TTL, FAST™, is a family of TTL circuits that exhibits a combination of performance and efficiency unapproached by any other TTL family. Made with the proven Isoplanar process, 54F/74F circuits offer the switching speed and output drive capability of Schottky TTL, with superior noise margins and only one-fourth the power consumption.

Section 1 Product Index and Selection Guide
Lists 54F/74F circuits currently available, in design or planned. The Selection Guide groups the circuits by function.

Section 2 Circuit Characteristics
Discusses FAST technology, circuit configurations and characteristics.

Section 3 Ratings, Specifications and Waveforms
Contains common ratings and specifications for FAST devices, as well as AC test load and waveforms.

Section 4 Data Sheets
Contains data sheets for currently available and pending new products.

Section 5 Ordering Information and Package Outlines
Explains simplified purchasing code which identifies device type, package type and temperature range. Contains detailed physical dimension drawings for each package.

Section 6 Field Sales Offices, Representatives and Distributor Locations

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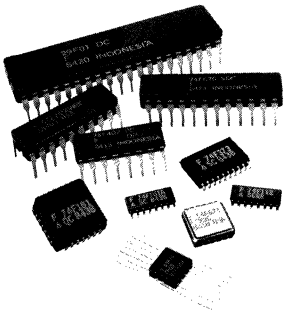

Literature Classification

PRELIMINARY

Preliminary product data sheet: This document contains specifications that are subject to change without notice. Fairchild reserves the right to make changes at any time in order to provide the best product possible.

ADVANCE INFORMATION

Advance Information-Packages: The material described is in the formative or design phase. Specifications may be changed in any manner without notice.

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Product Index and Selection Guide

1

Product Index

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Selection Guide

Gates

Function	Device	Page No.
NAND		
Quad 2-Input NAND	54F/74F00	4-3
Triple 3-Input NAND	54F/74F10	4-7
Dual 4-Input NAND Schmitt Trigger	54F/74F13	4-9
Dual 4-Input NAND	54F/74F20	4-13
Quad 2-Input Positive NAND Buffer	54F/74F37	4-15
Quad 2-Input NAND Buffer (OC)	54F/74F38	4-17
Dual 4-Input Positive NAND Buffer	54F/74F40	4-19
Quad 2-Input Positive NAND Schmitt Trigger	54F/74F132	4-43
AND		
Quad 2-Input AND	54F/74F08	4-6
Triple 3-Input AND	54F/74F11	4-8
OR/NOR/Exclusive-OR		
Quad 2-Input NOR	54F/74F02	4-4
Quad 2-Input OR	54F/74F32	4-14
Quad 2-Input Exclusive-OR	54F/74F86	4-30
Invert/AND-OR-Invert		
Hex Inverter	54F/74F04	4-5
Hex Schmitt Trigger Inverter	54F/74F14	4-11
AND-OR-Invert	54F/74F64	4-21

Dual Edge-Triggered Flip-Flops

Function	Device	Clock Edge	Direct Set	Direct Clear	Page No.
Dual D	54F/74F74	⌜	Yes	Yes	4-22
Dual $J\overline{K}$	54F/74F109	⌜	Yes	Yes	4-31
Dual JK	54F/74F112	⌞	Yes	Yes	4-34
Dual JK	54F/74F113	⌞	Yes	No	4-37
Dual JK	54F/74F114	⌞	Yes	Yes	4-40

Selection Guide (cont'd)

Multiple Flip-Flops

Function	Device	Clock Inputs	Master Reset	Broadside Pinout	3-State Outputs	Page No.
Hex D Flip-Flop	54F/74F174	1(⎍)	Yes			4-93
Quad D Flip-Flop	54F/74F175	1(⎍)	Yes			4-96
Octal D Flip-Flop	54F/74F273	1(⎍)	Yes			4-186
Octal D Flip-Flop	54F/74F374	1(⎍)			Yes	4-232
Octal D Flip-Flop	54F/74F377	1(⎍)				4-235
Hex D Flip-Flop	54F/74F378	1(⎍)				4-238
Quad D Flip-Flop	54F/74F379	1(⎍)				4-241
Octal D Flip-Flop	54F/74F534	1(⎍)			Yes	4-393
Octal D Flip-Flop	54F/74F564	1(⎍)		Yes	Yes	4-448
Octal D Flip-Flop	54F/74F574	1(⎍)		Yes	Yes	4-461
10-Bit D Flip-Flop	54F/74F821	1(⎍)	Yes	Yes	Yes	4-544
9-Bit D Flip-Flop	54F/74F823	1(⎍)	Yes	Yes	Yes	4-548
Octal Flip-Flop	54F/74F825	1(⎍)	Yes	Yes	Yes	4-552

Registers

Function	Device	Clock Inputs	Page No.
Quad 2-Port Register	54F/74F398	1(⎍)	4-268
Quad 2-Port Register	54F/74F399	1(⎍)	4-268
Data Access Register	54F/74F402	1(⎍)	4-277
Register Stack	54F/74F410	1(⎍)	4-309
Octal Register	54F/74F604	1(⎍)	4-477

Latches

Function	Device	Enable Inputs (Level)	Broadside Pinout	Transparent	3-State Outputs	Page No.
Dual Quad Addressable Latch	54F/74F256	1(L)				4-166
Octal Addressable Latch	54F/74F259	1(L)				4-177
Octal Latch	54F/74F373	1(H)			Yes	4-229
Multimode Octal Latch	54F/74F412				Yes	4-322
Multimode Octal Latch	54F/74F432				Yes	4-342
Octal D Latch	54F/74F533	1(H)			Yes	4-391
Octal D Latch	54F/74F563	1(H)	Yes		Yes	4-445
Octal D Latch	54F/74F573	1(H)	Yes		Yes	4-458
10-Bit D Latch	54F/74F841	1(L)	Yes	Yes	Yes	4-559
9-Bit D Latch	54F/74F843	1(L)	Yes	Yes	Yes	4-562
Octal D Latch	54F/74F845	3(L)	Yes	Yes	Yes	4-566

Selection Guide (cont'd)

Counters

Function	Device	Parallel Entry	Reset	U/D	3-State Outputs	Page No.
4-Bit BCD Decade	54F/74F160A	S	A			4-75
4-Bit Binary	54F/74F161A	S	A			4-80
4-Bit BCD Decade	54F/74F162A	S	S			4-75
4-Bit Binary	54F/74F163A	S	S			4-80
4-Bit BCD Decade	54F/74F168	S		Yes		4-88
4-Bit Binary	54F/74F169	S		Yes		4-88
4-Bit BCD Decade	54F/74F190	A		Yes		4-112
4-Bit Binary	54F/74F191	A		Yes		4-117
4-Bit BCD Decade	54F/74F192	A	A	Yes		4-122
4-Bit Binary	54F/74F193	A	A	Yes		4-127
8-Bit Binary	54F/74F269	S		Yes		4-182
16-Stage Programmable	54F/74F525		A			4-386
4-Bit BCD Decade	54F/74F568	S	S/A	Yes	Yes	4-451
4-Bit Binary	54F/74F569	S	S/A		Yes	4-451
8-Bit Binary	54F/74F579	S		Yes		4-464
8-Bit Binary	54F/74F779	S		Yes		4-536

S = Synchronous
A = Asynchronous

Shift Registers

Function	Device	No. of Bits	Serial Entry	Parallel Inputs	3-State Outputs	Page No.
Shift Right, Serial-In, Parallel-Out	54F/74F164	8	2			4-85
Bidirectional, Serial/Parallel-In, Serial/Parallel-Out	54F/74F194	4	2	Yes		4-132
Shift Register	54F/74F195	4	2	Yes		4-135
Octal Shift/Storage Register	54F/74F299	8	2		Yes	4-199
Octal Shift/Storage Register	54F/74F322	8	2		Yes	4-204
Octal Shift/Storage Register	54F/74F323	8	2		Yes	4-209
Universal Shift Register	54F/74F395	4	1	Yes	Yes	4-264
Serial-In, Serial/Parallel-Out	54F/74F673A	16	1		Yes	4-517
Serial/Parallel-In, Serial-Out	54F/74F674	16	1	Yes	Yes	4-522
Serial-In, Serial/Parallel-Out	54F/74F675A	16	1			4-529
Serial/Parallel-In, Serial-Out	54F/74F676	16	1	Yes		4-533

Selection Guide (cont'd)

Buffers/Line Drivers

Function	Device	Enable Inputs (Level)	Inverting/ Noninverting	Broadside Pinout	Page No.
Octal Buffer/Line Driver	54F/74F240	2(L)	I		4-152
Octal Buffer/Line Driver	54F/74F241	1(L) & 1(H)	N		4-152
Octal Buffer/Line Driver	54F/74F244	2(L)	N		4-152
Hex Buffer	54F/74F365	2(L)	N		4-225
Hex Inverter	54F/74F366	2(L)	I		4-227
Hex Buffer	54F/74F367	2(L)	N		4-225
Hex Inverter	54F/74F368	2(L)	I		4-227
Octal Buffer/Line Driver	54F/74F540	2(L)	I	Yes	4-408
Octal Buffer/Line Driver	54F/74F541	1(L) & 1(H)	N	Yes	4-408
Octal Buffer	54F/74F655	3(L)	N		4-510
Octal Buffer	54F/74F656	3(L)	N		4-510
10-Bit Buffer/Line Driver	54F/74F827	2(L)	N	Yes	4-556
10-Bit Buffer/Line Driver	54F/74F828	2(L)	I	Yes	4-556

Transceivers

Function	Device	Registered	Enable Inputs (Level)	3-State Output	Features	Page No.
Quad Bus Transceiver	54F/74F242		1(L) & 1(H)	Yes		4-155
Quad Bus Transceiver	54F/74F243		1(L) & 1(H)	Yes		4-155
Octal Bus Transceiver	54F/74F245		1(L)	Yes		4-158
Octal Registered Transceiver	54F/74F543	Yes	2(L)	Yes		4-410
Octal Registered Transceiver	54F/74F544	Yes	2(L)	Yes		4-413
Octal Bus Transceiver	54F/74F545		1(L)	Yes		4-416
Octal Registered Transceiver	54F/74F550	Yes	2(L)	Yes	Status Flags	4-427
Octal Registered Transceiver	54F/74F551	Yes	2(L)	Yes	Status Flags	4-427
Octal Registered Transceiver	54F/74F552	Yes	1(L)		Parity & Flag	4-432
Octal Transceiver	54F/74F588		1(L)	Yes	GPIB Compatible	4-474
Octal Bus Transceiver	54F/74F620		2(H)	Yes		4-487
Octal Bus Transceiver	54F/74F623		2(H)	Yes		4-487
Octal Bus Transceiver	54F/74F646		1(L) & 1(H)	Yes	w/Register	4-506
Octal Bus Transceiver	54F/74F648		1(L) & 1(H)	Yes	w/Register	4-506
Octal Bus Transceiver	54F/74F657		1(L) & 1(H)		Parity	4-513
Octal Registered Transceiver	29F52	Yes	2(L)	Yes		4-591
Octal Registered Transceiver	29F53	Yes	2(L)	Yes		4-591

Selection Guide (cont'd)

Multiplexers

Function	Device	Enable Inputs (Level)	True Output	Complement Output	Page No.
8-Input	54F/74F151	1(L)	Yes	Yes	4-63
Dual 4-Input	54F/74F153	2(L)	Yes	No	4-66
Quad 2-Input	54F/74F157	1(L)	Yes	No	4-69
Quad 2-Input	54F/74F158	1(L)	No	Yes	4-72
8-Input	54F/74F251	1(L)	Yes	Yes	4-160
Dual 4-Input	54F/74F253	2(L)	Yes	No	4-163
Quad 2-Input	54F/74F257	1(L)	Yes	No	4-170
Quad 2-Input	54F/74F258	1(L)	No	Yes	4-174
Quad 2-Input w/Storage	54F/74F298		Yes	No	4-196
4-Input w/Shift	54F/74F350	1(L)	Yes	No	4-213
Dual 4-Input	54F/74F352	2(L)	No	Yes	4-218
Dual 4-Input	54F/74F353	2(L)	No	Yes	4-222
Quad 2-Input w/Flip-Flop	54F/74F398		Yes	Yes	4-268
Quad 2-Input w/Flip-Flop	54F/74F399		Yes	No	4-268

Decoders/Demultiplexers

Function	Device	Address Inputs	Active LOW Enable	Active HIGH Enable	Active LOW Output Enable	Active LOW Outputs	Active HIGH Outputs	Page No.
1-of-8 Decoder/Demultiplexer	54F/74F138	3	2	1		8		4-45
Dual 1-of-4 Decoder	54F/74F139	2 & 2	1 & 1			4 & 4		4-49
1-of-10 Decoder	54F/74F537	4	1	1	1		10	4-396
1-of-8 Decoder	54F/74F538	3	2	2	2		8	4-400
Dual 1-of-4 Decoder	54F/74F539	2 & 2	1 & 1		1 & 1		4 & 4	4-404
Octal Decoder/Demultiplexer w/Latches	54F/74F547	3	1	2		8		4-419
Octal Decoder/Demultiplexer	54F/74F548	3	2	2		8		4-423

Adders

Function	Device	Master Reset	Carry Lookahead	Page No.
Binary Full Adder	54F/74F283		Yes	4-192
Quad Adder/Subtractor	54F/74F385	Yes		4-260
BCD Adder	54F/74F583		Yes	4-471

Selection Guide (cont'd)

Multipliers

Function	Device	Serial/ Parallel	Latches	3-State Outputs	Page No.
8-Bit Multiplier	54F/74F384	S/P			4-254
8x8-Bit Multiplier	54F/74F557	P	Yes	Yes	4-438
8x8-Bit Multiplier	54F/74F558	P		Yes	4-438
8-Bit Multiplier w/Adder/Subtractor	54F/74F784	S/P			4-540

Comparators

Function	Device	Features	Page No.
4-Bit Magnitude Comparator	54F/74F85		4-25
Octal Comparator	54F/74F521	Expandable	4-375
8-Bit Register Comparator	54F/74F524	Expandable, Registered	4-378

Divider

Function	Device	Features	Page No.
16-Stage Programmable Counter/Divider	54F/74F525	Crystal Oscillator	4-386

Parity Generator/Checker

Function	Device	Features	Page No.
Parity Generator/Checker	54F/74F280	Odd/Even Outputs 9-Bits In	4-189

ALUs

Function	Device	No. of Bits	Arithmetic Functions	Logic Functions	Features	Page No.
Arithmetic Logic Unit	54F/74F181	4	16	16	Carry Generate/ Propagate Output	4-99
Arithmetic Logic Unit	54F/74F381	4	3	3	Carry Generate/ Propagate Outputs	4-244
Arithmetic Logic Unit	54F/74F382	4	3	3	Ripple Carry Expansion	4-249
BCD Adder/Subtractor	54F/74F582	4	2		Lookahead & Ripple Carry Expansion	4-468

Selection Guide (cont'd)

ALU Support

Function	Device	No. of Bits	Features	Page No.
Carry Lookahead	54F/74F182	4	Carry Lookahead Generator for 4 ALUs	4-104
Shifter	54F/74F350	4	Expandable Shifter	4-213

FIFOs

Function	Device	Input	Output	Page No.
16x4 FIFO	54F/74F403	Serial/Parallel	Serial/Parallel	4-285
64x4 FIFO	54F/74F413	Parallel	Parallel	4-327
64x4 FIFO	54F/74F433	Serial/Parallel	Serial/Parallel	4-347

Memories

Function	Device	Latch	3-State Outputs	Page No.
16x4 RAM	54F/74F189		Yes	4-109
16x9 RAM	54F/74F211	Yes	Yes	4-138
16x9 RAM	54F/74F212		Yes	4-142
16x12 RAM	54F/74F213		Yes	4-146
16x4 RAM	54F/74F219		Yes	4-149

Memory Support

Function	Device	Latched	3-State Outputs	Page No.
Data Access Register	54F/74F407			4-302
Register Stack	54F/74F410			4-309
FIFO RAM Controller	54F/74F411			4-313
32-Bit Error Detection & Correction	54F/74F418		Yes	4-331
Parallel Error Detection & Correction	54F/74F420			4-337
Memory Mapper	54F/74F610	Yes	Yes	4-481
Memory Mapper	54F/74F612		Yes	4-481
16-Bit Error Detection & Correction	54F/74F630		Yes	4-490
52-Bit Error Detection & Correction	54F/74F632	Yes	Yes	4-495
Dynamic RAM Controller	29F68			4-595

Selection Guide (cont'd)

Bit Slice and Support

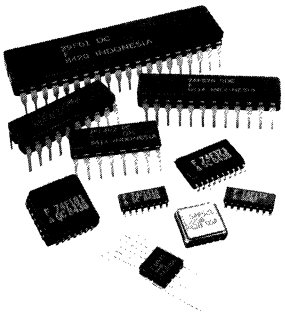
Function	Device	Features	Page No.
Arithmetic Logic Unit	29F01	4-Bit Microprocessor Slice w/16x4 RAM 8-Function ALU	4-570
Controller	29F10	Microprocessor Controller; 4K Addressing & 5-Deep LIFO Stack	4-580

Microprocessor Support

Function	Device	Page No.
Priority Interrupt Controller	54F/74F146	4-53
8-Bit Priority Encoder	54F/74F148	4-58

Specialized LSI

Function	Device	Features	Page No.
CRC Generator/Checker	54F/74F401	Polynomial Length-16	4-271
Expandable CRC Generator/Checker	54F/74F402	Polynomial Length-64	4-277
6-Bit A/D Flash Converter	54F/74F500		4-365
8-Bit A/D Converter	54F/74F505	Successive Approximation	4-369



FAST Technology

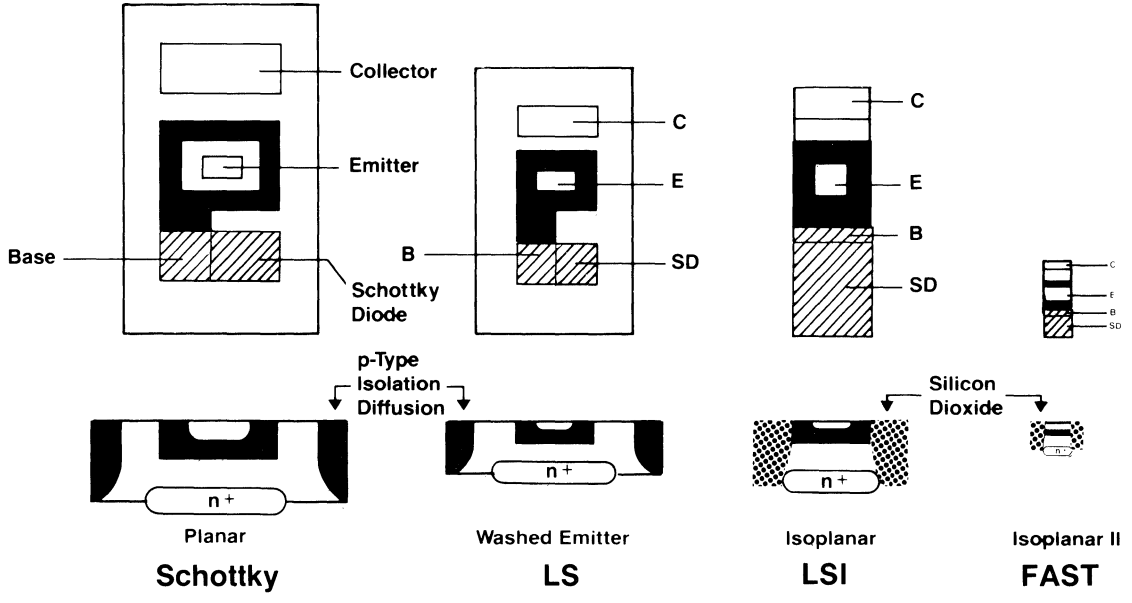
FAST is an acronym for Fairchild Advanced Schottky TTL. FAST circuits are made with the advanced Isoplanar II process, which produces transistors with very high, well-controlled switching speeds, extremely small parasitic capacitances and f_T in excess of 5 GHz. Isoplanar is an established Fairchild process, used for years in the manufacture of bipolar memories, CMOS, subanosecond ECL and I^3L^{TM} (Isoplanar Integrated Injection Logic) LSI devices.

In the Isoplanar process, components are isolated by a selectively grown thick oxide rather than the P+ isolation region used in the Planar process. Since this oxide needs no separation from the base-collector regions, component and chip sizes are substantially reduced. The base and emitter ends terminate in the oxide wall; masks can thus overlap the device area into the isolation oxide. This overlap feature eliminates the extremely close tolerances normally required for base and emitter masking, and the standard photolithographic processes can be used.

Figure 2-1 shows the relative size of phase-splitter transistors (Q2 in Figure 2-3) used in Schottky, Low Power Schottky and FAST circuits. The LS-TTL transistor is smaller than that of S-TTL because of process refinements, shallower diffusions and smaller operating currents. The relative size of the FAST and FAST LSI transistors illustrate the reduction afforded by the Isoplanar process. This in turn reduces junction capacitances, while the use of oxide isolation reduces sidewall capacitance. The end result of these reductions is an increase in frequency response by a factor of three or more. Figure 2-2 shows the frequency response of two sizes of transistors made with the Isoplanar II process. Because they have modest, well-defined loads and thus can use smaller, faster transistors, internal gates of MSI devices are faster than SSI gates such as the 'F00 or 'F02. SSI gates, on the other hand, are designed to have high output drive capability and thus use larger transistors.

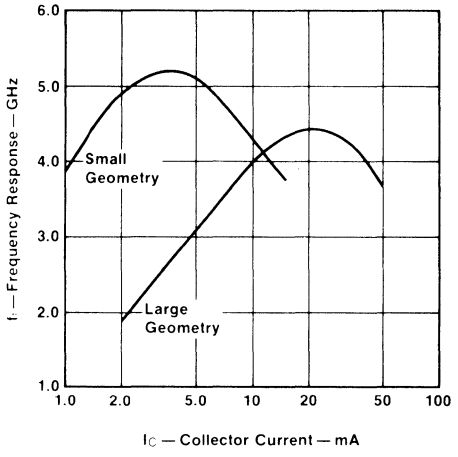
As is the case with other modern LSI processes, the shallower diffusions and thinner oxides make

Fig. 2-1 Relative Transistor Sizes in Various TTL Families



FAST devices more susceptible to damage from electrostatic discharge than are devices of earlier TTL families. Users should take the usual precautions when handling FAST devices: avoid placing them on non-conductive plastic surfaces or in plastic bags, make sure test equipment and jigs are grounded, individuals should be grounded before handling the devices, etc.

Fig. 2-2 Isoplanar Transistor Frequency Response

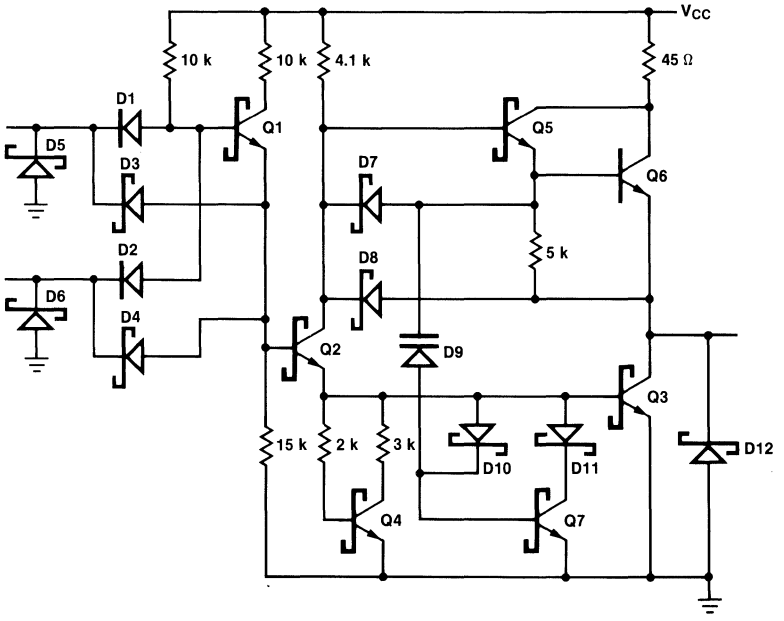


FAST Circuitry

The 2-input NAND gate, shown in Figure 2-3, has three stages of gain (Q1, Q2, Q3) instead of two stages as in other TTL families. This raises the input threshold voltage and increases the output drive. The higher threshold makes it possible to use PN diodes for the input AND function (D1 and D2) and still achieve an input threshold of 1.5 V. The capacitance of these diodes is comparatively low, which results in improved AC noise immunity. The effect of the threshold adjustment can be seen in the voltage transfer characteristics of Figures 2-4, 2-5 and 2-6. At 25°C (Figure 2-5) the FAST circuit threshold is nearly centered between the 0.8 V and 2.0 V limits specified for TTL circuits. This gives a better balance between the HIGH- and LOW-state noise margins. The +125°C characteristics (Figure 2-6) show that the FAST circuit threshold is comfortably above the 0.8 V specification, more so than in S-TTL or LS-TTL circuits. At -55°C, the FAST circuit threshold is still well below the 2.0 V specification, as shown in Figure 2-4.

FAST circuits contain several speed-up diodes to help discharge internal capacitances. Referring again to Figure 2-3, when a HIGH-to-LOW transition occurs at the D1 input, for example, Schottky diode D3 acts as a low-resistance path to discharge the several parasitic capacitances connected to the base of Q2. This effect only comes

Fig. 2-3 Basic FAST Gate Schematic



into play, however, as the input signal falls below about 1.2 V; D3 does not act as an entry path for negative spikes superimposed on a HIGH input level. When Q2 turns on and its collector voltage falls, D7 provides a discharge path for capacitance at the base of Q6. Whereas D3, D4 and D7 enhance switching speed by helping to discharge internal nodes, D8 contributes to the ability of a FAST circuit to rapidly discharge load capacitance. Part of the charge stored in load capacitance passes through D8 and Q2 to increase the base current of Q3 and increase Q3's current sinking capability during the HIGH-to-LOW output voltage transition.

In addition to the 2K-Q4-3K squaring network, which is standard for Schottky-clamped TTL circuits, FAST circuits contain a network D9-D10-D11-Q7 whose purpose is to provide a momentary low impedance at the base of Q3 during an output LOW-to-HIGH transition. The rising voltage at the emitter of Q5 causes displacement current to flow through varactor diode D9 and momentarily turn on Q7, which in turn pulls down the base of Q3 and absorbs the displacement current that flows through the collector-base capacitance (not shown) of Q3 when the output voltage rises. Without the D9-Q7 network, the displacement current through the collector-base capacitance acts as base current, tending to prolong the turn-off of Q3 and allow current to flow from Q6 to ground through Q3.

The collector-base capacitance of Q3, although small, is effectively multiplied by the voltage gain of Q3. This phenomenon, first identified many years ago with vacuum tube triodes, is called the Miller effect. Thus the D9-Q7 network is familiarly called the 'Miller killer' circuit and its use improves the output rise time and minimizes power consumption during repetitive switching at high frequencies. Diode D10 completes the discharge path for D9 through D7 when Q2 turns on. D11 limits how low Q7 pulls down the base of Q3 to a level adequate for the intended purpose, without sacrificing turn-on speed when a circuit is cycled rapidly.

Also shown in Figure 2-3 is a clamp diode, D12, at the output. This diode limits negative voltage excursions due to parasitic coupling in signal lines or transmission line effects.

The Schottky clamping diodes built into the transistors prevent saturation, thereby eliminating storage time as a factor in switching speed. Similarly, the speed-up diodes tend to minimize the impact of other variables on switching speed. The overall effect is to minimize variation in switching speed of FAST circuits with variations in supply voltage and ambient temperature (Figures 2-7 and 2-8). Propagation delay is specified not only under nominal supply voltage and temperature conditions, but also over the recommended operating range of V_{CC} and T_A for both military and commercial grade devices.

The internal switching speed of a logic circuit is only one aspect of the circuit's suitability for high-speed operation at the system or subsystem level; the other aspect is the ability of the circuit to drive load capacitance. FAST circuit outputs are structured to sink at least 20 mA in the LOW state, the

Fig. 2-4 Transfer Functions at Low Temperature

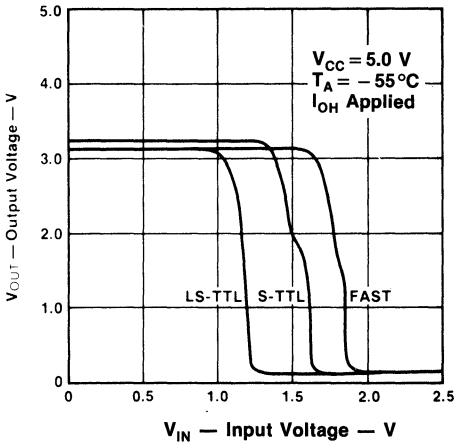
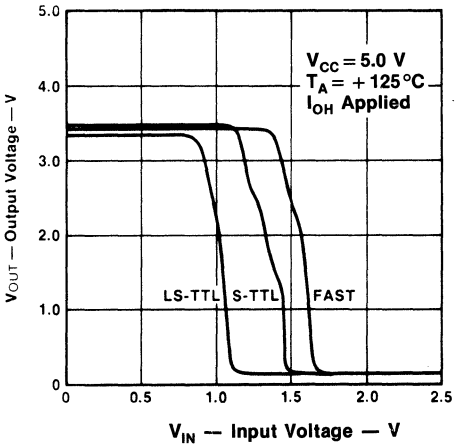


Fig. 2-5 Transfer Functions at Room Temperature



same as S-TTL. This capability plus the effect of the aforementioned feedback through D8 assures that the circuit can rapidly discharge capacitance. During a LOW-to-HIGH transition, the pull-up current is limited by the 45 Ω resistor, versus 55 Ω for S-TTL. Therefore, FAST circuits are inherently more capable than S-TTL of charging load capacitance.

Figure 2-9 shows the effects of load capacitance on propagation delays of FAST, S-TTL and LS-TTL NAND gates. The curves show that FAST gates are not only faster than those of earlier families, but also are less affected by capacitance and exhibit less skew between the LOW-to-HIGH and HIGH-to-LOW delays. These improved characteristics offered by FAST circuits make it easier to predict system performance early in the design phase, before loading details are precisely known. The curves show that the skew between HIGH-to-LOW and LOW-to-HIGH delays for the FAST gate is only about 0.5 ns, over a broad range of load capacitance, whereas the skew for the S-TTL gate is 1 ns or greater, depending on loading.

Output Characteristics

Figure 2-10 shows the current-voltage characteristics of a FAST gate with the pull-down transistor Q3 turned on. These curves illustrate

Fig. 2-6 Transfer Functions at High Temperature

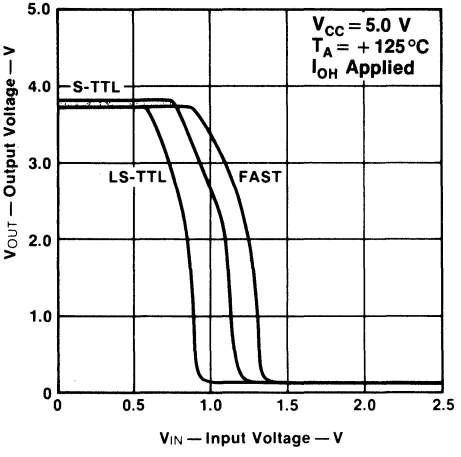


Fig. 2-7 Propagation Delay vs V_{CC}

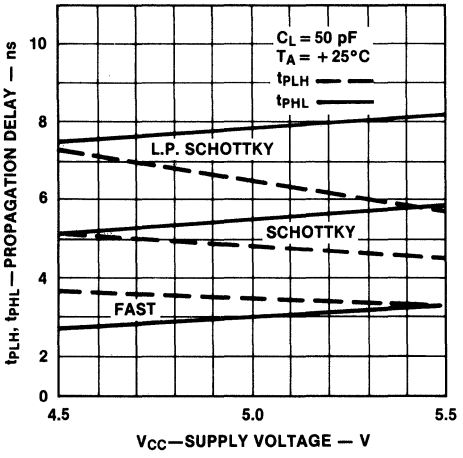


Fig. 2-8 Propagation Delay vs Temperature

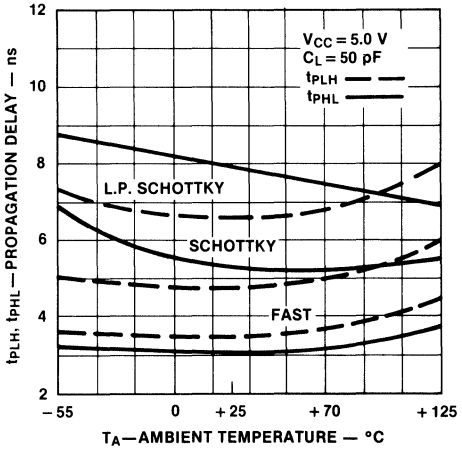
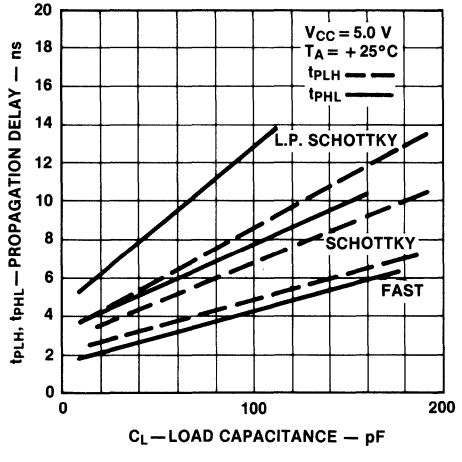


Fig. 2-9 Propagation Delay vs Load Capacitance



instantaneous conditions in discharging load capacitance during an output HIGH-to-LOW transmission when the output voltage is at about 3.5 V, for example, the circuit can absorb charge from the load capacitance at a 500 mA rate at +25°C. From this level the rate decreases steadily down to about 100 mA at 1.5 V. In this region from 3.5 V to 1.5 V, part of the charge from the load capacitance is fed back through D8 (Figure 2-3) and Q2 to provide extra base current for Q3, boosting its current-sinking capability and thus reducing the fall time. Below the 1.5 V level, Q3 continues to discharge the load capacitance, but without extra base current from D8. At about 0.5 V the integral Schottky clamp diode from base to collector of Q3 starts conducting and prevents Q3 from going into deep saturation.

On a greatly expanded scale, the output LOW characteristics of a gate are shown in Figure 2-11. With no load, the output voltage is about 0.1 V, increasing with current on a slope of about 7.5 Ω. When the load current increases beyond the current-sinking capability of Q3, the output voltage rises steeply. It can be seen that the worst-case specification of 0.5 V max at 20 mA load is easily met. Similar characteristics for a buffer shown in Figure 2-12, over a broader current range. The curves are well below the output LOW voltage specification of 0.55 V max at 48 mA over the military temperature range or 64 mA over the commercial temperature range.

The output HIGH characteristics of a FAST gate are shown in Figure 2-13. At low values of output

Fig. 2-10 Output LOW Characteristics—'F00

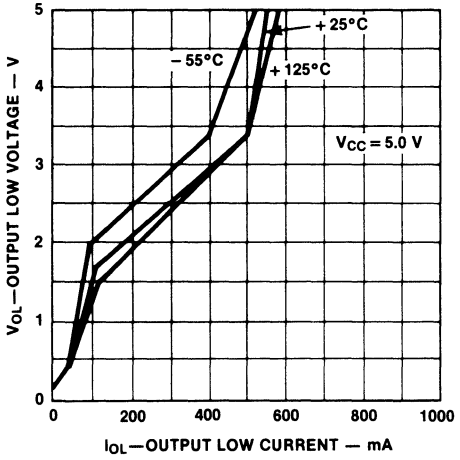


Fig. 2-11 Output LOW Characteristics—'F00

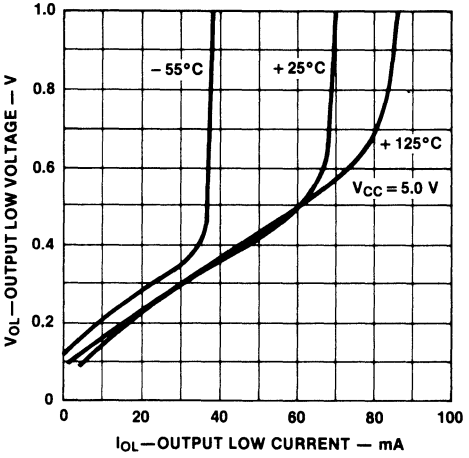


Fig. 2-12 Output LOW Characteristics—'F244

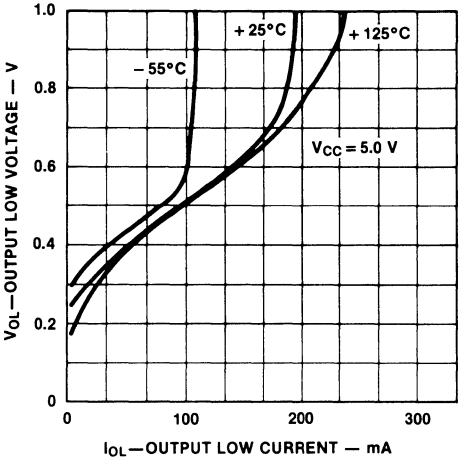
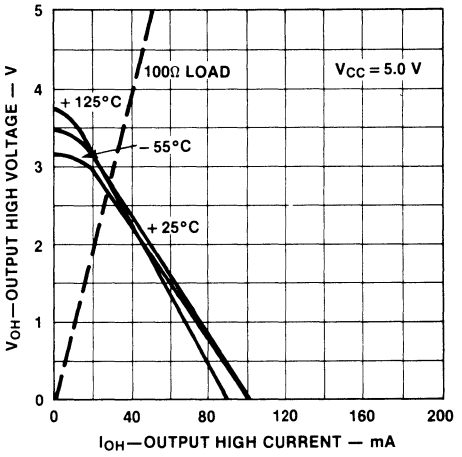


Fig. 2-13 Output HIGH Characteristics—'F00



current the voltage is approximately 3.5 V. This value is just the supply voltage minus the combined base-emitter voltages of the Darlington pull-up transistors Q5 and Q6 (Figure 2-3). For load currents above 16 or 18 mA, the voltage drop across the 45 Ω Darlington collector resistor becomes appreciable and the Darlington saturates. For greater load currents the output voltage decreases with a slope of about 50 Ω, which is largely due to the 45 Ω resistor. The value of current where a characteristic intersects the horizontal axis is the short-circuit output current I_{OS}. This is guaranteed to be at least 60 mA for a FAST gate, compared to 40 mA for S-TTL. This parameter is an important indicator of the ability of an output to charge load capacitance. Thus the FAST specifications insure that an output can charge load capacitance faster, or force a higher LOW-to-HIGH voltage step into the dynamic impedance of a long interconnection.

The output HIGH characteristics of a buffer are shown in Figure 2-14. These are similar in shape to Figure 2-13 but at higher levels of current. The output HIGH voltage of a buffer is guaranteed at two different levels of load current. With a 3 mA load, V_{OH} is guaranteed to be at least 2.4 V for both military and commercial devices. V_{OH} is also guaranteed to be at least 2.0 V with a 12 mA load for military or 15 mA load for commercial devices. In addition, the short-circuit output current of a buffer is guaranteed to be at least 100 mA.

When an output is driving a long interconnection, the initial LOW-to-HIGH transition is somewhat less than the final, quiescent HIGH level because of the loading effect of the line impedance. The full HIGH voltage level is only reached after the reflection from the far end of the line returns to the driver. The initial LOW-to-HIGH voltage step that an output can force into a line is determined by drawing a load line on the graph containing the output HIGH characteristic and noting the voltage value where the load line intersects the characteristic. For example, if a FAST gate is driving a 100 Ω line, a straight line from the lower left origin up to the point 5 V, 50 mA intersects the -55°C characteristic curve at about 2.8 V. This indicates that the gate output voltage will rise to 2.8 V initially, and the 2.8 V signal, accompanied by 28 mA of current, will travel to the end of the line. If not terminated, the 28 mA is forced to return to the driver, whereupon it unloads the driver and the output voltage rises to the maximum value. Similarly, a 50 Ω load line drawn on the buffer characteristic shows an intercept voltage of 2.5 V. In both cases, the initial voltage step is great enough to pass through the switching region of any inputs that might be located near the driver end of the line, and thus would not exhibit any exaggerated propagation delay due to the loading effect of the line impedance on the driver output. Thus the FAST output characteristics insure better system performance under adverse loading conditions.

Input Characteristics

The input of a FAST circuit represents a small capacitance, typically 4 to 5 pF, in parallel with an I-V characteristic that exhibits different slopes over different ranges of input voltage. Figure 2-15 shows the input characteristic of a FAST gate at three temperatures. In the upper right, the flat horizontal portion is the V_{IH}-I_{IH} characteristic. In this region,

Fig. 2-14 Output HIGH Characteristics—'F244

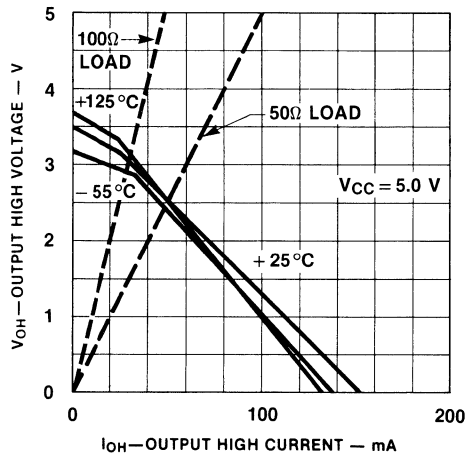
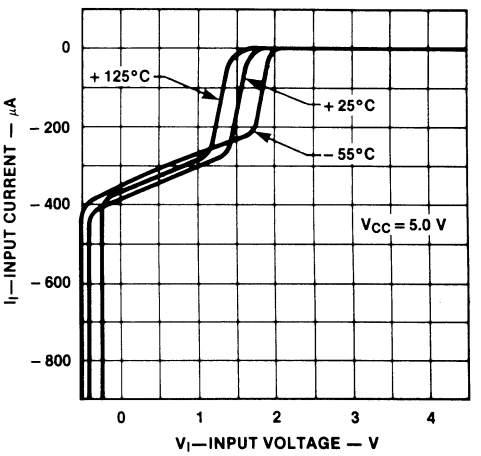


Fig. 2-15 Input Characteristics—'F00

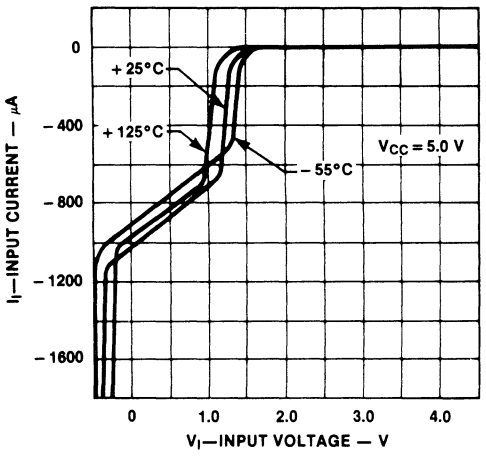


all of the current from the 10K Ω input resistor (Figure 2-3) is flowing into the base of Q1 and the only current flowing in the input diode is the leakage current I_{IH}. When the input voltage decreases to about 1.7 V (+25°C), current starts to flow out of the input diode and the curve shows a knee. At this point some of the current from the 10K Ω resistor is diverted from the base of Q1. When the input voltage declines to about 1.4 V the curve shows another knee; at this point, substantially all of the current from the 10K Ω resistor flows out of the input diode. The portion of the curve between 1.4 V and 1.7 V input voltage is the active region, essentially corresponding to the FAST transfer function in Figure 2-5.

Below 1.4 V input, the characteristic has the slope of the 10K Ω input resistor. When the input voltage declines to about -0.3 V, the Schottky clamping diode starts conducting and the current increases rapidly as the input voltage decreases further.

The input characteristics of a buffer, shown in Figure 2-16, differ from those of a gate in two respects. One is the location of the transition region along the horizontal axis. A buffer input has a hysteresis characteristic about 400 mV wide, such that the transition region shifts left or right accordingly as the input voltage transition is HIGH-to-LOW or LOW-to-HIGH, respectively. The curves in Figure 2-16 apply to the HIGH-to-LOW input voltage transition. The other difference between buffer and gate characteristics is the slope of the curves below the transition region. The input resistor of a buffer is 4 KΩ, and the slope of the characteristic follows this value, rather than the 10 KΩ slope of a gate input.

Fig. 2-16 Input Characteristics—'F244



The characteristics of an input Schottky clamp diode are shown in Figure 2-17, for much larger values of current than those of Figures 2-15 and 2-16. The purpose of the clamp diode is to limit undershoot at the end of a line following a HIGH-to-LOW signal transition. For example, an output signal change from +3.5 V to +0.5 V into a 100 Ω line propagates to the end of the line, accompanied by a 30 mA current change. If the line is terminated in a high impedance the 3 V signal change doubles, driving the terminal voltage down to -2.5 V. With the clamp diode, however, the negative excursion would be limited to about -0.7 V. The same HIGH-to-LOW signal change on a 50 Ω line would be clamped at about -1.0 V. Figure 2-18 shows the typical breakdown characteristics for a FAST input.

Fig. 2-17 Input Characteristics—'F00 or 'F244

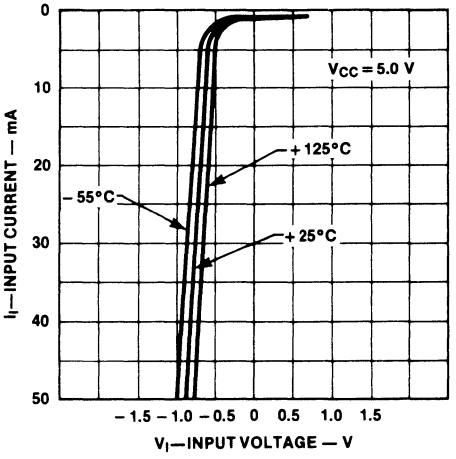
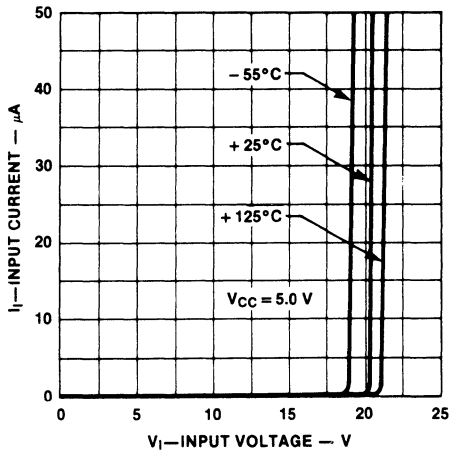


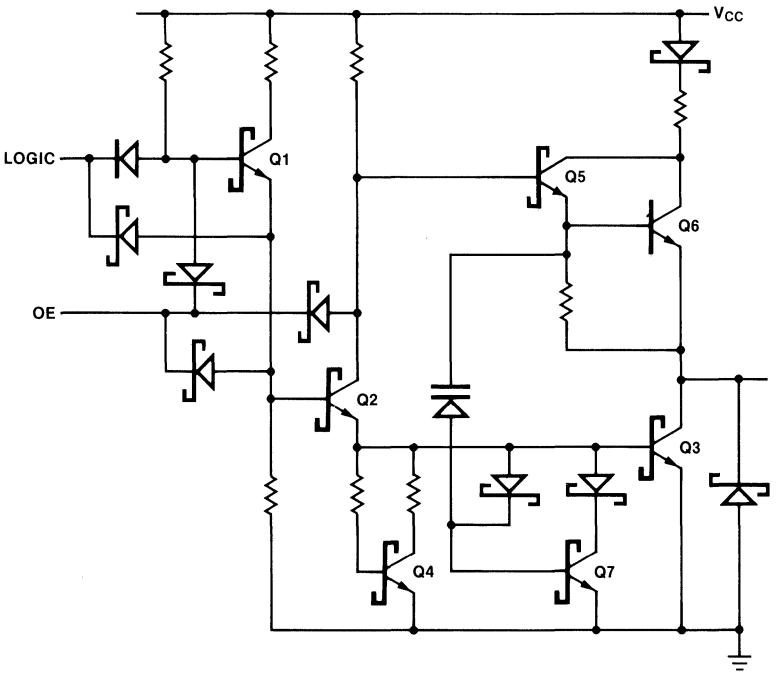
Fig. 2-18 Input Characteristics—'F00 or 'F244

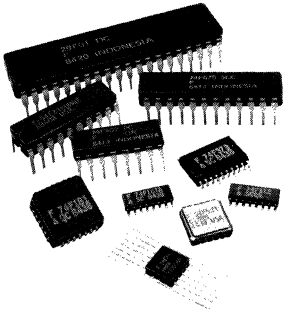


3-State Outputs

A partial schematic of a circuit having a 3-state output is shown in Figure 2-19. When the internal Output Enable (OE) signal is HIGH, the circuit operates in the normal fashion to provide HIGH or LOW output drive characteristics. When OE is LOW, however, the bases of Q1, Q2 and Q5 are pulled down. In this condition the output is a high impedance. In this High Z condition the output leakage is guaranteed not to exceed 50 μA. In the case of a transceiver, each data pin is an input as well as an output and the leakage specification is increased to 70 μA. In the High Z state, output capacitance averages about 5 pF for a 20 mA output and about 12 pF for a 64 mA output.

Fig. 2-19 Typical 3-State Output Control





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Ratings, Specifications and Waveforms

For convenience in system design, the input loading and fan-out characteristics of each circuit are specified in terms of unit loads.

One unit load in the HIGH state is defined as 40 μA; thus both the input HIGH leakage current, I_{IH}, and the output HIGH current-sourcing capability, I_{OH}, are normalized to 40 μA. The specified I_{IH} for a typical FAST single load input is 20 μA or 0.5 U.L. The I_{OH} rating for a FAST output depends upon whether the device has a standard or 3-state output or if the device is a buffer/line driver. The I_{OH} rating for a standard FAST device is 1.0 mA or 25 U.L., while 3-state and line driver circuits specify I_{OH} at 3.0 mA or 75 U.L.

Similarly, one unit load in the LOW state is defined as 1.6 mA and both the input LOW current, I_{IL}, and the output LOW current-sinking capability, I_{OL}, are normalized to 1.6 mA. The specified maximum I_{IL} for a typical FAST single load input is 0.6 mA or 0.375 U.L. However, the I_{OL} rating differs among standard, 3-state and buffer/line driver outputs. The I_{OL} rating for a standard output is 20 mA or 12.5 U.L. FAST devices with 3-state outputs specify I_{OL} at 24 mA or 15 U.L. for commercial temperature range and 20 mA or 12.5 U.L. for military temperature range. The I_{OH} rating for a FAST buffer/line driver output is 64 mA or 40 U.L. for the commercial temperature range and 48 mA or 30 U.L. over the military temperature range.

On the data sheets the input and output load factors are listed in the Input Loading/Fan-Out table. The tables from the 54F/74F373 Transparent Latch and the 29F52 Registered Transceiver are reproduced below.

Input Loading/Fan-Out: 54F/74F373

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
A_0-A_7	A-Register Inputs	1.75/0.406
	B-Register Outputs	25/12.5
B_0-B_7	B-Register Inputs	1.75/0.406
	A-Register Outputs	75/40 (30)
$\overline{OEA}$	Output Enable A-Register	0.5/0.375
CPA	A-Register Clock	0.5/0.375
$\overline{CEA}$	A-Register Clock Enable	0.5/0.375
$\overline{OEB}$	Output Enable B-Register	0.5/0.375
CPB	B-Register Clock	0.5/0.375
$\overline{CEB}$	B-Register Clock Enable	0.5/0.375

Input Loading/Fan-Out: 29F52

Pin Names	Description	29F(U.L.) HIGH/LOW
D_0-D_7	Data Inputs	0.5/0.375
LE	Latch Enable Input (Active HIGH)	0.5/0.375
$\overline{OE}$	Output Enable Input (Active LOW)	0.5/0.375
O_0-O_7	3-State Latch Outputs	75/15 (12.5)

In the right column, the 54F/74F373 input HIGH/LOW load factors are 0.5/0.375 with the first number representing I_{IH} and the second representing I_{IL}. The 29F52 has input HIGH/LOW load factors of 0.5/0.375 for the typical FAST single load inputs and 1.75/0.406 for the register inputs. For testing procurement purposes, these unit load specifications can easily be translated into actual test limits by multiplying the HIGH/LOW load factors by 40 μA and 1.6 mA respectively.

Also in the right-hand column are the output HIGH/LOW load factors, with the first number representing I_{OH} and the second representing I_{OL}. These load factors can be translated to actual test limits by multiplying them by 40 μA and 1.6 mA respectively. The 54F/74F373 output HIGH/LOW drive factors are 75/15 (12.5) which translate into an I_{OH} of 3.0 mA and I_{OL} of 24 mA for commercial grade and 20 mA for military grade. The 29F52 A-Register outputs are typical single load outputs with HIGH/LOW drive factors of 25/12.5 indicating an I_{OH} of 1.0 mA and an I_{OL} of 20 mA. The B-Register outputs specify unit load factors of 75/40 (30) translating into an I_{OH} of 3.0 mA and I_{OL} of 64 mA for commercial and 48 mA for military. In addition, the buffer/line drivers are specified at a higher I_{OH} limit of 15 mA commercial and 12 mA military at a V_{OH} of 2.0 V.

Absolute Maximum Ratings[1]
(beyond which useful life may be impaired)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
V_{CC} Pin Potential to Ground Pin	-0.5 V to +7.0 V
Input Voltage [2]	-0.5 V to +7.0 V
Input Current[2]	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State:	
Standard Output	-0.5 V to V_{CC} Value
3-State Output (with V_{CC} = 0 V)	-0.5 V to +5.5 V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL}

Recommended Operating Conditions[1]

	Min	Max
Free Air Ambient Temperature		
Military (XM)	-55°C	+125°C
Commercial (XC)	0°C	+70°C
Supply Voltage		
Military (XM)	+4.5 V	+5.5 V
Commercial (XC)	+4.75 V	+5.25 V

1. Unless otherwise restricted or extended by detail specifications.
2. Either input voltage or current limit sufficient to protect inputs.

Important Military Note:
Military parameters given herein are for general reference only. For current military specifications and subgroup testing information, please request Fairchild's Table 1 datasheet from your Fairchild Sales Engineer or account representative.

AC Loading and Waveforms

Figure 3-1 shows the AC loading circuit used in characterizing and specifying propagation delays of all FAST devices, unless otherwise specified in the data sheet of a specific device. The use of this load, which differs somewhat from previous practice, provides more meaningful information and minimizes problems of instrumentation and customer correlation. In the past, +25°C propagation delays for TTL devices were specified with a load of 15 pF to ground; this required great care in building test jigs to minimize stray capacitance, and implied the use of high impedance, high frequency scope probes. FAST circuits changed to 50 pF of capacitance allowing more leeway in stray capacitance and also loading the device during rising or falling output transitions, which more closely resembles the loading to be expected in average applications and thus gives the designer more useful delay figures. The net effect of the change in AC load is to increase the observed propagation delay by an average of about 1 ns.

The 500 Ω resistor to ground, in Figure 3-1, acts as a ballast, to slightly load the totem-pole pull-up and limit the quiescent HIGH-state voltage to about +3.5 V. Otherwise, an output would rise quickly to about +3.5 V but then continue to rise very slowly to about +4.4 V. On the subsequent HIGH-to-LOW transition the observed t_{PHL} would vary slightly with duty cycle, depending on how long the output voltage was allowed to rise before switching to the LOW state. Perhaps more importantly, the 500 Ω resistor to ground can be a high frequency passive probe for a sampling scope, which costs much less than the equivalent high impedance probe. Alternatively, the 500 Ω load to ground can simply be a 450 Ω resistor feeding into a 50 Ω coaxial cable leading to a sampling scope input connector, with the internal 50 Ω termination of the scope completing the path to ground. Note that with this scheme there should be a matching cable from the device input pin to the other input of the sampling scope; this also serves as a 50 Ω termination for the pulse generator that supplies the input signal.

Also shown in Figure 3-1 is a second 500 Ω resistor from the device output to a switch. For most measurements this switch is open; it is closed for measuring a device with open-collector outputs and for measuring one set of the Enable/Disable parameters (LOW-to-OFF and OFF-to-LOW) of a 3-state output. With the switch closed, the pair of 500 Ω resistors and the +7.0 V supply establish a quiescent HIGH level of +3.5 V, which correlates with the HIGH level discussed in the preceding paragraph.

Figures 3-12 and 3-13 show that the Disable times are measured at the point where the output voltage has risen or fallen by 0.3 V from the quiescent level (i.e., LOW for t_{PLZ} or HIGH for t_{PHZ}), compared to a ΔV of 0.5 V used in previous practice. This change enhances the repeatability of measurements and gives the system designer more realistic delay times to use in calculating minimum cycle times. Since the rising or falling waveform is RC-controlled, the first 0.3 V of change is more linear than the first 0.5 V and is less susceptible to external influences. More importantly, perhaps, from the system designer's point of view, a Δ V of 0.3 V is adequate to ensure that a device output has turned OFF; measuring to a Δ V of 0.5 V merely exaggerates the apparent Disable time and thus penalizes system performance, since the designer must use the Enable and Disable times to devise worst-case timing signals to ensure that the output of one device is disabled before that of another device is enabled.

Figure 3-17 describes the input signal voltages recommended for use when testing FAST circuits. The AC input signal levels follow industry convention of V_{IN} switching 0 to 3 volts. DC low input levels are typically 0 to V_{IL}, and high input levels are typically V_{IH} to V_{CC}. Input thresholds are guaranteed during V_{OL} and V_{OH} tests. High level noise immunity is the difference between V_{OH} and V_{IH}. Low level noise immunity is the difference between V_{IL} and V_{OL}. Noise-free V_{IH} or V_{IL} levels should not induce a switch on the appropriate output of the FAST device. When testing in an automatic test environment, extreme caution should be taken to ensure that input levels plus noise do not go into the transition region.

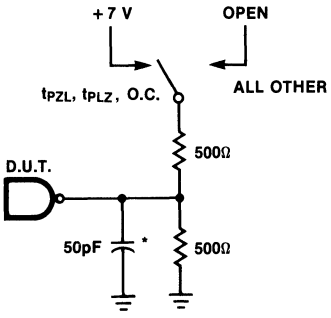
Good high frequency wiring practices should be used in constructing test jigs. Leads on the load capacitor should be as short as possible to minimize ripples on the output waveform transitions and to minimize undershoot. Generous ground metal (preferably a ground plane) should be used for the same reasons. A V_{CC} bypass capacitor should be provided at the test socket, also with minimum lead lengths. Input signals should have rise and fall times of 2.5 ns and signal swing of 0 V to +3.0 V. Rise and fall times $\leq$ 1 ns should

be used for testing f_{max} or pulse width. A 1.0 MHz square wave is recommended for most propagation delay tests. The repetition rate must necessarily be increased for testing f_{max}. A 50% duty cycle should always be used when testing f_{max}. Two pulse generators are usually required for testing such parameters as setup time, hold time, recovery time, etc.

Precautions should be taken to prevent damage to devices by electrostatic charge. Static charge tends to accumulate on insulated surfaces, such as synthetic fabrics or carpeting, plastic sheets, trays, foam, tubes or bags, and on ungrounded electrical tools or appliances. The problem is much worse in a dry atmosphere. In general, it is recommended that individuals take the precaution of touching a known ground before handling devices. To effectively avoid electrostatic damage to FAST devices it may be necessary for individuals to wear a grounded wrist strap when handling devices.

AC limits on SOIC packages are the same as DIP, except for all minimum limits, which are 0.2 ns faster.

Fig. 3-1 Test Load



*INCLUDES JIG AND PROBE CAPACITANCE

Fig. 3-2 Propagation Delays from Up/Down Control

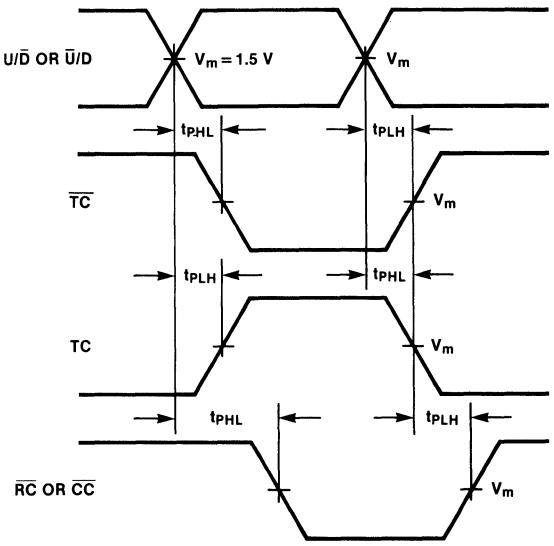


Fig. 3-3 Waveform for Inverting Functions

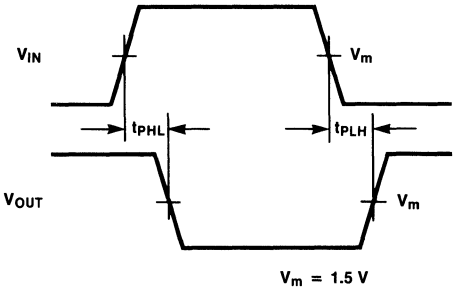


Fig. 3-4 Waveform for Non-Inverting Functions

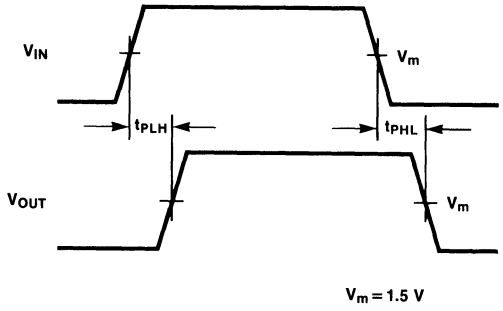


Fig. 3-5 Setup and Hold Times, Rising-Edge Clock

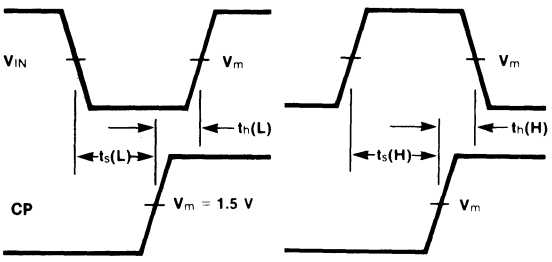


Fig. 3-6 Setup and Hold Times, Falling-Edge Clock

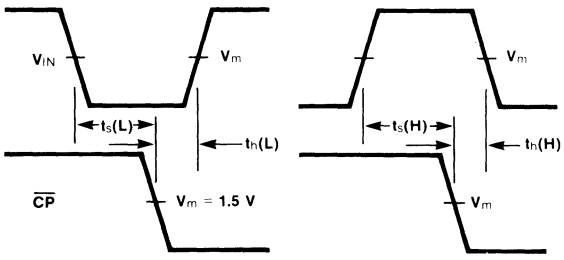


Fig. 3-7 Propagation Delays from Rising-Edge Clock or Enable

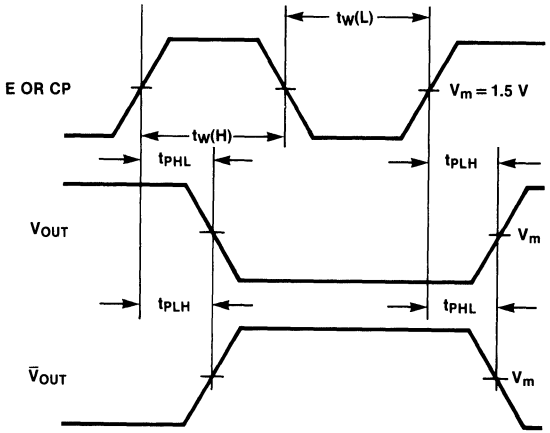
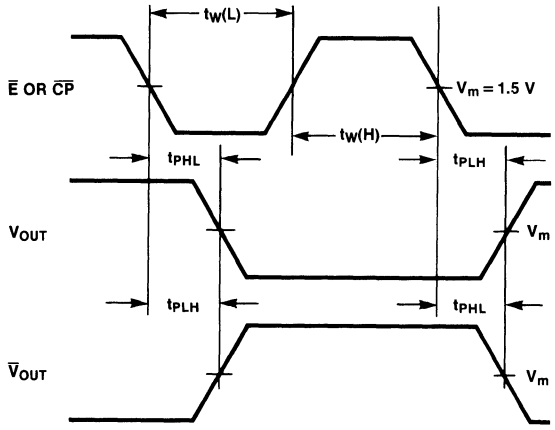


Fig. 3-8 Propagation Delays from Falling-Edge Clock or Enable



3

Fig. 3-9 Propagation Delays from Set and Clear (or Reset)

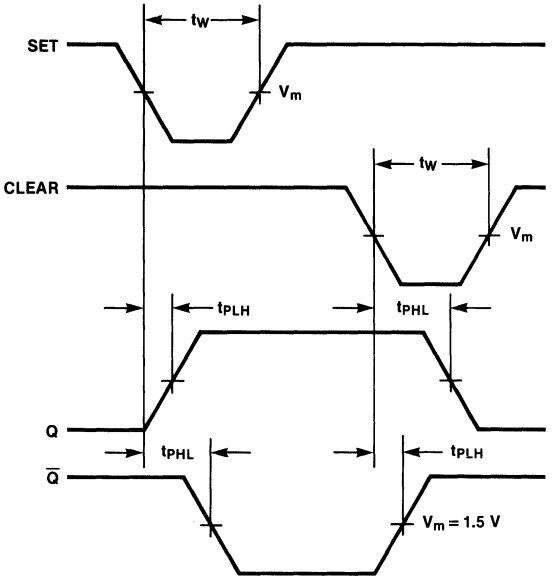


Fig. 3-10 Whether Response is Inverting or Non-Inverting Depends on Specific Truth Table Conditions

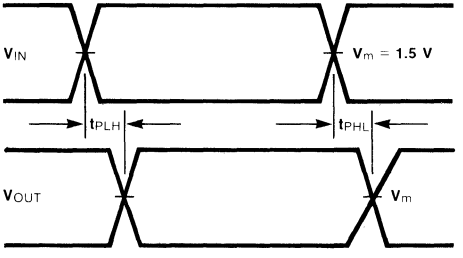


Fig. 3-11 Asynchronous Set, Reset, Parallel Load or Clear, Active Rising-Edge Clock or Active LOW Enable

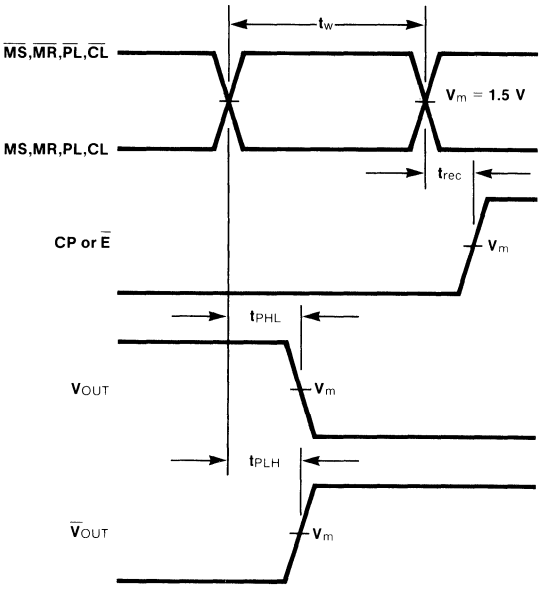


Fig. 3-12 3-State Output LOW Enable and Disable Times

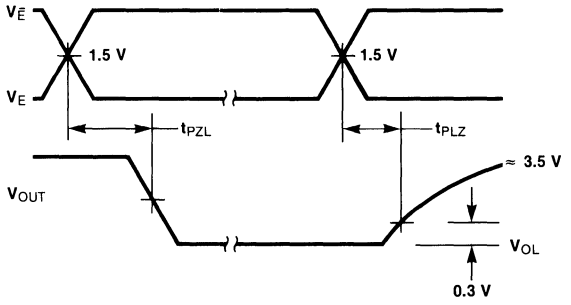


Fig. 3-13 3-State Output HIGH Enable and Disable Times

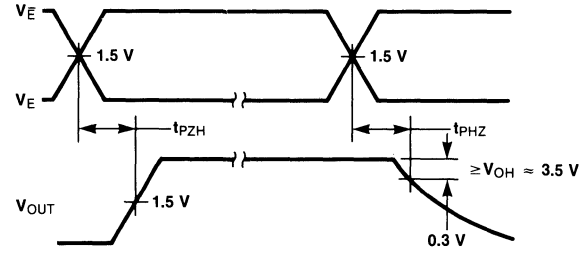


Fig. 3-14 Setup and Hold Times to Active LOW Enable or Parallel Load

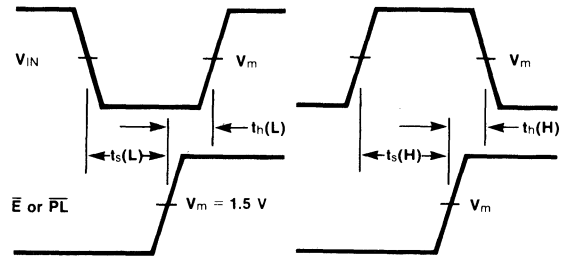


Fig. 3-15 Setup and Hold Times to Active HIGH Enable or Parallel Load

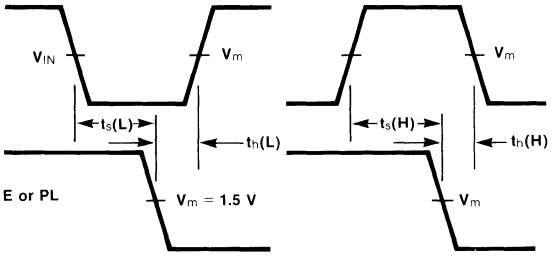


Fig. 3-16 Storage Address Setup and Hold Times

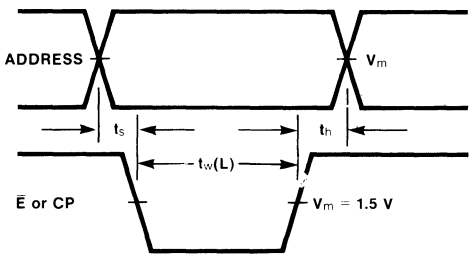
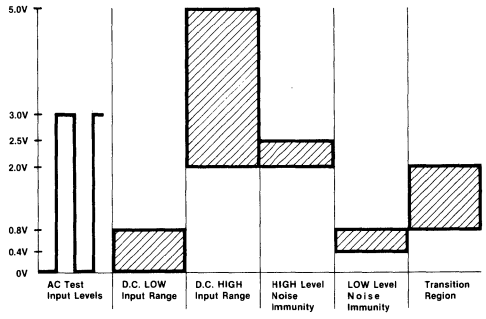


Fig. 3-17 Test Input Signal Levels



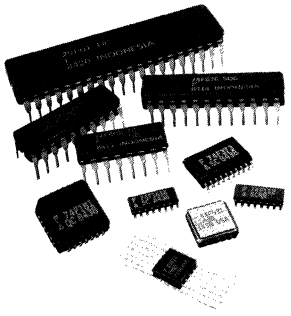
54F/74F DC Family Characteristics[1]

Symbol	Parameter		Limits[2] Min	Limits[2] Typ[3]	Limits[2] Max	Units	V_{CC}[4]	Conditions[2]	
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal over Recommended V_{CC} and T_A Range	
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal over Recommended V_{CC} and T_A Range	
V_{CD}	Input Clamp Diode Voltage				-1.2	V	Min	I_{IN} = -18 mA	
V_{OH}	Output HIGH Voltage Std/3-State[6]	Mil	2.5	3.4		V	Min	I_{OH} = -1 mA	
		Com[7]	2.7	3.4					
	Output HIGH Voltage 3-State/Line Driver[6]	Mil	2.4	3.3		V	Min	I_{OH} = -3 mA	
		Com[7]	2.7	3.3					
	Output HIGH Voltage Line Driver[6]	Mil	2.0	3.2		V	Min	I_{OH} = -12 mA	
		Com[7]	2.0	3.1				I_{OH} = -15 mA	
V_{OL}	Output LOW Voltage Standard[6]	Mil		0.30	0.5	V	Min	I_{OL} = 20 mA	
		Com		0.30	0.5				
	Output LOW Voltage 3-State[6]	Mil		0.30	0.5	V	Min	I_{OL} = 20 mA	
		Com		0.35	0.5			I_{OL} = 24 mA	
	Output LOW Voltage Line Driver[6]	Mil		0.38	0.55	V	Min	I_{OL} = 48 mA	
		Com		0.42	0.55			I_{OL} = 64 mA	
I_{IH}	Input HIGH Current	0.5 U.L.			20	μA	Max	V_{IN} = 2.7 V	I_{IH} = 40 μA Multiplied by Input HIGH U.L. Shown on Data Sheet
		n U.L.			n(40)				
	Input HIGH Current Breakdown Test, Std Inputs				100	μA	Max	V_{IN} = 7.0 V	
	Input HIGH Current Breakdown Test, Transceivers				1.0	mA	Max	V_{IN} = 5.5 V	
I_{IL}	Input LOW Current	0.375 U.L.			-0.6	mA	Max	I_{IL} = -1.6 mA Multiplied by Input LOW U.L. Shown on Data Sheet, V_{IN} = 0.5 V	
		n U.L.			n(-1.6)				

54F/74F Family DC Characteristics (cont'd)

Symbol	Parameter		Limits[2]			Units	V_{CC}[4]	Conditions[2]
			Min	Typ[3]	Max			
I_{OZH}	3-State Output OFF Current HIGH				50	μA	Max	$V_{OUT} = 2.7$ V
I_{OZL}	3-State Output OFF Current LOW				-50	μA	Max	$V_{OUT} = 0.5$ V
I_{OH}	Open Collector Output Leakage Current				100	μA	Min	$V_{IN} = V_{IH}/V_{IL}$ $V_{OUT} = V_{CC}$
I_{OS}[5]	Output Short-Circuit Current	Std/3-State[6]	-60		-150	mA	Max	$V_{OUT} = 0$ V
		Line Driver[6]	-100		-225			

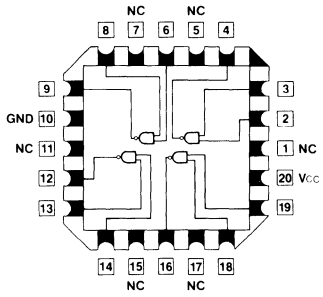
1. Unless otherwise noted, conditions and limits apply throughout the temperature range for which the particular device type is rated. The ground pin is the reference level for all applied and resultant voltages.
2. Unless otherwise stated on individual data sheets.
3. Typical characteristics refer to $T_A = +25°C$ and $V_{CC} = +5.0$ V.
4. Min and Max refer to the values listed in the table of recommended operating conditions.
5. For I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
6. Refers to the type of output pull-up/pulldown circuitry used for the particular device. Standard outputs may be identified by an Output HIGH/LOW fan-out of 25/12.5 U.L.; 3-State outputs may be identified by an Output HIGH/LOW fan-out of 75/15 (12.5) U.L.; Line Driver outputs may be identified by an Output HIGH/LOW fan-out of 75/40 (30) U.L.
7. Refers to ±5% V_{CC} specifications. ±10% V_{CC} Commercial limits are the same as the Military limits.



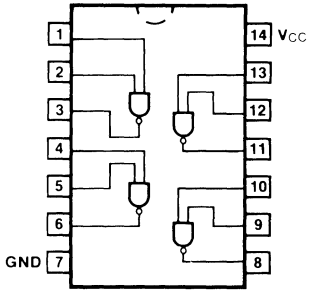
54F/74F00

Quad 2-Input NAND Gate

Connection Diagrams



Pin Assignment for LCC and PCC



Pin Assignment for DIP and SOIC

Ordering Code: See Section 5

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
	Inputs	0.5/0.375
	Outputs	25/12.5

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions	
		Min	Typ	Max			
I_{CCH}	Power Supply Current		1.9	2.8	mA	V_{IN} = Gnd	V_{CC} = Max
I_{CCL}			6.8	10.2		V_{IN} = Open	

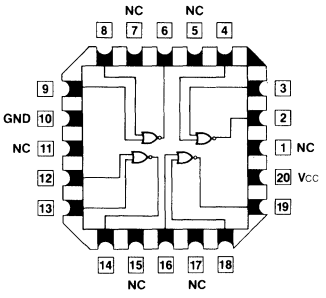
AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	2.4	3.7	5.0	2.0	7.0	2.4	6.0	ns	3-1
t_{PHL}		1.5	3.2	4.3	1.5	6.5	1.5	5.3		3-3

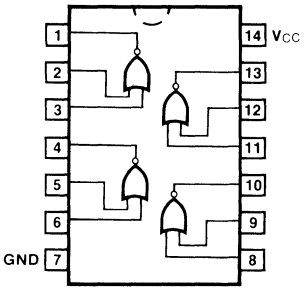
54F/74F02

Quad 2-Input NOR Gate

Connection Diagrams



Pin Assignment for LCC and PCC



Pin Assignment for DIP and SOIC

Ordering Code: See Section 5

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
	Inputs Outputs	0.5/0.375 25/12.5

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions	
		Min	Typ	Max			
I_{CCH}	Power Supply Current		3.7	5.6	mA	V_{IN} = Gnd	V_{CC} = Max
I_{CCL}			8.7	13.0		*	

*Measured with one input HIGH, one input LOW for each gate.

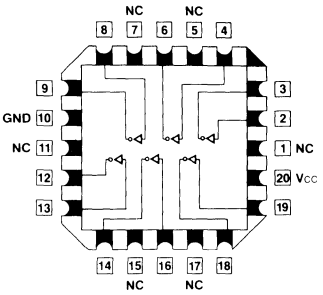
AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	2.5	4.4	5.5	2.5	7.5	2.5	6.5	ns	3-1
t_{PHL}		1.5	3.2	4.3	1.5	6.5	1.5	5.3		3-3

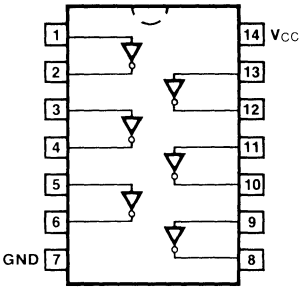
54F/74F04

Hex Inverter

Connection Diagrams



Pin Assignment for LCC and PCC



Pin Assignment for DIP and SOIC

Ordering Code: See Section 5

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
	Inputs Outputs	0.5/0.375 25/12.5

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions	
		Min	Typ	Max			
I_{CCH}	Power Supply Current		2.8	4.2	mA	V_{IN} = Gnd	V_{CC} = Max
I_{CCL}			10.2	15.3		V_{IN} = Open	

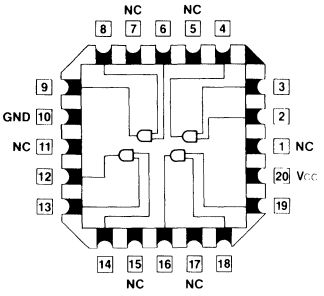
AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			54F T_A, V_{CC} = Mil, C_L = 50 pF		74F T_A, V_{CC} = Com, C_L = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	2.4	3.7	5.0	2.0	7.0	2.4	6.0	ns	3-1
t_{PHL}		1.5	3.2	4.3	1.5	6.5	1.5	5.3		3-3

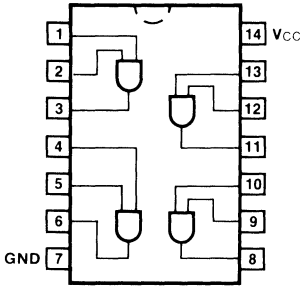
54F/74F08

Quad 2-Input AND Gate

Connection Diagrams



Pin Assignment for LCC and PCC



Pin Assignment for DIP and SOIC

Ordering Code: See Section 5

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
	Inputs Outputs	0.5/0.375 25/12.5

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions	
		Min	Typ	Max			
I_{CCH}	Power Supply Current		5.5	8.3	mA	V_{IN} = Open	V_{CC} = Max
I_{CCL}			8.6	12.9		V_{IN} = Gnd	

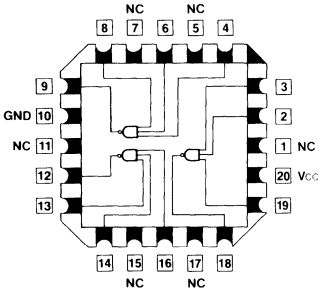
AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay	3.0 2.5	4.2 4.0	5.6 5.3	2.5 2.0	7.5 7.5	3.0 2.5	6.6 6.3	ns	3-1 3-4

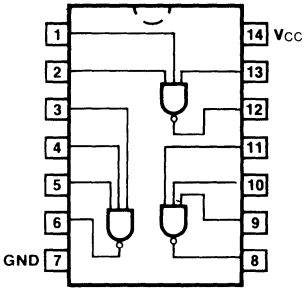
54F/74F10

Triple 3-Input NAND Gate

Connection Diagrams



Pin Assignment for LCC and PCC



Pin Assignment for DIP and SOIC

Ordering Code: See Section 5

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
	Inputs Outputs	0.5/0.375 25/12.5

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions	
		Min	Typ	Max			
I_{CCH}	Power Supply Current		1.4	2.1	mA	V_{IN} = Gnd	V_{CC} = Max
I_{CCL}			5.1	7.7		V_{IN} = Open	

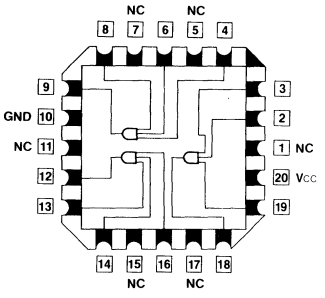
AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	2.4	3.7	5.0	2.0	7.0	2.4	6.0	ns	3-1
t_{PHL}		1.5	3.2	4.3	1.5	6.5	1.5	5.3		3-3

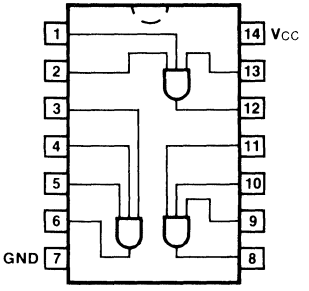
54F/74F11

Triple 3-Input AND Gate

Connection Diagrams



Pin Assignment for LCC and PCC



Pin Assignment for DIP and SOIC

Ordering Code: See Section 5

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
	Inputs	0.5/0.375
	Outputs	25/12.5

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions	
		Min	Typ	Max			
I_{CCH}	Power Supply Current		4.1	6.2	mA	V_{IN} = Open	V_{CC} = Max
I_{CCL}			6.5	9.7		V_{IN} = Gnd	

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	3.0	4.2	5.6	2.5	7.5	3.0	6.6	ns	3-1
t_{PHL}		2.5	4.1	5.5	2.0	7.5	2.5	6.5		3-4

54F/74F13

Dual 4-Input NAND Schmitt Trigger

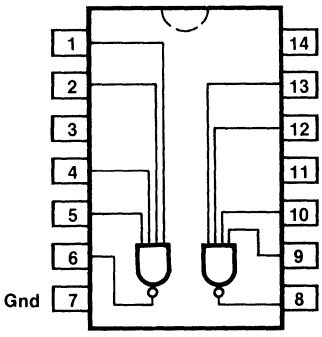
Description

The 'F13 contains two 4-input NAND gates which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have a greater noise margin than conventional NAND gates.

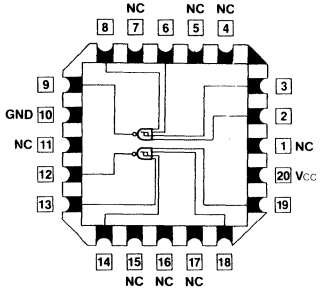
Each circuit contains a 4-input Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem-pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input threshold (typically 800 mV) is determined by resistor ratios and is essentially insensitive to temperature and supply voltage variations.

Ordering Code: See Section 5

Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
A,B,C,D	Inputs	0.5/0.375
O	Outputs	25/12.5

Function Table

Inputs				Outputs
A	B	C	D	O
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions	
		Min	Typ	Max			
I_{CCH}	Power Supply Current		4.5	8.5	mA	Outputs HIGH	V_{CC} = Max
I_{CCL}			7.0	10.0		Outputs LOW	

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay		7.0 13.5						ns	3-1 3-3

54F/74F14

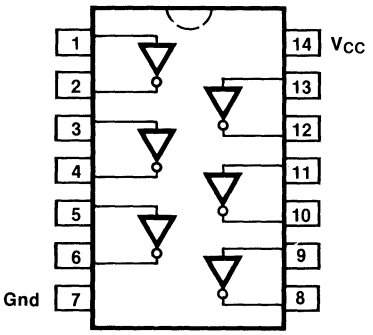
Hex Inverter Schmitt Trigger

Description

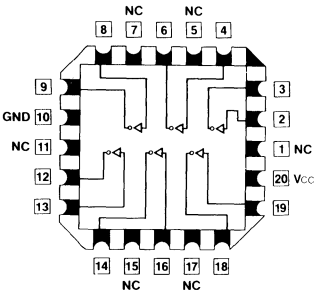
The 'F14 contains six logic inverters which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have a greater noise margin than conventional inverters.

Each circuit contains a Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem-pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transition, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input thresholds (typically 800 mV) is determined internally by resistor ratios and is essentially insensitive to temperature and supply voltage variations.

Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Ordering Code: See Section 5

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
A	Inputs	0.5/0.375
O	Outputs	25/12.5

Function Table

Input	Output
A	O
0	1
1	0

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions	
		Min	Typ	Max			
I_{CCH}	Power Supply Current		13	22	mA	Outputs HIGH	V_{CC} = Max
I_{CCL}			23	32		Outputs LOW	

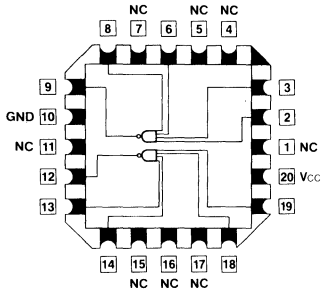
AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay		6.5 7.5						ns	3-1 3-3

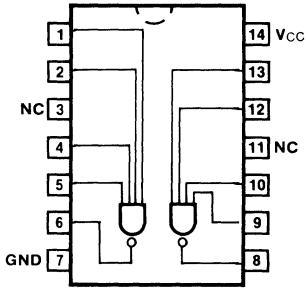
54F/74F20

Dual 4-Input NAND Gate

Connection Diagrams



Pin Assignment for LCC and PCC



Pin Assignment for DIP and SOIC

Ordering Code: See Section 5

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
	Inputs Outputs	0.5/0.375 25/12.5

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions	
		Min	Typ	Max			
I_{CCH}	Power Supply Current		0.9	1.4	mA	V_{IN} = Gnd	V_{CC} = Max
I_{CCL}			3.4	5.1		V_{IN} = Open	

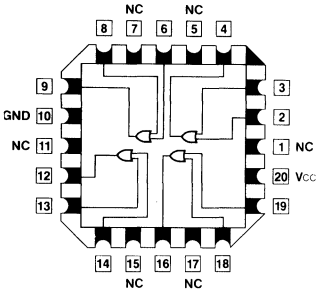
AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	2.4	3.7	5.0	2.0	7.0	2.4	6.0	ns	3-1
t_{PHL}		1.5	3.2	4.3	1.5	6.5	1.5	5.3		3-3

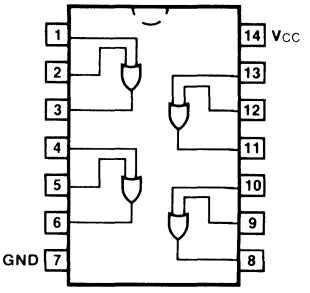
54F/74F32

Quad 2-Input OR Gate

Connection Diagrams



Pin Assignment for LCC and PCC



Pin Assignment for DIP and SOIC

Ordering Code: See Section 5

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
	Inputs Outputs	0.5/0.375 25/12.5

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions	
		Min	Typ	Max			
I_{CCH}	Power Supply Current		6.1	9.2	mA	V_{IN} = Open	V_{CC} = Max
I_{CCL}			10.3	15.5		V_{IN} = Gnd	

AC Characteristics: See Section 3 for waveforms and load configurations

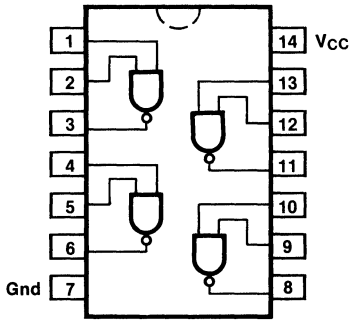
Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	3.0	4.2	5.6	3.0	7.5	3.0	6.6	ns	3-1
t_{PHL}		3.0	4.0	5.3	2.5	7.5	3.0	6.3		3-4

54F/74F37

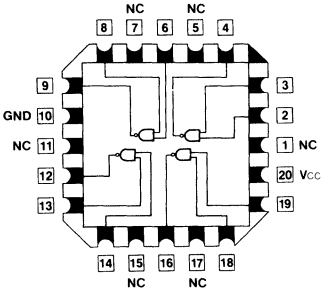
Quad 2-Input NAND Buffer

PRELIMINARY

Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Ordering Code: See Section 5

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
A,B	Inputs	0.5/0.375
O	Outputs	75/40 (30)

Function Table

Inputs		Output
A	**B**	**O**
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current			22	mA	V_{CC} = Max, Outputs LOW

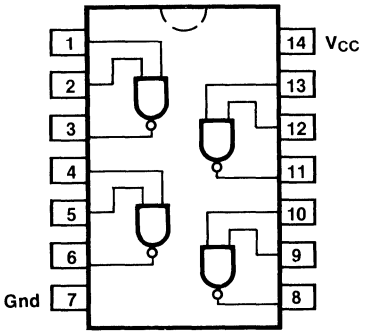
AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay		5.0 4.3						ns	3-1 3-3

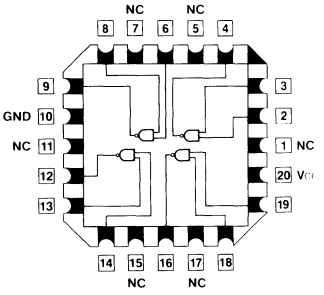
54F/74F38

Quad 2-Input NAND Buffer (Open Collector)

Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Ordering Code: See Section 5

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
A,B	Inputs	0.5/0.375
O	Output	OC*/12.5

*OC = Open Collector

Function Table

Inputs		Output
A	B	O
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions	
		Min	Typ	Max			
I_{CCH}	Power Supply Current			22	mA	V_{CC} = Max	V_{IN} = Gnd
I_{CCL}				22			V_{IN} = HIGH

AC Characteristics: See Section 3 for waveforms and load configurations

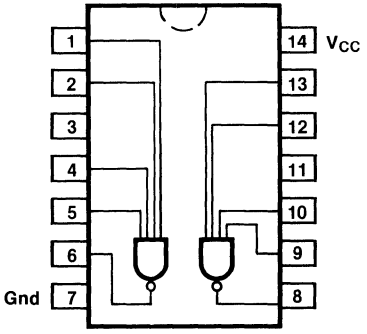
Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay			9.0					ns	3-1
t_{PHL}				6.0						3-3

54F/74F40

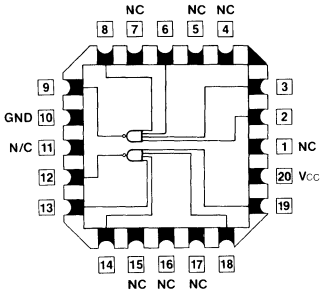
Dual 4-Input NAND Buffer

PRELIMINARY

Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Ordering Code: See Section 5

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
A,B,C,D	Inputs	0.5/0.375
O	Outputs	75/40 (30)

Function Table

Inputs				Outputs
A	B	C	D	O
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current			22	mA	V_{CC} = Max, Outputs LOW

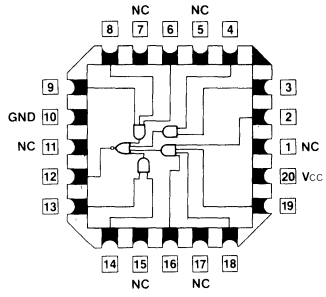
AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay		5.0 4.3						ns	3-1 3-3

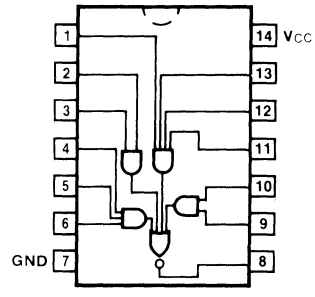
54F/74F64

4-2-3-2-Input AND/OR Invert Gate

Connection Diagrams



Pin Assignment for LCC and PCC



Pin Assignment for DIP and SOIC

Ordering Code: See Section 5

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
A, B	Inputs	0.5/0.375
O	Outputs	25/12.5

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions	
		Min	Typ	Max			
I_{CCH}	Power Supply Current		1.9	2.8	mA	V_{IN} = Gnd	V_{CC} = Max
I_{CCL}			3.1	4.7		*	

* I_{CCL} is measured with all inputs of one gate open and remaining inputs grounded

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	2.5	4.6	6.5	2.5	8.5	2.5	7.5	ns	3-1
t_{PHL}		1.5	3.2	4.5	1.5	6.5	1.5	5.5		3-3

54F/74F74

Dual D-Type Positive Edge-Triggered Flip-Flop

Description

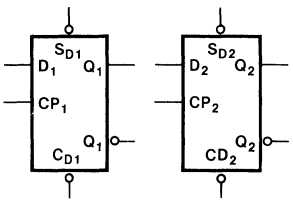
The 'F74 is a dual D-type flip-flop with Direct Clear and Set inputs and complementary (Q, $\overline{Q}$) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

Asynchronous Inputs:

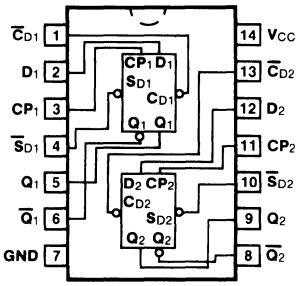
LOW input to $\overline{S}_D$ sets Q to HIGH level
LOW input to $\overline{C}_D$ sets Q to LOW level
Clear and Set are independent of clock
Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

Ordering Code: See Section 5

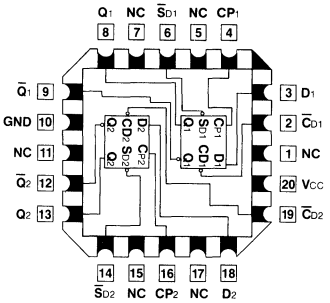
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

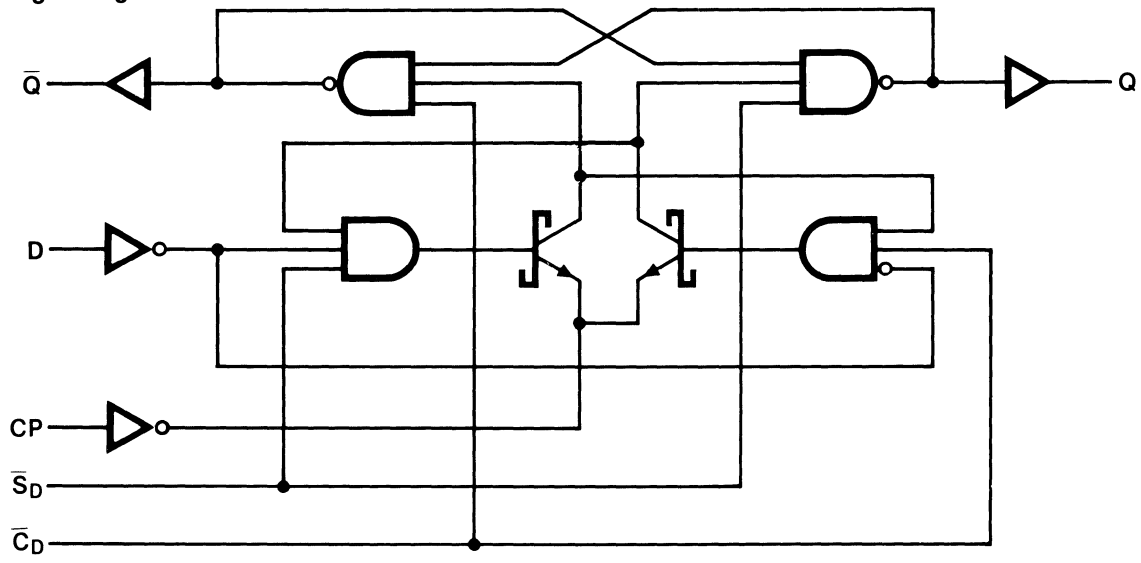
Pin Names	Description	54F/74F(U.L.) HIGH/LOW
D_1, D_2	Data Inputs	0.5/0.375
CP_1, CP_2	Clock Pulse Inputs (Active Rising Edge)	0.5/0.375
$\overline{C}_{D1}$, $\overline{C}_{D2}$	Direct Clear Inputs (Active LOW)	0.5/1.125
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct Set Inputs (Active LOW)	0.5/1.125
Q_1, $\overline{Q}_1$, Q_2, $\overline{Q}_2$	Outputs	25/12.5

Truth Table
(Each Half)

Input	Outputs	
@ t_n	@ t_{n+1}	
D	Q	$\overline{Q}$
L	L	H
H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
t_n = Bit Time before Clock Pulse
t_{n+1} = Bit Time after Clock Pulse

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		10.5	16.0	mA	V_{CC} = Max, V_{CP} = 0 V

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$			T_A, V_{CC} = Mil $C_L = 50\ pF$		T_A, V_{CC} = Com $C_L = 50\ pF$			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	100	125		80		100		MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	3.8 4.4	5.3 6.2	6.8 8.0	3.8 4.4	8.5 10.5	3.8 4.4	7.8 9.2	ns	3-1 3-7
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	3.2 3.5	4.6 7.0	6.1 9.0	3.2 3.5	8.0 11.5	3.2 3.5	7.1 10.5	ns	3-1 3-9

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW D_n to CP_n	2.0 3.0			3.0 4.0		2.0 3.0		ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D_n to CP_n	1.0 1.0			2.0 2.0		1.0 1.0			
$t_w(H)$ $t_w(L)$	CP_n Pulse Width HIGH or LOW	4.0 5.0			4.0 6.0		4.0 5.0		ns	3-7
$t_w(L)$	$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width LOW	4.0			4.0		4.0		ns	3-9
t_{rec}	Recovery Time $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP	2.0			3.0		2.0		ns	3-11

54F/74F85

4-Bit Magnitude Comparator

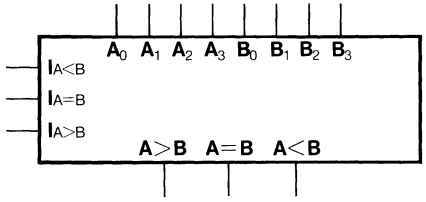
Description

The 'F85 is a 4-bit magnitude comparator that can be expanded to almost any length. It compares two 4-bit binary, BCD, or other monotonic codes and presents the three possible magnitude results at the outputs. The 4-bit inputs are weighted (A_0-A_3) and (B_0-B_3), where A_3 and B_3 are the most significant bits.

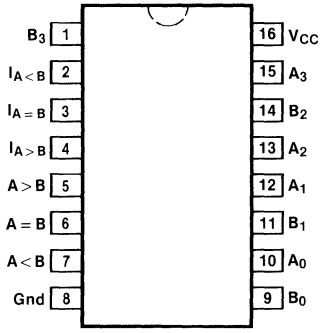
- **Magnitude Comparison of Any Binary Words**
- **Serial or Parallel Expansion Without Extra Gating**

Ordering Code: See Section 5

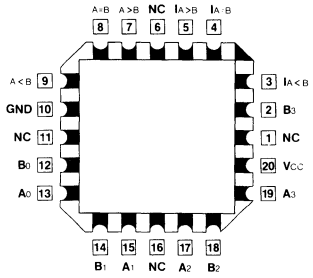
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
A_0-A_3	A Inputs	0.5/0.375
B_0-B_3	B Inputs	0.5/0.375
$I_{A<B}$	Expansion Input, Less Than	0.5/0.375
$I_{A=B}$	Expansion Input, Equal To	0.5/0.375
$I_{A>B}$	Expansion Input, Greater Than	0.5/0.375
A>B	Greater Than Output	25/12.5
A=B	Equal To Output	25/12.5
A<B	Less Than Output	25/12.5

Functional Description

The operation of the 'F85 is described in the Function Table, which shows all possible logic conditions. The upper part of the table describes the normal operation under all conditions that will occur in a single device or in a series expansion scheme. In the upper part of the table the three outputs are mutually exclusive. In the lower part of the table, the outputs reflect the feed-forward conditions that exist in the parallel expansion scheme.

The expansion inputs $I_{A>B}$, $I_{A=B}$, and $I_{A<B}$ are the least significant bit positions. When used for series expansion, the A>B, A=B and A<B outputs of the least significant word are connected to the corresponding $I_{A>B}$, $I_{A=B}$, and $I_{A<B}$ inputs of the next higher stage. Stages can be added in this manner to any length, but a propagation delay penalty of about 15ns is added with each additional stage. For proper operation the expansion inputs of the least significant word should be tied as follows: $I_{A>B}$ = LOW, $I_{A=B}$ = HIGH, and $I_{A<B}$ = LOW.

The parallel expansion scheme shown in Figure a demonstrates the most efficient general use of these comparators. In the parallel expansion scheme, the expansion inputs can be used as a fifth input bit position, except on the least significant device which must be connected as in the serial scheme. The expansion inputs are used by labeling $I_{A<B}$ as an 'A' input, $I_{A<B}$ as a 'B' input and setting $I_{A=B}$ LOW. The 'F85 can be used as a 5-bit comparator only when the outputs are used to drive the A_0-A_3 and B_0-B_3 inputs of another 'F85 device. The parallel technique can be expanded to any number of bits as shown in Table 1.

Table 1

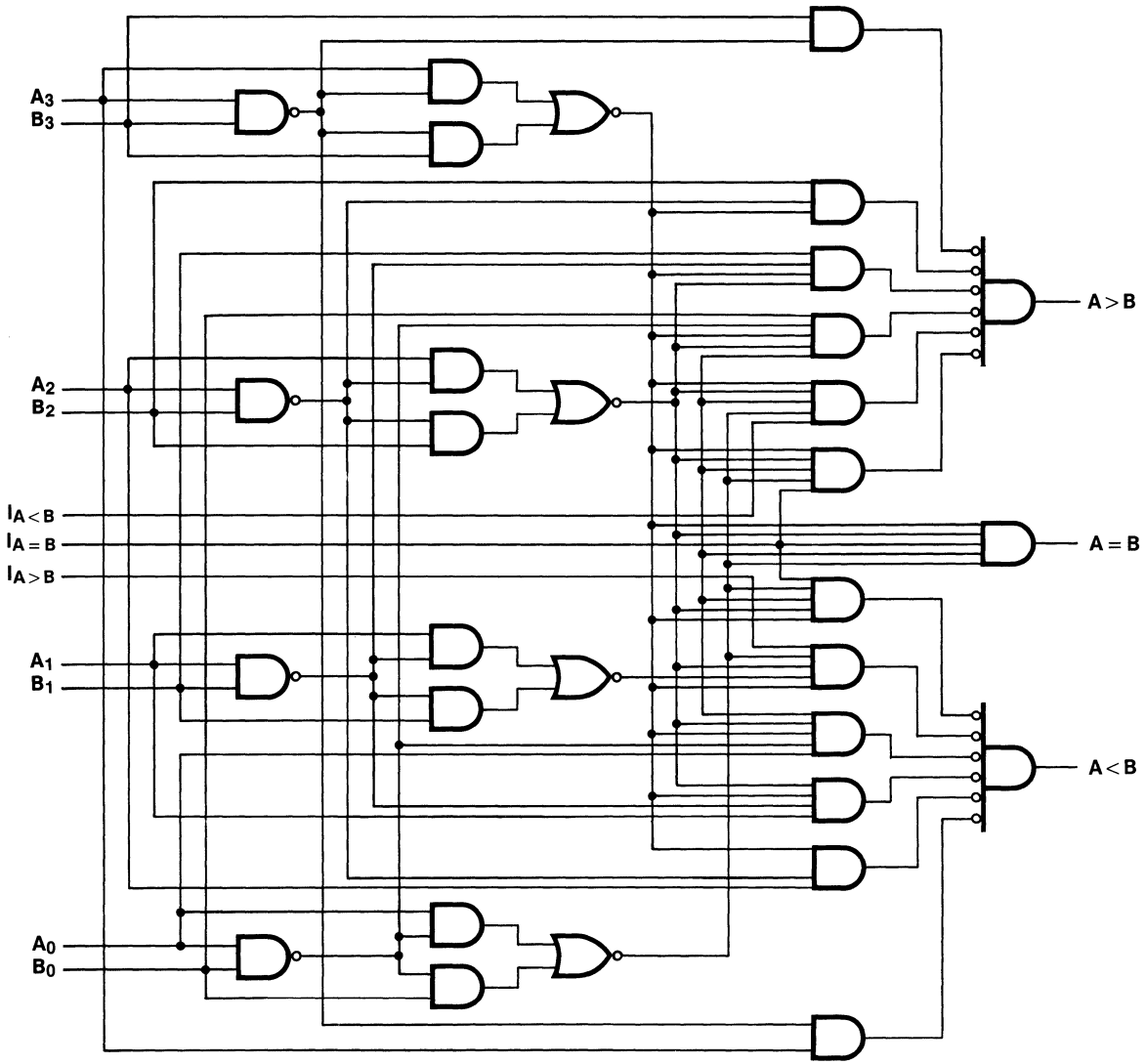
Word Length	Number of Packages	Typical Speeds 54F/74F
1-4 Bits	1	12 ns
5-25 Bits	2-6	22 ns
25-120 Bits	8-31	34 ns

Function Table

Comparing Inputs				Cascading Inputs			Outputs		
A_3,B_3	A_2,B_2	A_1,B_1	A_0,B_0	$I_{A>B}$	$I_{A<B}$	$I_{A=B}$	A>B	A<B	A=B
$A_3>B_3$	X	X	X	X	X	X	H	L	L
$A_3<B_3$	X	X	X	X	X	X	L	H	L
$A_3=B_3$	$A_2>B_2$	X	X	X	X	X	H	L	L
$A_3=B_3$	$A_2<B_2$	X	X	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1>B_1$	X	X	X	X	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1<B_1$	X	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0>B_0$	X	X	X	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0<B_0$	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	L	L	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	H	L	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	L	H	L	L	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	X	X	H	L	L	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	H	L	L	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	L	L	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

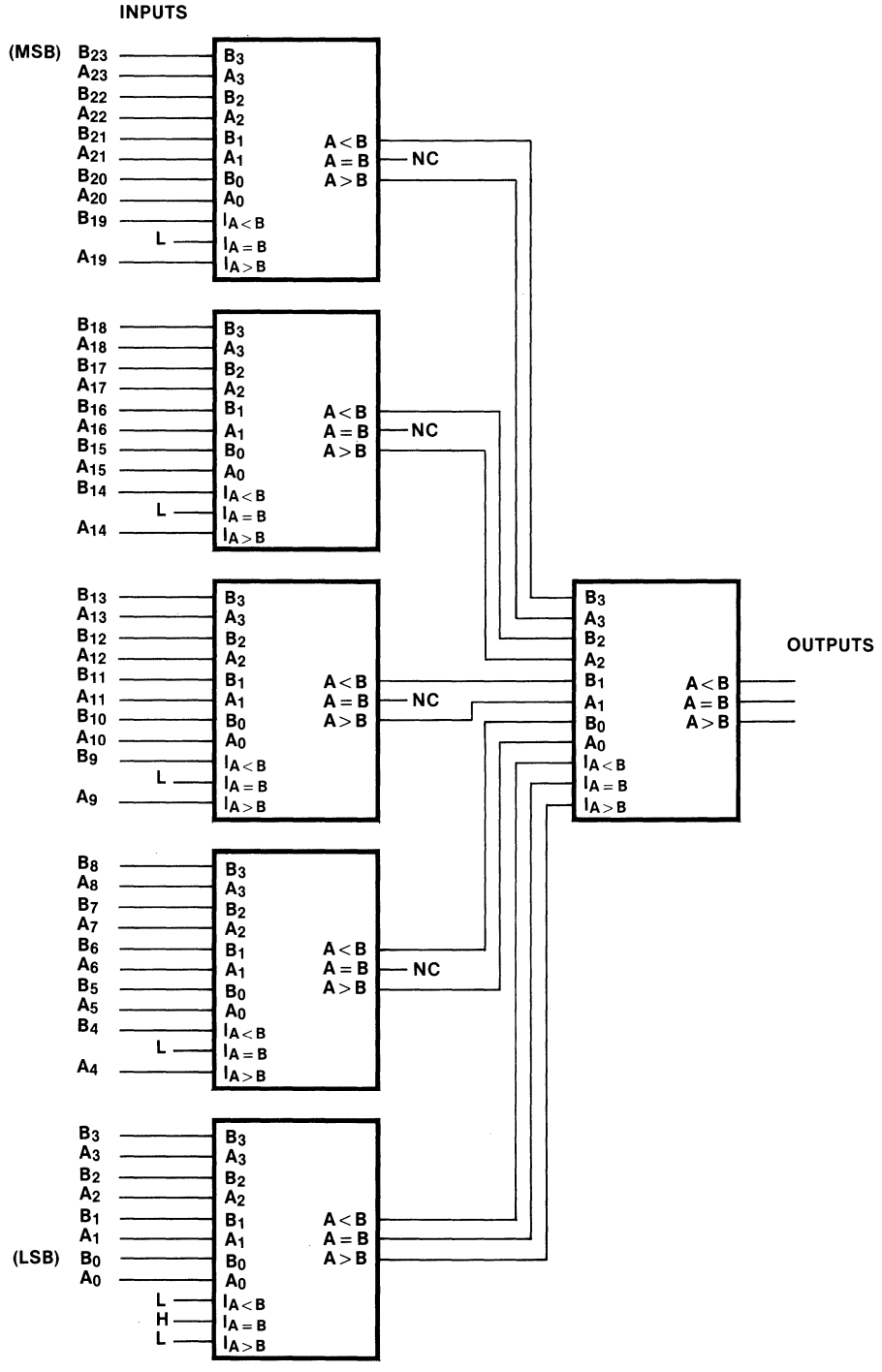
DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		32	47	mA	Outputs = OPEN, Inputs = Gnd, V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A or B to A<B or A>B		14.0 14.0						ns	3-1 3-3
t_{PLH} t_{PHL}	Propagation Delay A or B to A=B		14.0 11.5						ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay $I_{A<B}$ or $I_{A=B}$ to A>B		8.0 7.0						ns	3-1 3-3
t_{PLH} t_{PHL}	Propagation Delay $I_{A=B}$ to A=B		7.0 7.0						ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay $I_{A>B}$ or $I_{A=B}$ to A<B		8.0 7.0						ns	3-1 3-3

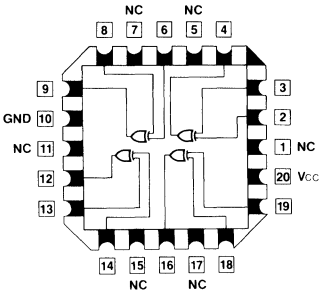
Comparison of Two 24-Bit Words



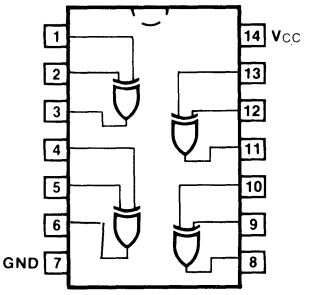
54F/74F86

Quad 2-Input Exclusive-OR Gate

Connection Diagrams



Pin Assignment for LCC and PCC



Pin Assignment for DIP and SOIC

Ordering Code: See Section 5

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
	Inputs Outputs	0.5/0.375 25/12.5

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions	
		Min	Typ	Max			
I_{CCL}	Power Supply Current		18	28	mA	Inputs HIGH	V_{CC} = Max
I_{CCH}			12	18		One Input LOW One Input HIGH	

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F $T_A = +25°C$ $V_{CC} = +5.0$ V $C_L = 50$ pF			54F T_A, V_{CC} = Mil $C_L = 50$ pF		74F T_A, V_{CC} = Com $C_L = 50$ pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay (Other Input LOW)	3.0 3.0	4.0 4.2	5.5 5.5	2.5 3.0	7.0 7.0	3.0 3.0	6.5 6.5	ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay (Other Input HIGH)	3.5 3.0	5.3 4.7	7.0 6.5	3.5 3.0	8.5 8.0	3.5 3.0	8.0 7.5	ns	3-1 3-3

54F/74F109

Dual J$\overline{K}$ Positive Edge-Triggered Flip-Flop

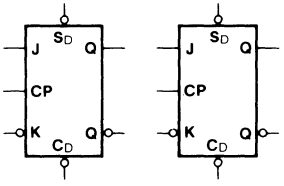
Description

The 'F109 consists of two high-speed, completely independent transition clocked J$\overline{K}$ flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The J$\overline{K}$ design allows operation as a D flip-flop (refer to 'F74 data sheet) by connecting the J and $\overline{K}$ inputs.

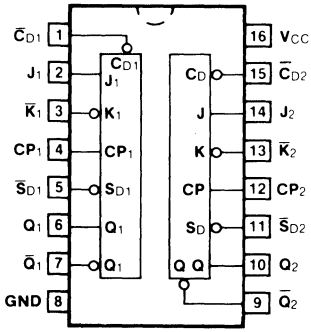
Asynchronous Inputs;
- LOW input to $\overline{S}_D$ sets Q to HIGH level
- LOW input to $\overline{C}_D$ sets Q to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

Ordering Code: See Section 5

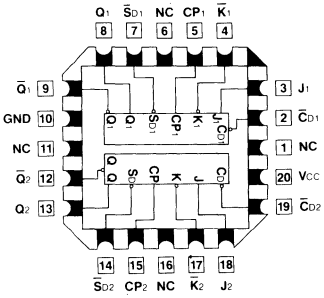
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

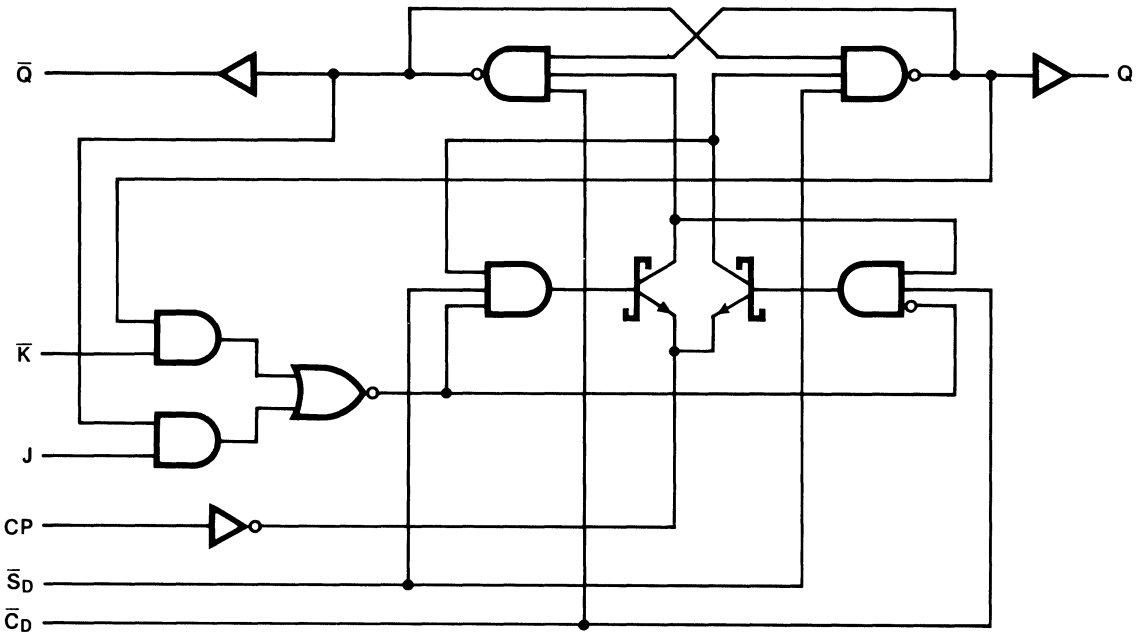
Pin Names	Description	54F/74F(U.L.) HIGH/LOW
J_1, J_2, $\overline{K}_1$, $\overline{K}_2$	Data Inputs	0.5/0.375
CP_1, CP_2	Clock Pulse Inputs (Active Rising Edge)	0.5/0.375
$\overline{C}_{D1}$, $\overline{C}_{D2}$	Direct Clear Inputs (Active LOW)	0.5/1.125
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct Set Inputs (Active LOW)	0.5/1.125
Q_1, Q_2, $\overline{Q}_1$, $\overline{Q}_2$	Outputs	25/12.5

Truth Table

Inputs		Outputs	
@ t_n		@ t_{n+1}	
J	$\overline{K}$	Q	$\overline{Q}$
L	H	No Change	
L	L	L	H
H	H	H	L
H	L	Toggles	

H = HIGH Voltage Level
L = LOW Voltage Level
t_n = Bit Time before Clock Pulse
t_{n+1} = Bit Time after Clock Pulse

Logic Diagram (one half shown)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		11.7	17.0	mA	V_{CC} = Max, V_{CP} = 0 V

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$			T_A, V_{CC} = Mil $C_L = 50\ pF$		T_A, V_{CC} = Com $C_L = 50\ pF$			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	100	125		70		90		MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	3.8 4.4	5.3 6.2	7.0 8.0	3.8 4.4	9.0 10.5	3.8 4.4	8.0 9.2	ns	3-1 3-7
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	3.2 3.5	5.2 7.0	7.0 9.0	3.2 3.5	9.0 11.5	3.2 3.5	8.0 10.5	ns	3-1 3-9

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW J_n or $\overline{K}_n$ to CP_n	3.0 3.0			3.0 3.0		3.0 3.0		ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW J_n or $\overline{K}_n$ to CP_n	1.0 1.0			1.0 1.0		1.0 1.0			
$t_w(H)$ $t_w(L)$	CP_n Pulse Width HIGH or LOW	4.0 5.0			4.0 5.0		4.0 5.0		ns	3-7
$t_w(L)$	$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width, LOW	4.0			4.0		4.0		ns	3-9
t_{rec}	Recovery Time $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP	2.0			2.0		2.0		ns	3-11

54F/74F112

Dual JK Negative Edge-Triggered Flip-Flop

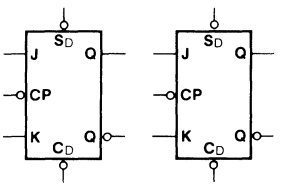
Description

The 'F112 contains two independent, high-speed JK flip-flops with Direct Set and Clear inputs. Synchronous state changes are initiated by the falling edge of the clock. Triggering occurs at a voltage level of the clock and is not directly related to the transition time. The J and K inputs can change when the clock is in either state without affecting the flip-flop, provided that they are in the desired state during the recommended setup and hold times relative to the falling edge of the clock. A LOW signal on $\overline{S}_D$ or $\overline{C}_D$ prevents clocking and forces Q or $\overline{Q}$ HIGH, respectively. Simultaneous LOW signals on $\overline{S}_D$ and $\overline{C}_D$ force both Q and $\overline{Q}$ HIGH.

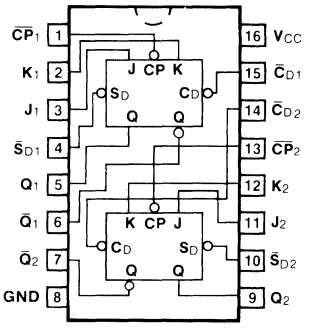
Asynchronous Inputs:
- LOW input to $\overline{S}_D$ sets Q to HIGH level
- LOW input to $\overline{C}_D$ sets Q to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

Ordering Code: See Section 5

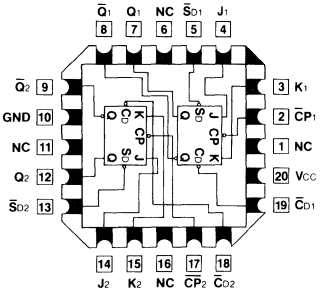
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

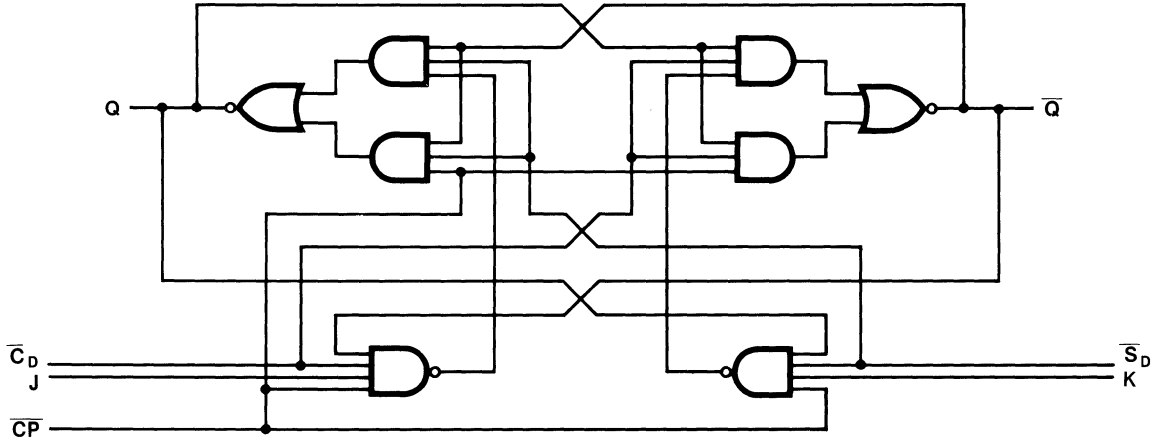
Pin Names	Description	54F/74F(U.L.) HIGH/LOW
J_1, J_2, K_1, K_2	Data Inputs	0.5/0.375
$\overline{CP}_1$, $\overline{CP}_2$	Clock Pulse Inputs (Active Falling Edge)	0.5/1.5
$\overline{C}_{D1}$, $\overline{C}_{D2}$	Direct Clear Inputs (Active LOW)	0.5/1.875
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct Set Inputs (Active LOW)	0.5/1.875
Q_1, Q_2, $\overline{Q}_1$, $\overline{Q}_2$	Outputs	25/12.5

Truth Table

Inputs		Output
$@t_n$		$@t_{n+1}$
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q_n}$

H = HIGH Voltage Level
L = LOW Voltage Level
t_n = Bit Time before Clock Pulse
t_{n+1} = Bit Time after Clock Pulse

Logic Diagram (one half shown)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		12	19	mA	V_{CC} = Max, V_{CP} = 0

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$			T_A, V_{CC} = Mil $C_L = 50\ pF$		T_A, V_{CC} = Com $C_L = 50\ pF$			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	110	130				100		MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}_n$ to Q_n or $\overline{Q}_n$	2.0 2.0	5.0 5.0	6.5 6.5			2.0 2.0	7.5 7.5	ns	3-1 3-8
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_{Dn}$, $\overline{S}_{Dn}$ to Q_n, $\overline{Q}_n$	2.0 2.0	4.5 4.5	6.5 6.5			2.0 2.0	7.5 7.5	ns	3-1 3-9

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW J_n or K_n to $\overline{CP}_n$	4.0 3.0					5.0 3.5		ns	3-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW J_n or K_n to $\overline{CP}_n$	0 0					0 0			
$t_w(H)$ $t_w(L)$	$\overline{CP}_n$ Pulse Width HIGH or LOW	4.5 4.5					5.0 5.0		ns	3-8
$t_w(L)$	$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width, LOW	4.5					5.0		ns	3-9
t_{rec}	$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to $\overline{CP}_n$ Recovery Time	4.0					5.0		ns	3-11

54F/74F113

Dual JK Edge-Triggered Flip-Flop

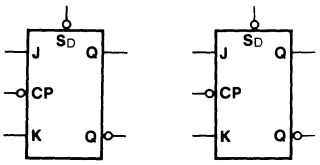
Description

The 'F113 offers individual J, K, Set and Clock inputs. When the clock goes HIGH the inputs are enabled and data may be entered. The logic level of the J and K inputs may be changed when the clock pulse is HIGH and the bistable will perform according to the Truth Table as long as minimum setup and hold times are observed. Input data is transferred to the outputs on the falling edge of the clock pulse.

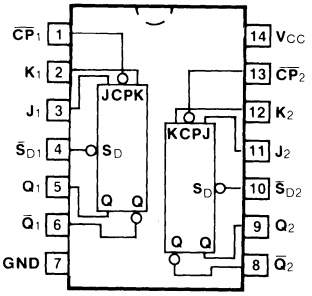
Asynchronous Input:
LOW input to $\overline{S}_D$ sets Q to HIGH level
Set is independent of clock

Ordering Code: See Section 5

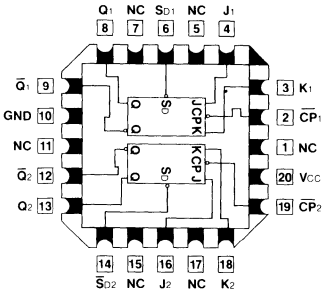
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

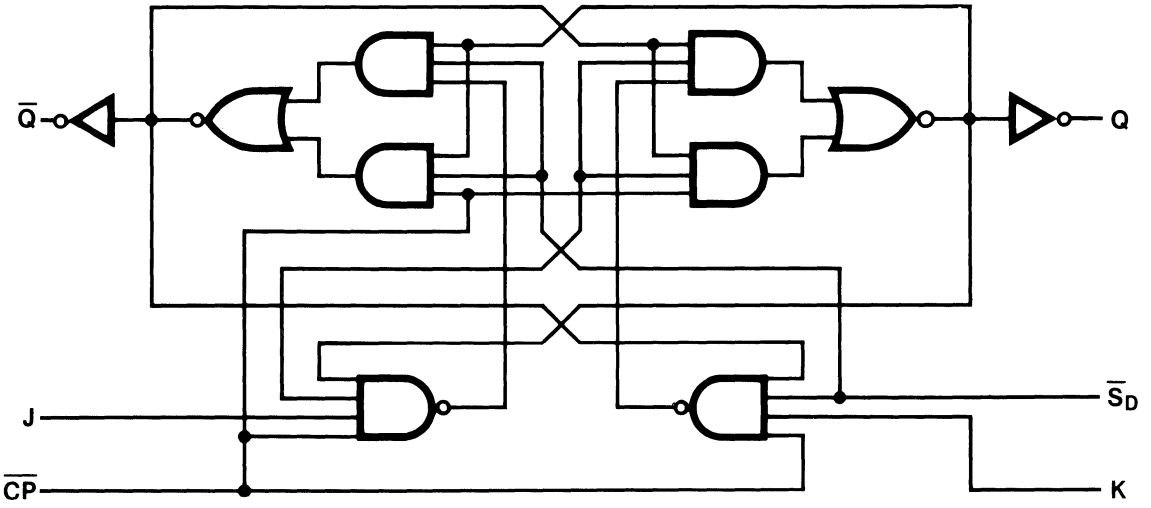
Pin Names	Description	54F/74F(U.L.) HIGH/LOW
J_1, J_2, K_1, K_2	Data Inputs	0.5/0.375
$\overline{CP}_1$, $\overline{CP}_2$	Clock Pulse Inputs (Active Falling Edge)	0.5/1.50
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct Set Inputs (Active LOW)	0.5/1.875
Q_1, Q_2, $\overline{Q}_1$, $\overline{Q}_2$	Outputs	25/12.5

Truth Table

Inputs		Output
@ t_n		@ t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

H = HIGH Voltage Level
L = LOW Voltage Level
t_n = Bit Time before Clock Pulse
t_{n+1} = Bit Time after Clock Pulse

Logic Diagram (one half shown)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		12	19	mA	V_{CC} = Max, V_{CP} = 0 V

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	110	125				100		MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}_n$ to Q_n or $\overline{Q}_n$	2.0 2.0	4.0 4.0	6.0 6.0			2.0 2.0	7.0 7.0	ns	3-1 3-8
t_{PLH} t_{PHL}	Propagation Delay $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	2.0 2.0	4.5 4.5	6.5 6.5			2.0 2.0	7.5 7.5	ns	3-1 3-9

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW J_n or K_n to $\overline{CP}_n$	4.0 3.0		5.0 3.5	ns	3-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW J_n or K_n to $\overline{CP}_n$	0 0		0 0		
$t_w(H)$ $t_w(L)$	$\overline{CP}_n$ Pulse Width HIGH or LOW	4.5 4.5		5.0 5.0	ns	3-8
$t_w(L)$	$\overline{S}_{Dn}$ Pulse Width, LOW	4.5		5.0	ns	3-9
t_{rec}	$\overline{S}_{Dn}$ to $\overline{CP}_n$ Recovery Time	4.0		5.0	ns	3-11

54F/74F114

Dual JK Negative Edge-Triggered Flip-Flop With Common Clocks and Clears

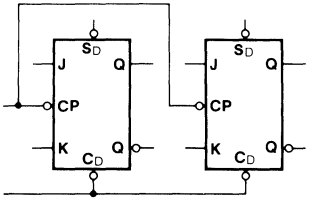
Description

The 'F114 contains two high-speed JK flip-flops with common Clock and Clear inputs. Synchronous state changes are initiated by the falling edge of the clock. Triggering occurs at a voltage level of the clock and is not directly related to the transition time. The J and K inputs can change when the clock is in either state without affecting the flip-flop, provided that they are in the desired state during the recommended setup and hold times relative to the falling edge of the clock. A LOW signal on $\overline{S}_D$ or $\overline{C}_D$ prevents clocking and forces Q or $\overline{Q}$ HIGH, respectively. Simultaneous LOW signals on $\overline{S}_D$ and $\overline{C}_D$ force both Q and $\overline{Q}$ HIGH.

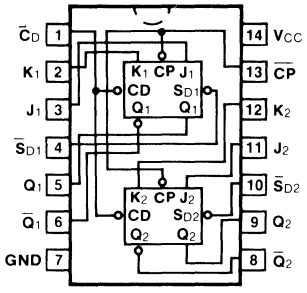
Asynchronous Inputs:
- LOW input to $\overline{S}_D$ sets Q to HIGH level
- LOW input to $\overline{C}_D$ sets Q to LOW level
- Clear and Set are independent of Clock
- Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

Ordering Code: See Section 5

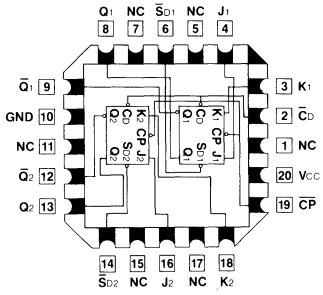
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

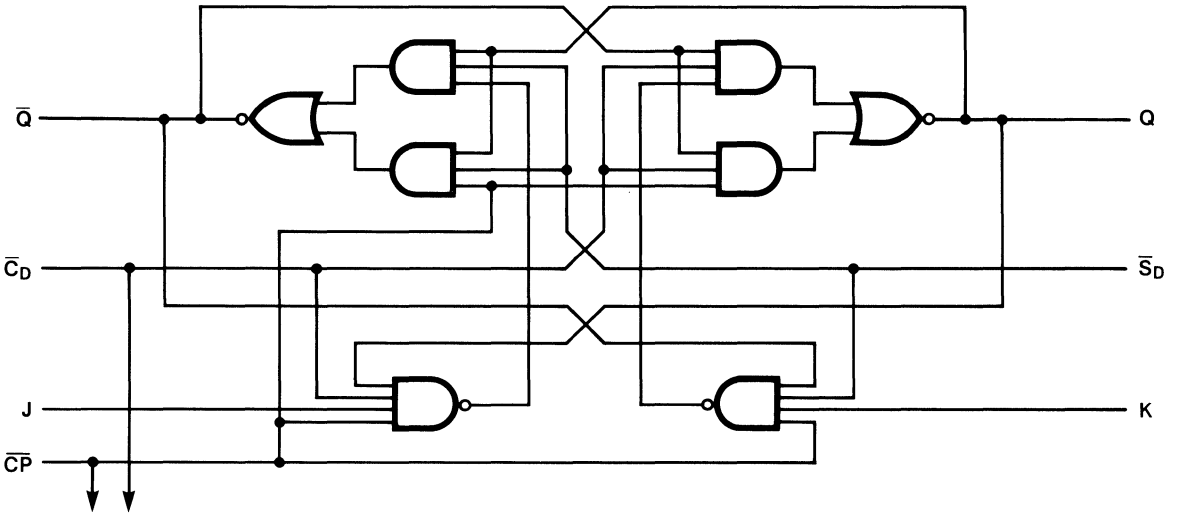
Pin Names	Description	54F/74F(U.L.) HIGH/LOW
J_1, J_2, K_1, K_2	Data Inputs	0.5/0.375
$\overline{CP}$	Clock Pulse Input (Active Falling Edge)	0.5/3.0
$\overline{C}_D$	Direct Clear Input (Active LOW)	0.5/3.7
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct Set Inputs (Active LOW)	0.5/1.875
Q_1, Q_2, $\overline{Q}_1$, $\overline{Q}_2$	Outputs	25/12.5

Truth Table

Inputs		Output
@t_n		@t_n
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

H = HIGH Voltage Level
L = LOW Voltage Level
t_n = Bit Time before Clock Pulse
t_{n+1} = Bit Time after Clock Pulse

Logic Diagram (one half shown)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		12	19	mA	V_{CC} = Max, V_{CP} = 0

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$			T_A, V_{CC} = Mil $C_L = 50\ pF$		T_A, V_{CC} = Com $C_L = 50\ pF$			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	100	125				90		MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to Q_n or $\overline{Q}_n$	3.0 3.0	5.0 5.5	6.5 7.5			3.0 3.0	7.5 8.5	ns	3-1 3-8
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_D$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	3.0 3.0	4.5 4.5	6.5 6.5			3.0 3.0	7.5 7.5	ns	3-1 3-9

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW J_n or K_n to $\overline{CP}$	4.0 3.0					5.0 3.5		ns	3-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW J_n or K_n to $\overline{CP}$	0 0					0 0			
$t_w(H)$ $t_w(L)$	$\overline{CP}$ Pulse Width HIGH or LOW	4.5 4.5					5.0 5.0		ns	3-8
$t_w(L)$	$\overline{C}_D$ or $\overline{S}_{Dn}$ Pulse Width, LOW	4.5					5.0		ns	3-9
t_{rec}	$\overline{C}_D$ or $\overline{S}_{Dn}$ to $\overline{CP}$ Recovery Time	4.0					5.0		ns	3-11

54F/74F132

Quad 2-Input NAND Schmitt Trigger

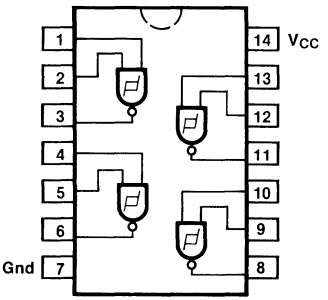
Description

The 'F132 contains four 2-input NAND gates which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have a greater noise margin than conventional NAND gates.

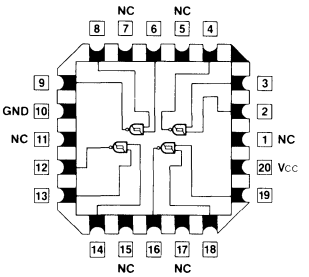
Each circuit contains a 2-input Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem-pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input threshold (typically 800 mV) is determined by resistor ratios and is essentially insensitive to temperature and supply voltage variations.

Ordering Code: See Section 5

Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
A, B	Inputs	0.5/0.375
O	Outputs	25/12.5

Function Table

Inputs		Outputs
A	B	O
L	L	H
L	H	H
H	L	H
H	H	L

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions	
		Min	Typ	Max			
I_{CCH}	Power Supply Current		8.5	12.0	mA	Outputs HIGH	V_{CC} = Max
I_{CCL}			13.0	19.5		Outputs LOW	

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay		7.0 8.5						ns	3-1 3-3

54F/74F138

1-of-8 Decoder/Demultiplexer

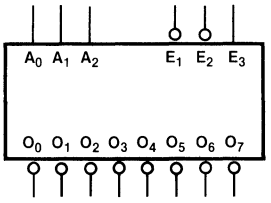
Description

The 'F138 is a high-speed 1-of-8 decoder/demultiplexer. This device is ideally suited for high-speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three 'F138 devices or a 1-of-32 decoder using four 'F138 devices and one inverter.

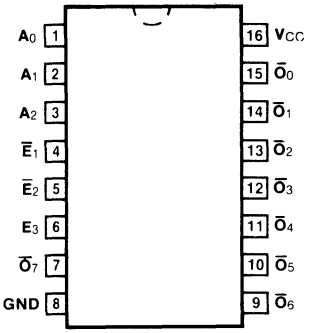
- **FAST Process for High Speed**
- **Demultiplexing Capability**
- **Multiple Input Enable for Easy Expansion**
- **Active LOW Mutually Exclusive Outputs**

Ordering Code: See Section 5

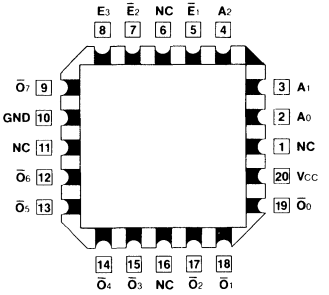
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
A_0-A_2	Address Inputs	0.5/0.375
$\overline{E}_1$, $\overline{E}_2$	Enable Inputs (Active LOW)	0.5/0.375
E_3	Enable Input (Active HIGH)	0.5/0.375
$\overline{O}_0$-$\overline{O}_7$	Outputs (Active LOW)	25/12.5

Functional Description

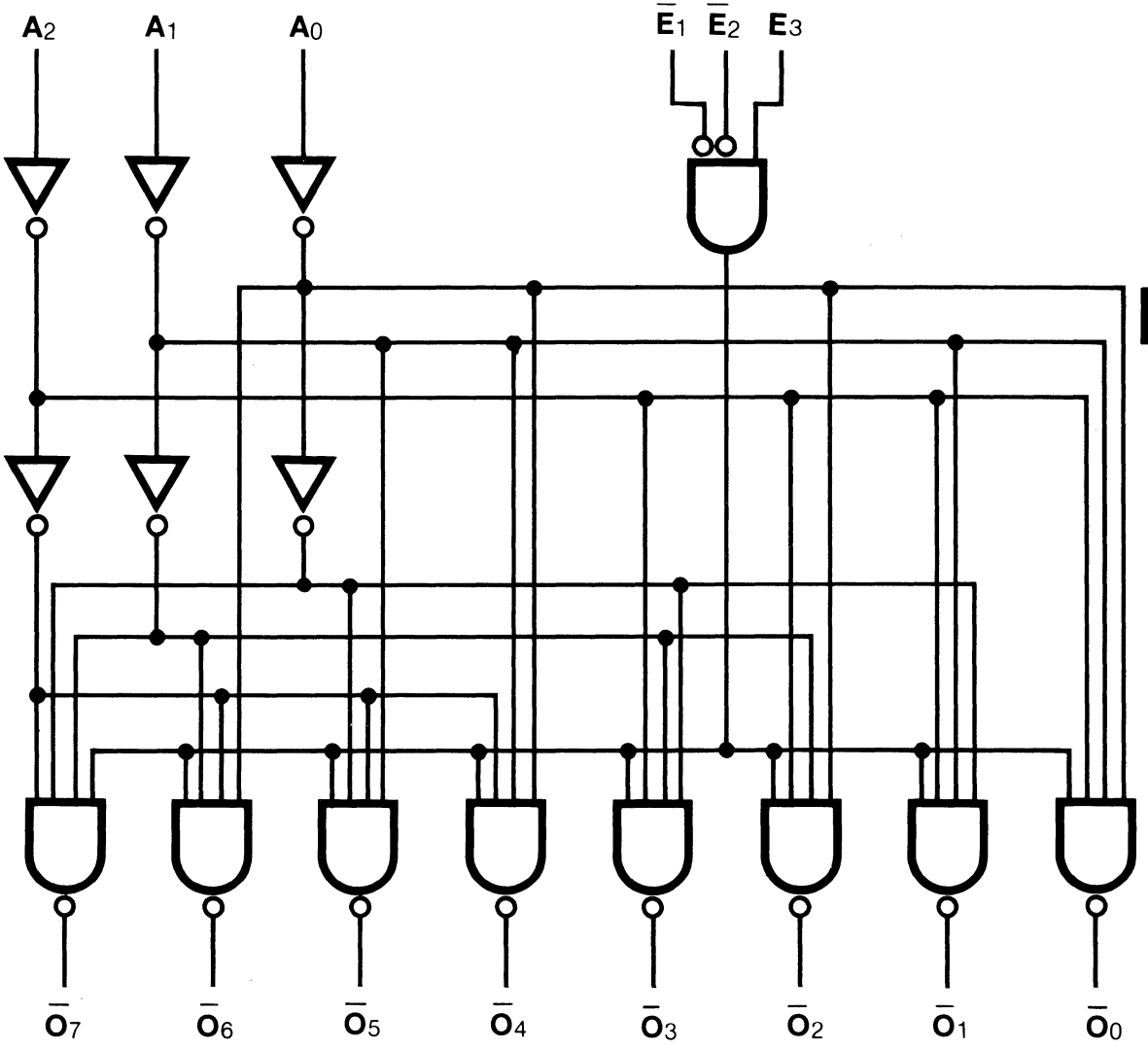
The 'F138 high-speed 1-of-8 decoder/multiplexer accepts three binary weighted inputs (A_0, A_1, A_2) and, when enabled, provides eight mutually exclusive active LOW outputs ($\overline{O}_0$-$\overline{O}_7$). The 'F138 features three Enable inputs, two active LOW ($\overline{E}_1$, $\overline{E}_2$) and one active HIGH (E_3). All outputs will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four 'F138 devices and one inverter (See Figure a). The 'F138 can be used as an 9-output demultiplexer by using one of the active LOW Enable inputs as the data input and the other Enable inputs as strobes. The Enable inputs which are not used must be permanently tied to their appropriate active HIGH or active LOW state.

Truth Table

Inputs						Outputs							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

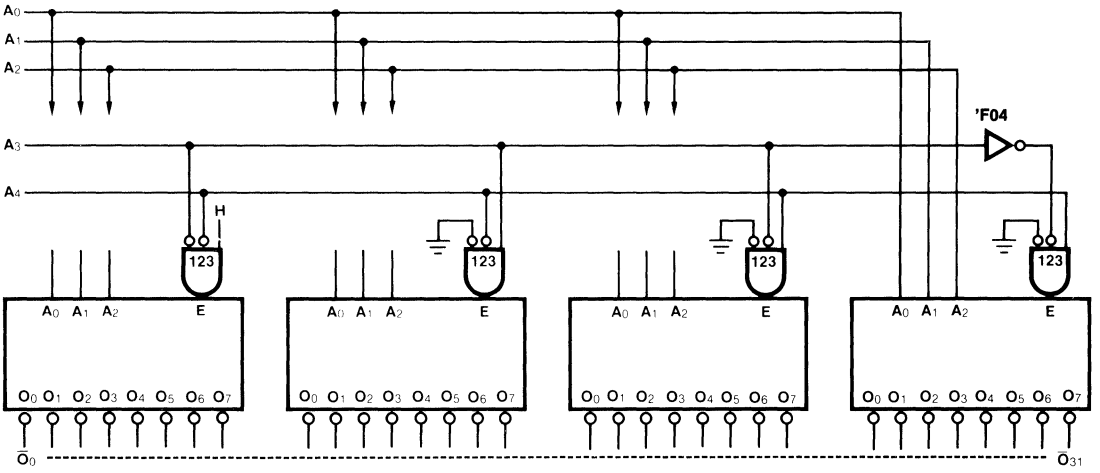
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Fig. a Expansion to 1-of-32 Decoding



DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		13	20	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	3.5	5.6	7.5	3.5	12.0	3.5	8.5	ns	3-1
t_{PHL}	A_n to $\overline{O}_n$	4.0	6.1	8.0	4.0	9.5	4.0	9.0		3-10
t_{PLH}	Propagation Delay	3.5	5.4	7.0	3.5	11.0	3.5	8.0	ns	3-1
t_{PHL}	$\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$	3.0	5.3	7.0	3.0	8.0	3.0	7.5		3-4
t_{PLH}	Propagation Delay	4.0	6.2	8.0	4.0	12.5	4.0	9.0	ns	3-1
t_{PHL}	E_3 to $\overline{O}_n$	3.5	5.6	7.5	3.5	8.5	3.5	8.5		3-3

54F/74F139

Dual 1-of-4 Decoder

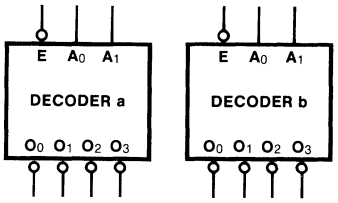
Description

The 'F139 is a high-speed, dual 1-of-4 decoder/demultiplexer. The device has two independent decoders, each accepting two inputs and providing four mutually exclusive active LOW outputs. Each decoder has an active LOW Enable input which can be used as a data input for a 4-output demultiplexer. Each half of the 'F139 can be used as a function generator providing all four minterms of two variables.

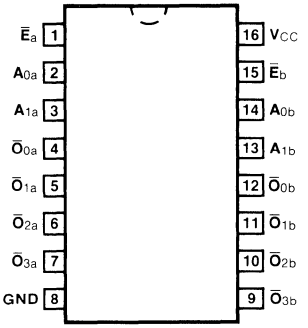
- **Multifunction Capability**
- **Two Completely Independent 1-of-4 Decoders**
- **Active LOW Mutually Exclusive Outputs**

Ordering Code: See Section 5

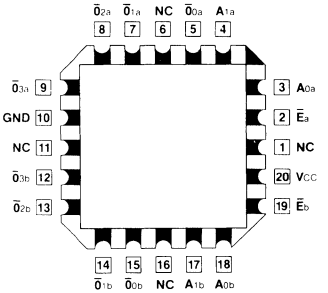
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC

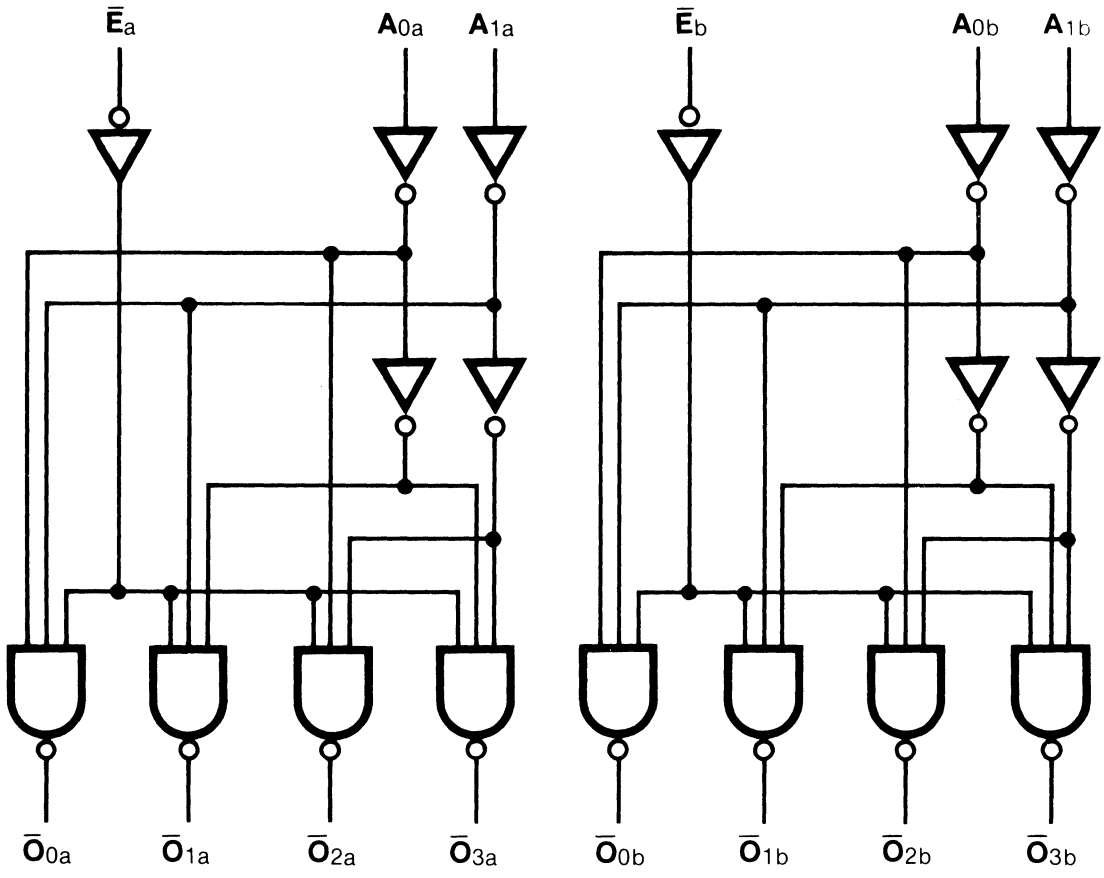


Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
A_0, A_1	Address Inputs	0.5/0.375
$\overline{E}$	Enable Inputs (Active LOW)	0.5/0.375
$\overline{O}_0$-$\overline{O}_3$	Outputs (Active LOW)	25/12.5

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Functional Description

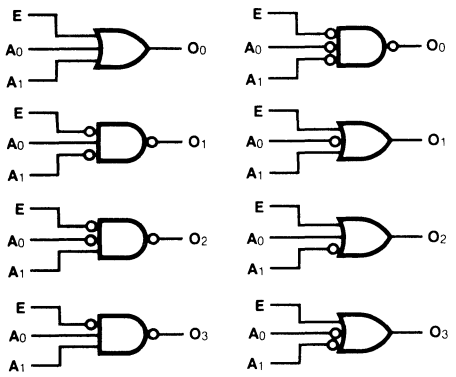
The 'F139 is a high-speed dual 1-of-4 decoder/demultiplexer. The device has two independent decoders, each of which accepts two binary weighed inputs (A_0-A_1) and provides four mutually exclusive active LOW outputs ($\overline{O}_0$-$\overline{O}_3$). Each decoder has an active LOW enable ($\overline{E}$). When $\overline{E}$ is HIGH all outputs are forced HIGH. The enable can be used as the data input for a 4-output demultiplexer application. Each half of the 'F139 generates all four minterms of two variables. These four minterms are useful in some applications, replacing multiple gate functions as shown in Figure a, and thereby reducing the number of packages required in a logic network.

Truth Table

Inputs			Outputs			
$\overline{E}$	A_0	A_1	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Fig. a Gate Functions (each half)



DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		13	20	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			54F T_A, V_{CC} = Mil C_L = 50 pF		74F T_A, V_{CC} = Com C_L = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_0 or A_1 to $\overline{O}_n$	3.5 4.0	5.3 6.1	7.5 8.0	2.5 3.5	12.0 9.5	3.0 4.0	8.5 9.0	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_1$ to $\overline{O}_n$	3.5 3.0	5.4 4.7	7.0 6.5	3.0 2.5	9.0 8.0	3.5 3.0	8.0 7.5	ns	3-1 3-4

54F/74F146

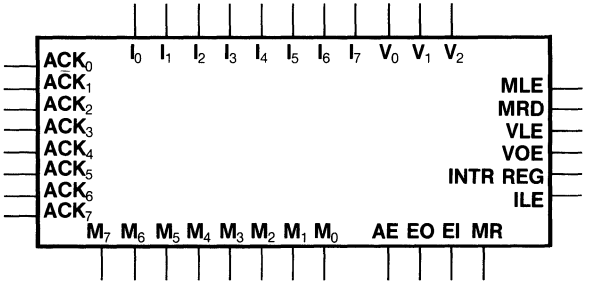
Priority Interrupt/DMA Request Controller

Description

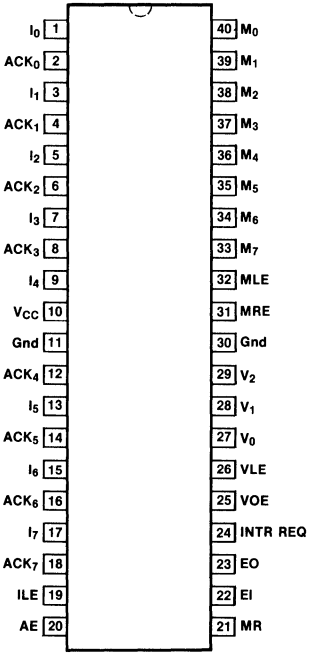
The 'F146 Priority Interrupt/DMA Request Controller is used to control the access of input and output units to the processing unit. The 'F146 can handle simultaneous or multiple requests according to their priority. Both a signal indicating an interrupt/DMA request and 3-bit binary coded vector of the the highest level interrupt are generated. Interrupt input and vector output latches are provided to add flexibility to the interrupt scheme. The mask latch provides masking capability of any level interrupt before prioritization. The I/O ports and control logic allow direct bus interfacing. The acknowledge outputs generate the bus acknowledge signals for DMA controlling or multi-processor environments.

Ordering Code: See Section 5

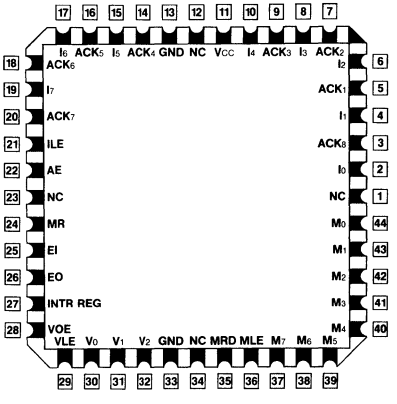
Logic Symbol



Connection Diagrams



Pin Assignment for DIP



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
$\overline{I}_0$-$\overline{I}_7$	Interrupt Pins	0.5/0.375
$\overline{ACK}_0$-$\overline{ACK}_7$	Acknowledge Outputs	25/12.5
ILE	Interrupt Latch Enable	0.5/0.375
$\overline{AE}$	Acknowledge Enable (Active LOW)	0.5/0.375
$\overline{MR}$	Master Reset	0.5/0.375
$\overline{INRQ}$	Interrupt Request	25/12.5
M_0-M_7	Mask Inputs	0.5/0.375
$\overline{CS}$	Mask Latch Address Select Line	0.5/0.375
R/$\overline{W}$	Mask Latch Read/Write Control Line	0.5/0.375
$\overline{V}_0$-$\overline{V}_2$	Priority Vector	25/12.5
VLE	Vector Latch Enable	0.5/0.375
$\overline{VOE}$	Vector Output Enable (Active LOW)	0.5/0.375
$\overline{EO}$	Expansion Output (Active LOW)	25/12.5
$\overline{EI}$	Expansion Input (Active LOW)	0.5/0.375

Functional Description

The basic function of the 'F146 Priority Interrupt/DMA Controller is as follows. The receipt of an interrupt signal from the Interrupting Peripheral generates an Interrupt Request signal, stopping the processor after the current instruction or bus cycle. The processor will respond by enabling the vector data generated by the 'F146 to be read on the data bus and generating an acknowledge enable signal. This Acknowledge signal is used by the 'F146 to generate the Peripheral Acknowledge signal and reset the Interrupt Request. The 'F146 consists of four major sections as described below:

Interrupt Latch

The interrupt latch is organized as eight SR latches. The Set input is used to catch negative transitions on the Interrupt ($\overline{I}_n$) inputs. Latch Enable (ILE) latches the current interrupt status and inhibits further changes. The Reset ($\overline{MR}$) input to each latch is fully overriding, resetting the latch regardless of the state of the ILE input. If both S and R are HIGH, the previous state of the Latch is held.

Mask Latch

The Mask Latch is an Octal Latched Transceiver. This latch allows changes to the interrupt scheme to be made dynamically by masking out chosen interrupts before prioritizing. The Address Select Line ($\overline{CS}$) selects the mask latch on the negative transition and the Latch Read/Write Control Line (R/$\overline{W}$) controls the Read/Write status of the mask latch. The Mask (M) I/O ports add the freedom of storing the current mask word for retrieval at a later time, thus requiring no register overhead.

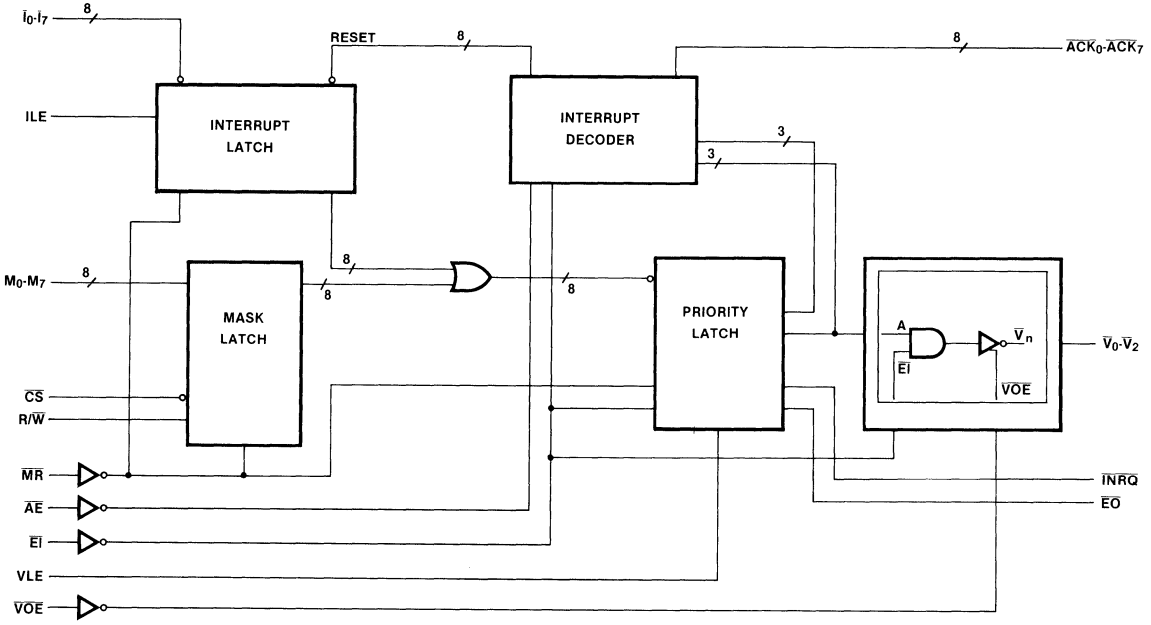
Priority Latch

The Priority Encoder ($\overline{V}_n$) and Vector Latch (VLE) can be integrated into one functional block. The Priority Latch encodes the eight interrupt lines (and the complements) providing a 3-bit binary vector. A priority is assigned to each input so that when two or more inputs are active, the one with the highest priority is represented by the vector output. The Expansion Input ($\overline{EI}$) and the Expansion Output ($\overline{EO}$) signals are provided for cascade expansion, with the $\overline{EO}$ being the more significant Priority Encoder driving the $\overline{EI}$ which is less significant. The latch is employed to prevent erroneous vector outputs during reading and peripheral acknowledge cycles. The Group Signal ($\overline{INRQ}$) provides direct detection of an interupt before vector generation is complete.

Interrupt Decoder

A 3-to-8 line decoder decodes the vector address generating the peripheral acknowledge outputs ($\overline{ACK}_n$) and the Interrupt Latch Reset ($\overline{MR}$) signals.

Block Diagram



DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		100	150	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F	54F	74F	Units
		$T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$	T_A, V_{CC} = Mil $C_L = 50\ pF$	T_A, V_{CC} = Com $C_L = 50\ pF$	
		Min Typ Max	Min Max	Min Max	
t_{PLH} t_{PHL}	Propagation Delay $\overline{I}$ to $\overline{INRQ}$	14.0 14.0			ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{EI}$ to $\overline{EO}$, $\overline{ACK_n}$, $\overline{V_n}$ or $\overline{INRQ}$	8.0 8.0			ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{CS}$ to $\overline{INRQ}$ or $\overline{V_n}$	14.0 14.0			ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{I_n}$ to $\overline{V_n}$	14.0 14.0			ns
t_{PLH} t_{PHL}	Propagation Delay ILE to $\overline{V_n}$	14.0 14.0			ns
t_{PLH} t_{PHL}	Propagation Delay ILE to $\overline{INRQ}$	14.0 14.0			ns
t_{PLH} t_{PHL}	Propagation Delay R/$\overline{W}$ to $\overline{INRQ}$ or $\overline{V_n}$	14.0 14.0			ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{MR}$ to $\overline{V_n}$	10.0 10.0			ns
t_{PLH} t_{PHL}	Propagation Delay VLE to $\overline{V_n}$	11.5 11.5			ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{AE}$ to $\overline{ACK_n}$	8.0 8.0			ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{MR}$ to $\overline{INRQ}$	14.0 14.0			ns
t_{PLH} t_{PHL}	Propagation Delay M_n to $\overline{INRQ}$ or $\overline{V_n}$	14.0 14.0			ns
t_{PHZ} t_{PLZ}	Output Enable Time $\overline{VOE}$ to $\overline{V_n}$	8.0 8.0			ns
t_{PZH} t_{PZL}	Output Disable Time $\overline{VOE}$ to $\overline{V_n}$	8.0 8.0			ns
t_{PHZ} t_{PLZ}	Output Enable Time $\overline{CS}$ or R/$\overline{W}$ to M_n	8.0 8.0			ns
t_{PZH} t_{PZL}	Propagation Delay $\overline{CS}$ or R/$\overline{W}$ to M_n	8.0 8.0			ns

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com	
		Min Typ Max	Min Max	Min Max	
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{I}_n$ to ILE	4.0 4.0			ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{I}_n$ to ILE	3.0 3.0			
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW M_n to $\overline{CS}$ or R/$\overline{W}$	4.0 4.0			ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW M_n to $\overline{CS}$ or R/$\overline{W}$	3.0 3.0			
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW M_n or $\overline{I}_n$ to VLE	7.0 7.0			ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW M_n or $\overline{I}_n$ to VLE	3.0 3.0			
$t_w(L)$	$\overline{MR}$ Pulse Width, LOW	6.0			ns
$t_w(L)$	ILE or VLE Pulse Width, LOW	6.0			ns
t_{rec}	Recovery Time $\overline{MR}$ to ILE	6.0			ns
t_{rec}	Recovery Time $\overline{MR}$ to $\overline{CS}$ or R/$\overline{W}$	6.0			ns

54F/74F148

8-Line to 3-Line Priority Encoder

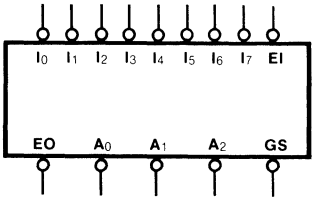
Description

The 'F148 provides three bits of binary coded output representing the position of the highest order active input, along with an output indicating the presence of any active input. It is easily expanded via input and output enables to provide priority encoding over many bits.

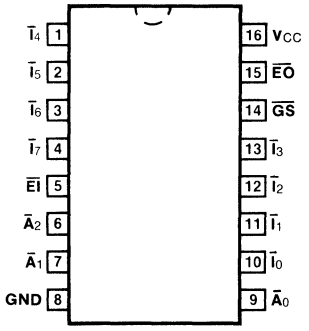
- **Encodes Eight Data Lines in Priority**
- **Provides 3-Bit Binary Priority Code**
- **Input Enable Capability**
- **Signals When Data Present on Any Input**
- **Cascadable for Priority Encoding of n Bits**

Ordering Code: See Section 5

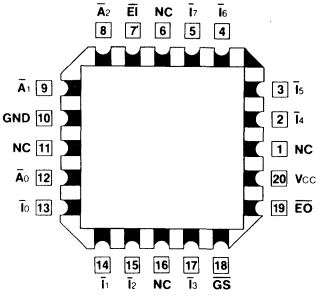
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
$\overline{I}_0$	Priority Input (Active LOW)	0.5/0.375
$\overline{I}_1$-$\overline{I}_7$	Priority Inputs (Active LOW)	0.5/0.75
$\overline{EI}$	Enable Input (Active LOW)	0.5/0.375
$\overline{EO}$	Enable Output (Active LOW)	25/12.5
$\overline{GS}$	Group Select Output (Active LOW)	25/12.5
$\overline{A}_0$-$\overline{A}_2$	Address Outputs (Active LOW)	25/12.5

Functional Description

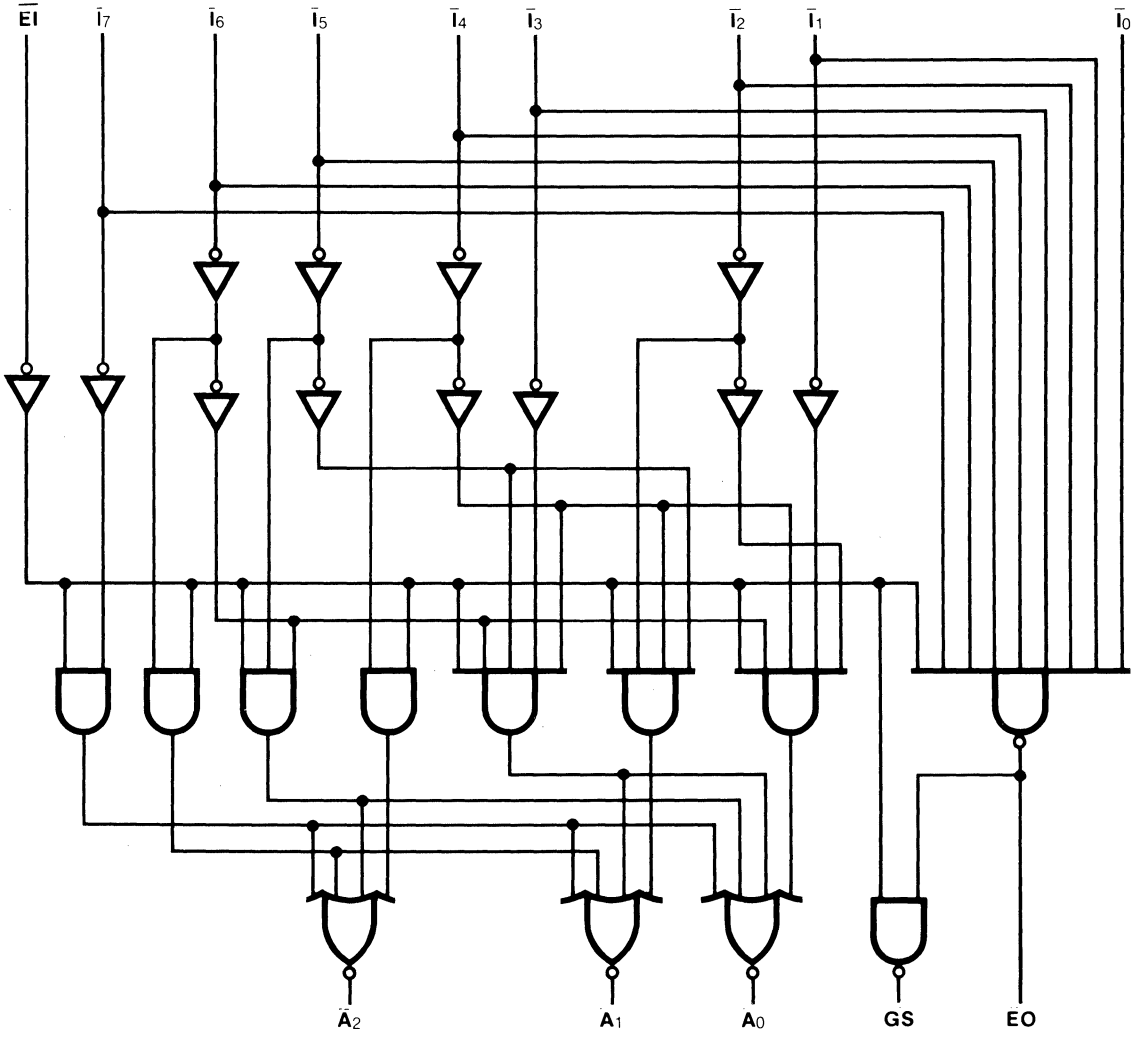
The 'F148 8-input priority encoder accepts data from eight active LOW inputs ($\overline{I}_0$-$\overline{I}_7$) and provides a binary representation on the three active LOW outputs. A priority is assigned to each input so that when two or more inputs are simultaneously active, the input with the highest priority is represented on the output, with input line 7 having the highest priority. A HIGH on the Enable Input ($\overline{EI}$) will force all outputs to the inactive (HIGH) state and allow new data to settle without producing erroneous information at the outputs. A Group Signal output ($\overline{GS}$) and Enable Output ($\overline{EO}$) are provided along with the three priority data outputs ($\overline{A}_2$, $\overline{A}_1$, $\overline{A}_0$). $\overline{GS}$ is active LOW when any input is LOW: this indicates when any input is active. $\overline{EO}$ is active LOW when all inputs are HIGH. Using the Enable Output along with the Enable Input allows cascading for priority encoding on any number of input signals. Both $\overline{EO}$ and $\overline{GS}$ are in the inactive HIGH state when the Enable Input is HIGH.

Truth Table

Inputs									Outputs				
$\overline{EI}$	$\overline{I}_0$	$\overline{I}_1$	$\overline{I}_2$	$\overline{I}_3$	$\overline{I}_4$	$\overline{I}_5$	$\overline{I}_6$	$\overline{I}_7$	$\overline{GS}$	$\overline{A}_0$	$\overline{A}_1$	$\overline{A}_2$	$\overline{EO}$
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	H	L	L	H
L	X	X	X	X	X	L	H	H	L	L	H	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	L	L	L	H	H
L	X	X	L	H	H	H	H	H	L	H	L	H	H
L	X	L	H	H	H	H	H	H	L	L	H	H	H
L	L	H	H	H	H	H	H	H	L	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

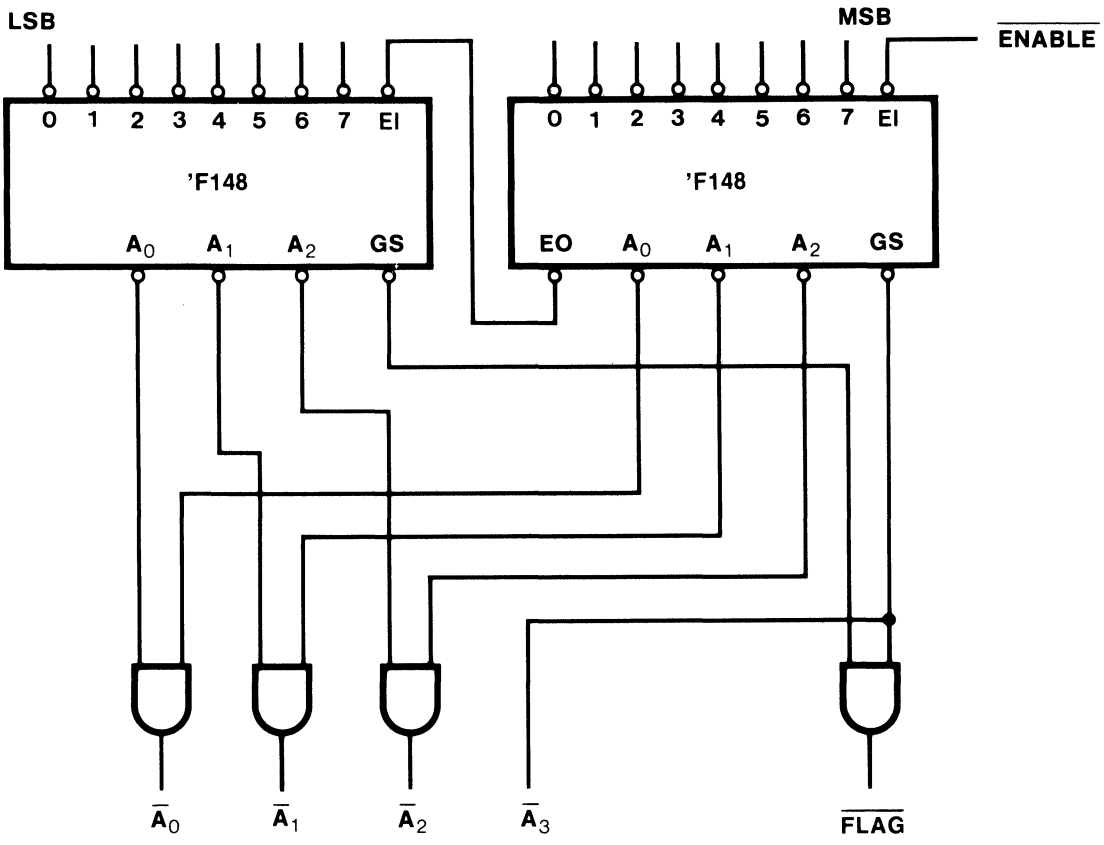
Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		23	35	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay $\overline{I}_n$ to $\overline{A}_n$	3.5 4.0	7.0 8.0	9.0 10.5			3.5 4.0	10.0 12.0	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay $\overline{I}_n$ to $\overline{EO}$	2.5 2.5	5.0 5.5	6.5 7.5			2.5 2.5	7.5 8.5	ns	3-1 3-3
t_{PLH} t_{PHL}	Propagation Delay $\overline{I}_n$ to $\overline{GS}$	3.0 2.0	7.0 6.0	9.0 8.0			3.0 2.0	10.0 9.0	ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay $\overline{EI}$ to $\overline{A}_n$	3.5 3.0	6.5 6.0	8.5 8.0			3.5 3.0	9.5 9.0	ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay $\overline{EI}$ to $\overline{GS}$	2.5 3.0	5.0 6.0	7.0 7.5			2.5 3.0	8.0 8.5	ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay $\overline{EI}$ to $\overline{EO}$	3.0 4.5	5.5 8.0	7.0 10.5			3.0 4.5	8.0 12.0	ns	3-1 3-4

Application

16-Input Priority Encoder



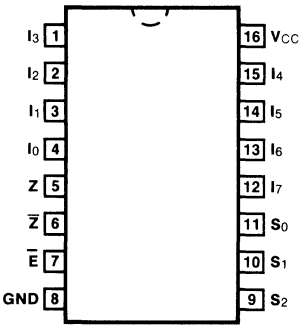
54F/74F151A

8-Input Multiplexer

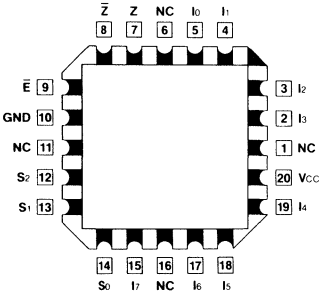
Description

The 'F151A is a high-speed 8-input digital multiplexer. It provides in one package the ability to select one line of data from up to eight sources. The 'F151A can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided.

Connection Diagrams



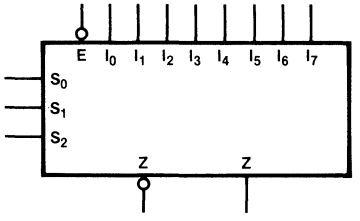
Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Ordering Code: See Section 5

Logic Symbol



Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
I_0-I_7	Data Inputs	0.5/0.375
S_0-S_2	Select Inputs	0.5/0.375
$\overline{E}$	Enable Input (Active LOW)	0.5/0.375
Z	Data Output	25/12.5
$\overline{Z}$	Inverted Data Output	25/12.5

Functional Description

The 'F151A is a logic implementation of a single pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0, S_1, S_2. Both assertion and negation outputs are provided. The Enable input ($\overline{E}$) is active LOW. When it is not activated, the negation output is HIGH and the assertion output is LOW regardless of all other inputs. The logic function provided at the output is:

$$Z = \overline{E} \bullet (I_0 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_1 \bullet S_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_2 \bullet \overline{S}_0 \bullet S_1 \bullet \overline{S}_2 + I_3 \bullet S_0 \bullet S_1 \bullet \overline{S}_2 + I_4 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet S_2 + I_5 \bullet S_0 \bullet \overline{S}_1 \bullet S_2 + I_6 \bullet \overline{S}_0 \bullet S_1 \bullet S_2 + I_1 \bullet S_0 \bullet S_1 \bullet S_2)$$

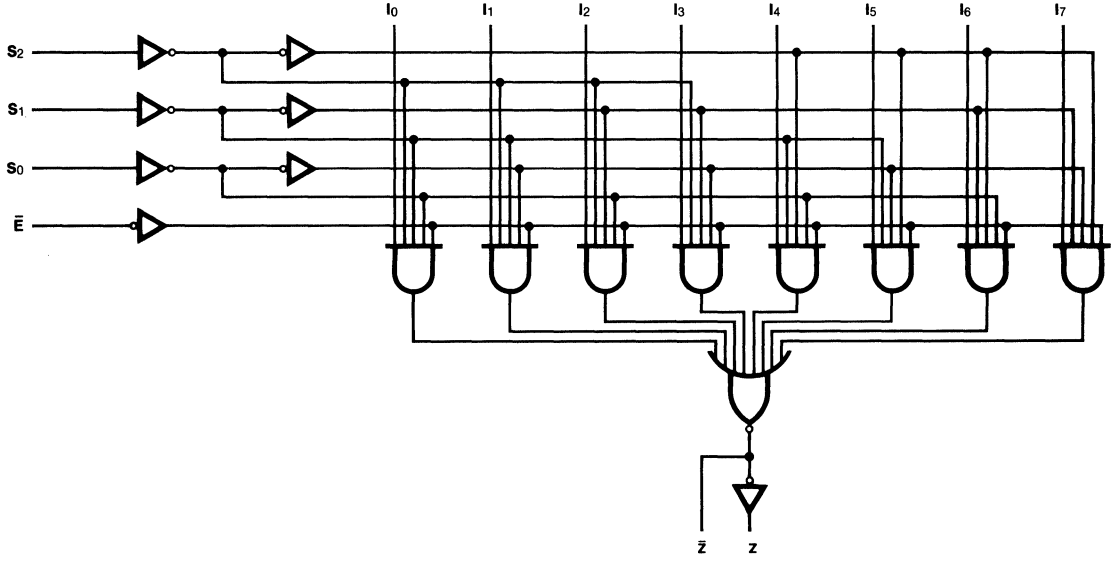
The 'F151A provides the ability, in one package, to select from eight sources of data or control information. By proper manipulation of the inputs, the 'F151A can provide any logic function of four variables and its negation.

Truth Table

Inputs				Outputs	
$\overline{E}$	S_2	S_1	S_0	$\overline{Z}$	Z
H	X	X	X	H	L
L	L	L	L	$\overline{I}_0$	I_0
L	L	L	H	$\overline{I}_1$	I_1
L	L	H	L	$\overline{I}_2$	I_2
L	L	H	H	$\overline{I}_3$	I_3
L	H	L	L	$\overline{I}_4$	I_4
L	H	L	H	$\overline{I}_5$	I_5
L	H	H	L	$\overline{I}_6$	I_6
L	H	H	H	$\overline{I}_7$	I_7

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		13.5	21.0	mA	V_{CC} = Max, V_{IN} = HIGH

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			54F T_A, V_{CC} = Mil C_L = 50 pF		74F T_A, V_{CC} = Com C_L = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{Z}$	4.0 3.2	6.2 5.2	9.0 7.5	3.5 3.0	11.5 8.0	3.5 3.2	9.5 7.5	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay S_n to Z	4.5 4.0	7.5 6.2	10.5 9.0	4.5 4.0	13.5 9.5	4.5 4.0	12.0 9.0	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to $\overline{Z}$	3.0 3.0	4.7 4.4	6.1 6.0	3.0 2.5	7.5 6.5	3.0 2.5	7.0 6.0	ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Z	5.0 3.5	7.0 5.3	9.5 7.0	4.0 3.0	12.0 8.0	4.0 3.0	10.5 7.5	ns	3-1 3-3
t_{PLH} t_{PHL}	Propagation Delay I_n to $\overline{Z}$	3.0 1.5	4.8 2.5	6.5 4.0	2.5 1.5	7.5 6.0	3.0 1.5	7.0 5.0	ns	3-1 3-3
t_{PLH} t_{PHL}	Propagation Delay I_n to Z	3.0 3.7	4.8 5.5	6.5 7.0	2.5 3.5	8.5 9.0	2.5 3.7	7.5 7.5	ns	3-1 3-4

54F/74F153

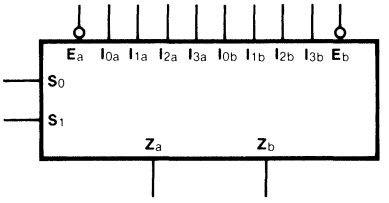
Dual 4-Input Multiplexer

Description

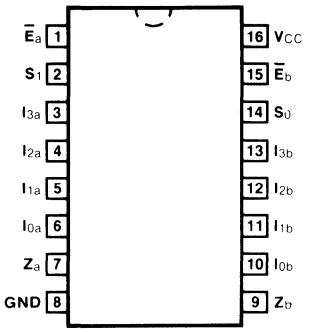
The 'F153 is a high-speed dual 4-input multiplexer with common select inputs and individual enable inputs for each section. It can select two lines of data from four sources. The two buffered outputs present data in the true (non-inverted) form. In addition to multiplexer operation, the 'F153 can generate any two functions of three variables.

Ordering Code: See Section 5

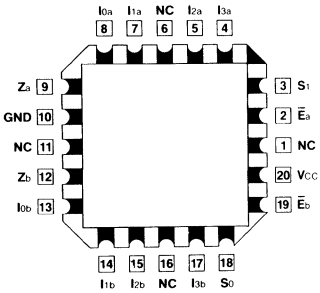
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
I_{0a}-I_{3a}	Side A Data Inputs	0.5/0.375
I_{0b}-I_{3b}	Side B Data Inputs	0.5/0.375
S_0, S_1	Common Select Inputs	0.5/0.375
$\overline{E}_a$	Side A Enable Input (Active LOW)	0.5/0.375
$\overline{E}_b$	Side B Enable Input (Active LOW)	0.5/0.375
Z_a	Side A Output	25/12.5
Z_b	Side B Output	25/12.5

Functional Description

The 'F153 is a dual 4-input multiplexer. It can select two bits of data from up to four sources under the control of the common Select inputs (S_0, S_1). The two 4-input multiplexer circuits have individual active LOW Enables ($\overline{E}_a$, $\overline{E}_b$) which can be used to strobe the outputs independently. When the Enables ($\overline{E}_a$, $\overline{E}_b$) are HIGH, the corresponding outputs (Z_a, Z_b) are forced LOW. The 'F153 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two Select inputs. The logic equations for the outputs are shown below.

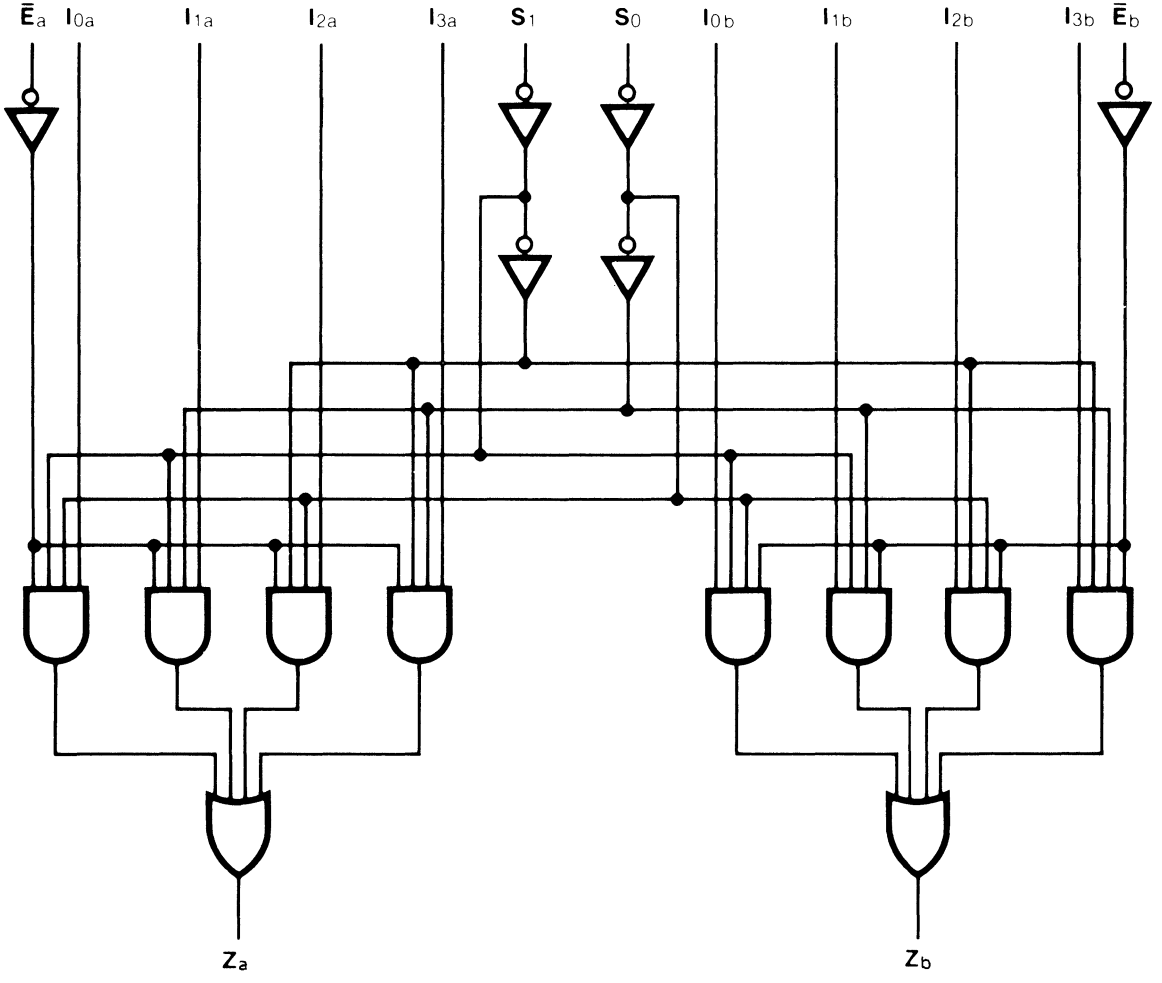
$$Z_a = \overline{E}_a \bullet (I_{0a} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1a} \bullet \overline{S}_1 \bullet S_0 + I_{2a} \bullet S_1 \bullet \overline{S}_0 + I_{3a} \bullet S_1 \bullet S_0)$$

$$Z_b = \overline{E}_b \bullet (I_{0b} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1b} \bullet \overline{S}_1 \bullet S_0 + I_{2b} \bullet S_1 \bullet \overline{S}_0 + I_{3b} \bullet S_1 \bullet S_0)$$

The 'F153 can be used to move data from a group of registers to a common output bus. The particular register from which the data came would be determined by the state of the Select inputs. A less obvious application is as a function generator. The 'F153 can generate two functions of three variables. This is useful for implementing highly irregular random logic.

4

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Truth Table

Select Inputs		Inputs (a or b)					Output
S_0	S_1	$\overline{E}$	I_0	I_1	I_2	I_3	Z
X	X	H	X	X	X	X	L
L	L	L	L	X	X	X	L
L	L	L	H	X	X	X	H
H	L	L	X	L	X	X	L
H	L	L	X	H	X	X	H
L	H	L	X	X	L	X	L
L	H	L	X	X	H	X	H
H	H	L	X	X	X	L	L
H	H	L	X	X	X	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		12	20	mA	V_{CC} = Max, V_{IN} = Gnd

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	4.5	8.1	10.5	4.5	14.0	4.5	12.0	ns	3-1
t_{PHL}	S_n to Z_n	3.5	7.0	9.0	3.5	11.0	3.5	10.5		3-10
t_{PLH}	Propagation Delay	4.5	7.1	9.0	4.5	11.5	4.5	10.5	ns	3-1
t_{PHL}	$\overline{E}_n$ to Z_n	3.0	5.7	7.0	2.5	9.0	2.5	8.0		3-3
t_{PLH}	Propagation Delay	3.0	5.3	7.0	2.5	9.0	3.0	8.0	ns	3-1
t_{PHL}	I_n to Z_n	3.0	5.1	6.5	2.5	8.0	2.5	7.5		3-4

54F/74F157A

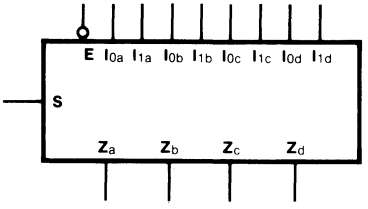
Quad 2-Input Multiplexer

Description

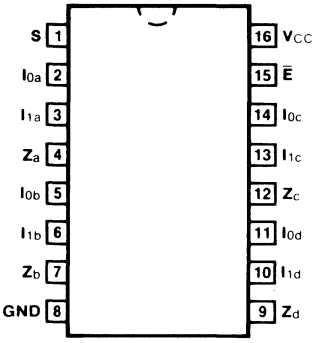
The 'F157A is a high-speed quad 2-input multiplexer. Four bits of data from two sources can be selected using the common Select and Enable inputs. The four buffered outputs present the selected data in the true (non-inverted) form. The 'F157A can also be used to generate any four of the 16 different functions to two variables.

Ordering Code: See Section 5

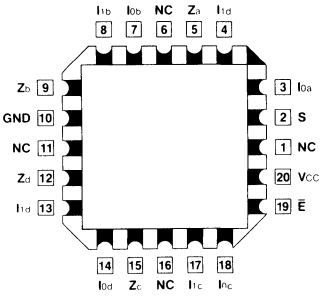
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
I_{0a}-I_{0d}	Source 0 Data Inputs	0.5/0.375
I_{1a}-I_{1d}	Source 1 Data Inputs	0.5/0.375
$\overline{E}$	Enable Input (Active LOW)	0.5/0.375
S	Select Input	0.5/0.375
Z_a-Z_d	Outputs	25/12.5

Functional Description

The 'F157A is a quad 2-input multiplexer. It selects four bits of data from two sources under the control of a common Select input (S). The Enable input ($\overline{E}$) is active LOW. When $\overline{E}$ is HIGH, all of the outputs (Z) are forced LOW regardless of all other inputs. The 'F157A is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$Z_a = \overline{E} \bullet (I_{1a} \bullet S + I_{0a} \bullet \overline{S})$$
$$Z_b = \overline{E} \bullet (I_{1b} \bullet S + I_{0b} \bullet \overline{S})$$
$$Z_c = \overline{E} \bullet (I_{1c} \bullet S + I_{0c} \bullet \overline{S})$$
$$Z_d = \overline{E} \bullet (I_{1d} \bullet S + I_{0d} \bullet \overline{S})$$

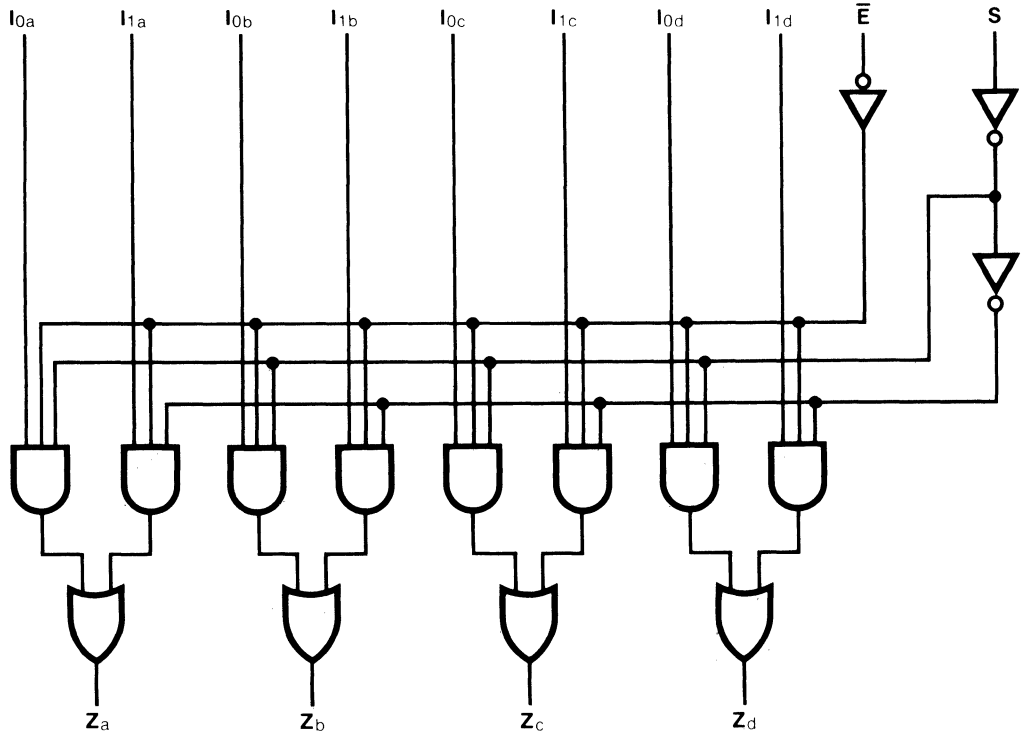
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

A common use of the 'F157A is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The 'F157A can generate any four of the 16 different functions of two variables with one variable common. This is useful for implementing highly irregular logic.

Truth Table

Inputs				Output
$\overline{E}$	S	I_0	I_1	Z
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		15	23	mA	V_{CC} = Max, All Inputs = HIGH

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay S to Z_n	4.0 3.0	7.0 5.0	10.0 7.0	4.0 3.0	12.0 9.0	4.0 3.0	11.0 8.0	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Z_n	5.0 2.5	7.0 4.5	9.5 6.5	5.0 2.5	13.0 7.5	5.0 2.5	11.0 7.0	ns	3-1 3-3
t_{PLH} t_{PHL}	Propagation Delay I_n to Z_n	2.5 2.5	4.5 4.0	6.0 5.5	2.5 1.5	7.5 7.5	2.5 2.0	6.5 7.0	ns	3-1 3-4

54F/74F158A

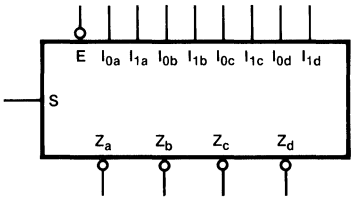
Quad 2-Input Multiplexer

Description

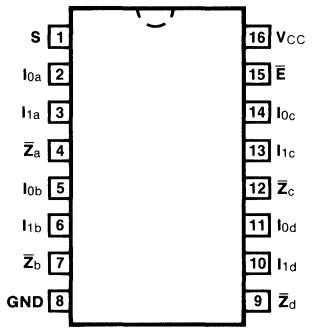
The 'F158A is a high-speed quad 2-input multiplexer. It selects four bits of data from two sources using the common Select and Enable inputs. The four buffered outputs present the selected data in the inverted form. The 'F158A can also generate any four of the 16 different functions of two variables.

Ordering Code: See Section 5

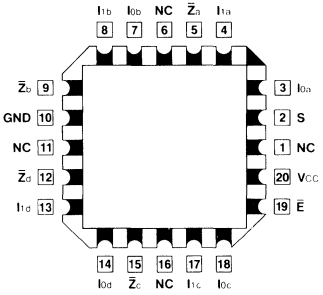
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PLCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
I_{0a}-I_{0d}	Source 0 Data Inputs	0.5/0.375
I_{1a}-I_{1d}	Source 1 Data Inputs	0.5/0.375
$\overline{E}$	Enable Input (Active LOW)	0.5/0.375
S	Select Input	0.5/0.375
$\overline{Z}_a$-$\overline{Z}_d$	Inverted Outputs	25/12.5

Functional Description

The 'F158A quad 2-input multiplexer selects four bits of data from two sources under the control of a common Select input (S) and presents the data in inverted form at the four outputs. The Enable input ($\overline{E}$) is active LOW. When $\overline{E}$ is HIGH, all of the outputs ($\overline{Z}$) are forced HIGH regardless of all other inputs. The 'F158A is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input.

A common use of the 'F158A is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The 'F158A can generate four functions of two variables with one variable common. This is useful for implementing gating functions.

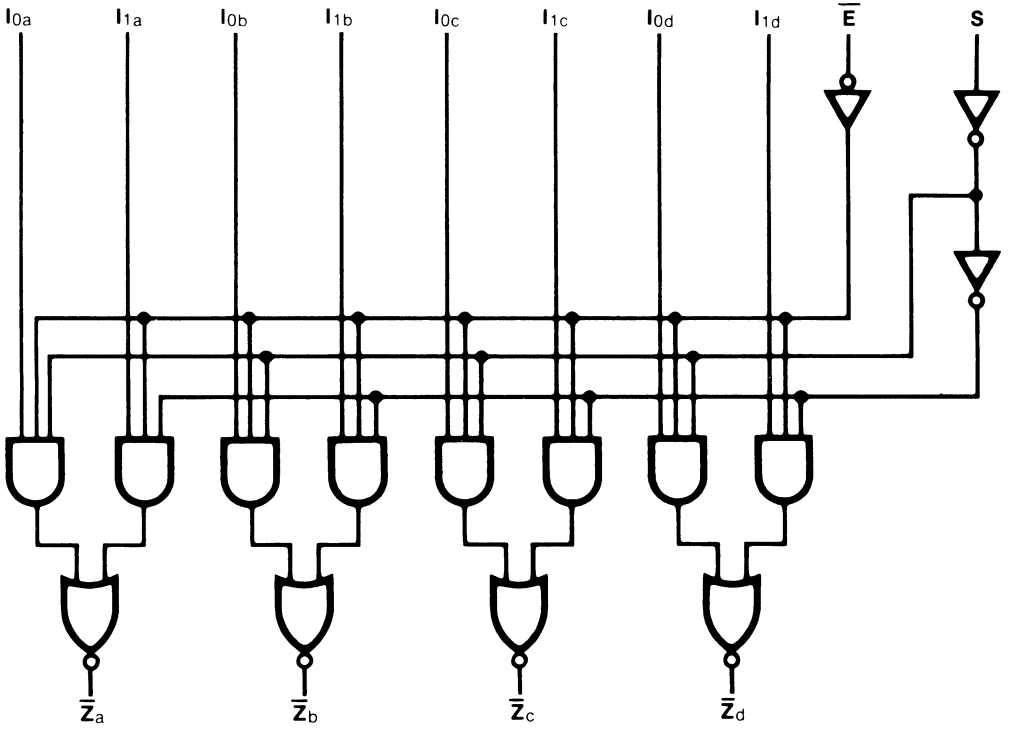
Truth Table

Inputs				Outputs
$\overline{E}$	S	I_0	I_1	$\overline{Z}$
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

4

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		10	15	mA	V_{CC} = Max, V_{IN} = HIGH

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay S to $\overline{Z}$	3.0 2.5	5.5 4.5	8.5 6.5	3.0 2.5	10.5 8.0	3.0 2.5	9.5 7.0	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to $\overline{Z}$	2.5 2.0	4.5 4.0	6.0 6.0	2.5 2.0	8.0 7.0	2.5 2.0	7.0 6.5	ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay I_n to $\overline{Z}$	2.5 1.5	4.0 2.5	5.9 4.0	2.5 1.5	8.5 5.0	2.5 1.5	7.0 4.5	ns	3-1 3-3

54F/74F160A • 54F/74F162A

Synchronous Presettable BCD Decade Counter

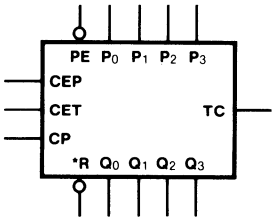
Description

The 'F160A and 'F162A are high-speed synchronous decade counters operating in the BCD (8421) sequence. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The 'F160A has an asynchronous Master Reset input that overrides all other inputs and forces the outputs LOW. The 'F162A has a Synchronous Reset input that overrides counting and parallel loading and allows all outputs to be simultaneously reset on the rising edge of the clock. The 'F160A and 'F162A are high speed versions of the 'F160 and 'F162.

- **Synchronous Counting and Loading**
- **High-Speed Synchronous Expansion**
- **Typical Count Rate of 120 MHz**

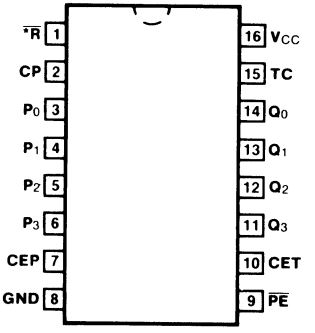
Ordering Code: See Section 5

Logic Symbol

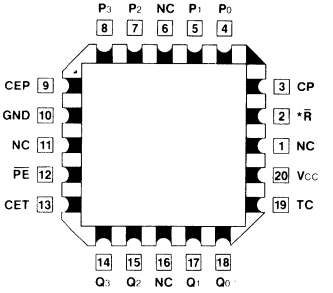


* $\overline{MR}$ for 'F160A
* $\overline{SR}$ for 'F162A

Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

* $\overline{MR}$ for 'F160A
* $\overline{SR}$ for 'F162A

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
CEP	Count Enable Parallel Input	0.5/0.375
CET	Count Enable Trickle Input	0.5/0.75
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
$\overline{MR}$ ('F160A)	Asynchronous Master Reset Input (Active LOW)	0.5/0.375
$\overline{SR}$ ('F162A)	Synchronous Reset Input (Active LOW)	0.5/0.75
P_0-P_3	Parallel Data Inputs	0.5/0.375
$\overline{PE}$	Parallel Enable Input (Active LOW)	0.5/0.75
Q_0-Q_3	Flip-Flop Outputs	25/12.5
TC	Terminal Count Output	25/12.5

Functional Description

The 'F160A and 'F162A count modulo-10 in the BCD (8421) sequence. From state 9 (HLLH) they increment to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset of the ('F160A) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset ('F160A), synchronous reset ('F162A), parallel load, count-up and hold. Five control inputs—Master Reset ($\overline{MR}$, 'F160A), Synchronous Reset ($\overline{SR}$, 'F162A), Parallel Enable ($\overline{PE}$), Count Enable Parallel (CEP) and Count Enable Trickle (CET)—determine the mode of operation, as shown in the Mode Select Table. A LOW signal on $\overline{MR}$ overrides all other inputs and asynchronously forces all outputs LOW. A LOW signal on $\overline{SR}$ overrides counting and parallel loading and allows all outputs to go LOW on the next rising edge of CP. A LOW signal on $\overline{PE}$ overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With $\overline{PE}$ and $\overline{MR}$ ('F160A) or $\overline{SR}$ ('F162A) HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

The 'F160A and 'F162A use D-type edge-triggered flip-flops and changing the $\overline{SR}$, $\overline{PE}$, CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

The Terminal Count (TC) output is HIGH when CET is HIGH and counter is in state 9. To implement synchronous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways. Please refer to the 'F568 data sheet. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, counters or registers. In the 'F160A and 'F162A decade counters, the TC output is fully decoded and can only be HIGH in state 9. If a decade counter is preset to an illegal state, or assumes an illegal state when power is applied, it will return to the normal sequence within two counts, as shown in the State Diagram.

Logic Equations: Count Enable = $CEP \bullet CET \bullet \overline{PE}$

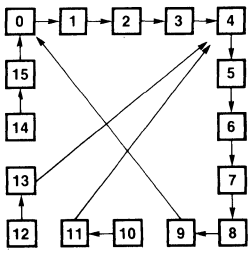
$TC = Q_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet Q_3 \bullet CET$

Mode Select Table

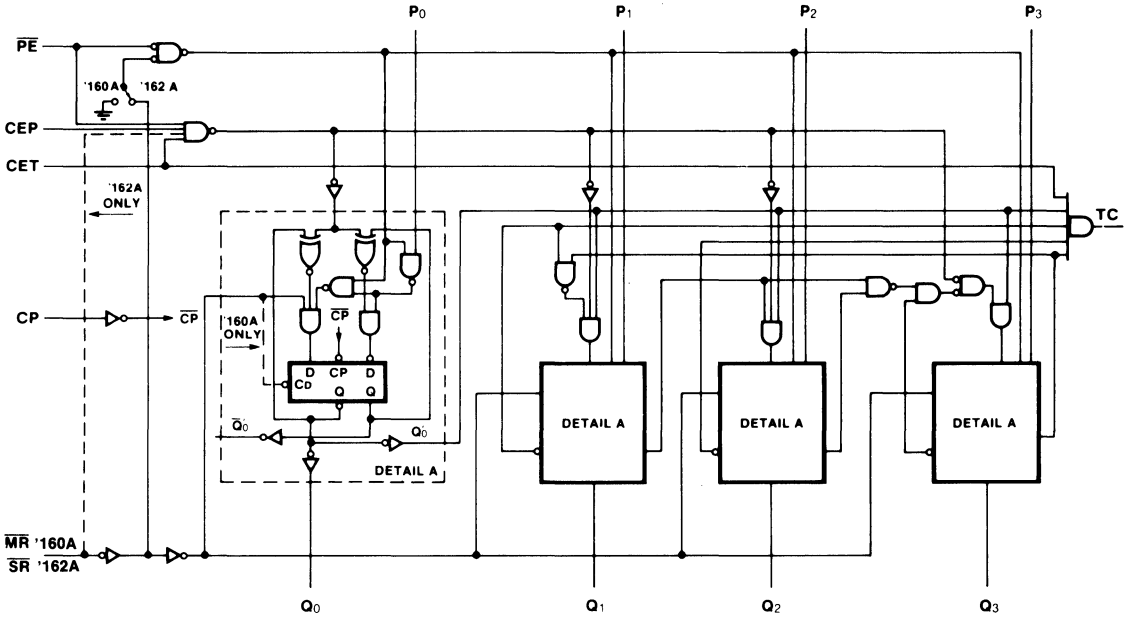
*$\overline{SR}$	$\overline{PE}$	CET	CEP	Action on the Rising Clock Edge (⌐)
L	X	X	X	Reset (Clear)
H	L	X	X	Load ($P_n \rightarrow Q_n$)
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

*For 'F162A only
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

State Diagram



Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		37	55	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F $T_A = +25°C$, $V_{CC} = +5.0\ V$, $C_L = 50\ pF$			54F T_A, V_{CC} = Mil, $C_L = 50\ pF$		74F T_A, V_{CC} = Com, $C_L = 50\ pF$		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Count Frequency	100	120		75		90		MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay, Count CP to Q_n ($\overline{PE}$ Input HIGH)	3.5 3.5	5.5 7.5	7.5 10.0	3.5 3.5	9.0 11.5	3.5 3.5	8.5 11.0	ns	3-1, 3-7
t_{PLH} t_{PHL}	Propagation Delay, Load CP to Q_n ($\overline{PE}$ Input LOW)	4.0 4.0	6.0 6.0	8.5 8.5	4.0 4.0	10.0 10.0	4.0 4.0	9.5 9.5		
t_{PLH} t_{PHL}	Propagation Delay CP to TC	5.0 5.0	10.0 10.0	14.0 14.0	5.0 5.0	16.5 15.5	5.0 5.0	15.0 15.0	ns	3-1 3-7
t_{PLH} t_{PHL}	Propagation Delay CET to TC	2.5 2.5	4.5 4.5	7.5 7.5	2.5 2.5	9.0 9.0	2.5 2.5	8.5 8.5	ns	3-1 3-4
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n ('F160A)	5.5	9.0	12.0	5.5	14.0	5.5	13.0	ns	3-1 3-11
t_{PHL}	Propagation Delay $\overline{MR}$ to TC ('F160A)	4.5	8.0	10.5	4.5	12.5	4.5	11.5	ns	3-1 3-11

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F $T_A = +25°C$ $V_{CC} = +5.0\,V$			54F T_A, V_{CC} = Mil		74F T_A, V_{CC} = Com		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW P_n to CP	5.0 5.0			5.5 5.5		5.0 5.0		ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW P_n to CP	2.0 2.0			2.5 2.5		2.0 2.0			
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP	11.0 8.5			13.5 10.5		11.5 9.5		ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP	2.0 0			2.0 0		2.0 0			
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW CEP or CET to CP	11.0 5.0			13.0 6.0		11.5 5.0		ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW CEP or CET to CP	0 0			0 0		0 0			
$t_w(H)$ $t_w(L)$	Clock Pulse Width (Load) HIGH or LOW	5.0 5.0			5.0 5.0		5.0 5.0		ns	3-7
$t_w(H)$ $t_w(L)$	Clock Pulse Width (Count) HIGH or LOW	4.0 6.0			5.0 8.0		4.0 7.0		ns	3-7
$t_w(L)$	$\overline{MR}$ Pulse Width, LOW ('F160A)	5.0			5.0		5.0		ns	3-11
t_{rec}	Recovery Time $\overline{MR}$ to CP ('F160A)	6.0			6.0		6.0			

54F/74F161A • 54F/74F163A

Synchronous Presettable Binary Counter

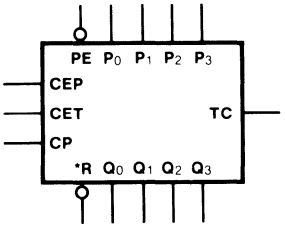
Description

The 'F161A and 'F163A are high-speed synchronous modulo-16 binary counters. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The 'F161A has an asynchronous Master Reset input that overrides all other inputs and forces the outputs LOW. The 'F163A has a Synchronous Reset input that overrides counting and parallel loading and allows the outputs to be simultaneously reset on the rising edge of the clock. The 'F161A and 'F163A are high-speed versions of the 'F161 and 'F163.

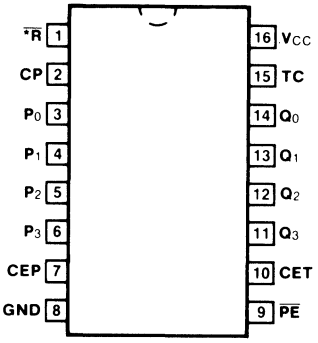
- **Synchronous Counting and Loading**
- **High-Speed Synchronous Expansion**
- **Typical Count Frequency of 120 MHz**

Ordering Code: See Section 5

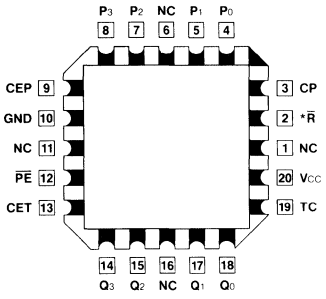
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



* $\overline{MR}$ for 'F161A
* $\overline{SR}$ for 'F163A

Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
CEP	Count Enable Parallel Input	0.5/0.375
CET	Count Enable Trickle Input	0.5/0.75
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
$\overline{MR}$ ('F161A)	Asynchronous Master Reset Input (Active LOW)	0.5/0.375
$\overline{SR}$ ('F163A)	Synchronous Reset Input (Active LOW)	0.5/0.75
P_0-P_3	Parallel Data Inputs	0.5/0.375
$\overline{PE}$	Parallel Enable Input (Active LOW)	0.5/0.75
Q_0-Q_3	Flip-Flop Outputs	25/12.5
TC	Terminal Count Output	25/12.5

Functional Description

The 'F161A and 'F163A count in modulo-16 binary sequence. From state 15 (HHHH) they increment to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset of the 'F161A) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset ('F161A), synchronous reset ('F163A), parallel load, count-up and hold. Five control inputs—Master Reset ($\overline{MR}$, 'F161A), Synchronous Reset ($\overline{SR}$, 'F163A), Parallel Enable ($\overline{PE}$), Count Enable Parallel (CEP) and Count Enable Trickle (CET)—determine the mode of operation, as shown in the Mode Select Table. A LOW signal on $\overline{MR}$ overrides all other inputs and asynchronously forces all outputs LOW. A LOW signal on $\overline{SR}$ overrides counting and parallel loading and allows all outputs to go LOW on the next rising edge of CP. A LOW signal on $\overline{PE}$ overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With $\overline{PE}$ and $\overline{MR}$ ('F161A) or $\overline{SR}$ ('F163A) HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

The 'F161A and 'F163A use D-type edge triggered flip-flops and changing the $\overline{SR}$, $\overline{PE}$, CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

The Terminal Count (TC) output is HIGH when CET is HIGH and the counter is in state 15. To implement synchronous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways. Please refer to the 'F568 data sheet. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, counters or registers.

Logic Equations: Count Enable = $CEP \bullet CET \bullet \overline{PE}$

$TC = Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3 \bullet CET$

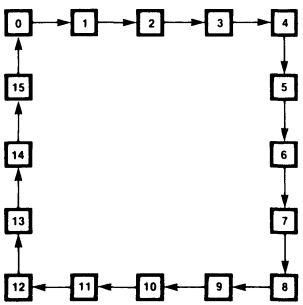
4

Mode Select Table

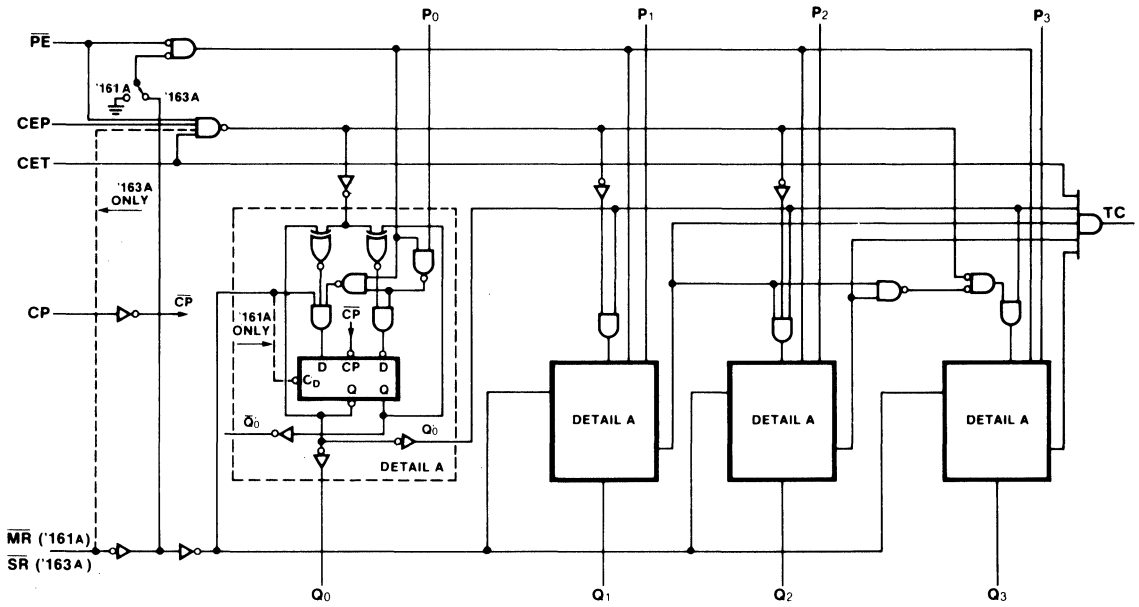
*$\overline{SR}$	$\overline{PE}$	CET	CEP	Action on the Rising Clock Edge (⌐)
L	X	X	X	Reset (Clear)
H	L	X	X	Load ($P_n \rightarrow Q_n$)
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

*For 'F163A only
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

State Diagram



Block Diagram



DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		37	55	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F $T_A = +25°C$, $V_{CC} = +5.0$ V, $C_L = 50$ pF			54F T_A, V_{CC} = Mil, $C_L = 50$ pF		74F T_A, V_{CC} = Com, $C_L = 50$ pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Count Frequency	100	120		75		90		MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH)	3.5 3.5	5.5 7.5	7.5 10.0	3.5 3.5	9.0 11.5	3.5 3.5	8.5 11.0	ns	3-1, 3-7
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ Input LOW)	4.0 4.0	6.0 6.0	8.5 8.5	4.0 4.0	10.0 10.0	4.0 4.0	9.5 9.5		
t_{PLH} t_{PHL}	Propagation Delay CP to TC	5.0 5.0	10.0 10.0	14.0 14.0	5.0 5.0	16.5 15.0	5.0 5.0	15.0 15.0	ns	3-1 3-7
t_{PLH} t_{PHL}	Propagation Delay CET to TC	2.5 2.5	4.5 4.5	7.5 7.5	2.5 2.5	9.0 9.0	2.5 2.5	8.5 8.5	ns	3-1 3-4
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n ('F161A)	5.5	9.0	12.0	5.5	14.0	5.5	13.0	ns	3-1 3-11
t_{PHL}	Propagation Delay $\overline{MR}$ to TC	4.5	8.0	10.5	4.5	12.5	4.5	11.5	ns	3-1 3-11

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F $T_A = +25°C$ $V_{CC} = +5.0\ V$			54F T_A, V_{CC} = Mil		74F T_A, V_{CC} = Com		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW P_n to CP	5.0 5.0			5.5 5.5		5.0 5.0		ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW P_n to CP	2.0 2.0			2.5 2.5		2.0 2.0			
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP	11.0 8.5			13.5 10.5		11.5 9.5		ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP	2.0 0			2.0 0		2.0 0			
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW CEP or CET to CP	11.0 5.0			13.0 6.0		11.5 5.0		ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW CEP or CET to CP	0 0			0 0		0 0			
$t_w(H)$ $t_w(L)$	Clock Pulse Width (Load) HIGH or LOW	5.0 5.0			5.0 5.0		5.0 5.0		ns	3-7
$t_w(H)$ $t_w(L)$	Clock Pulse Width (Count) HIGH or LOW	4.0 6.0			5.0 8.0		4.0 7.0		ns	3-7
$t_w(L)$	$\overline{MR}$ Pulse Width, LOW ('F161A)	5.0			5.0		5.0		ns	3-11
t_{rec}	Recovery Time $\overline{MR}$ to CP ('F161A)	6.0			6.0		6.0			

54F/74F164

Serial-In, Parallel-Out Shift Register

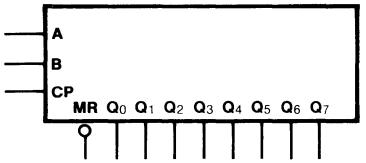
Description

The 'F164 is a high-speed 8-bit serial-in/parallel-out shift register. Serial data is entered through a 2-input AND gate synchronous with the LOW-to-HIGH transition of the clock. The device features an asynchronous Master Reset which clears the register, setting all outputs LOW independent of the clock.

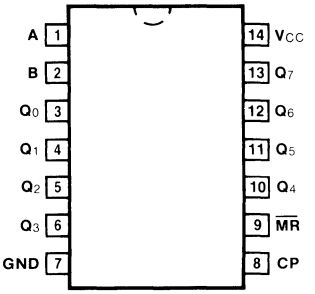
- **Typical Shift Frequency of 90 MHz**
- **Asynchronous Master Reset**
- **Gated Serial Data Input**
- **Fully Synchronous Data Transfers**

Ordering Code: See Section 5

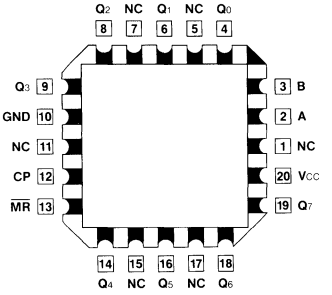
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
A, B	Data Inputs	0.5/0.375
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
$\overline{MR}$	Master Reset Input (Active LOW)	0.5/0.375
Q_0-Q_7	Outputs	25/12.5

Functional Description

The 'F164 is an edge-triggered 8-bit shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (A or B); either of these inputs can be used as an active HIGH Enable for data entry through the other input. An unused input must be tied HIGH.

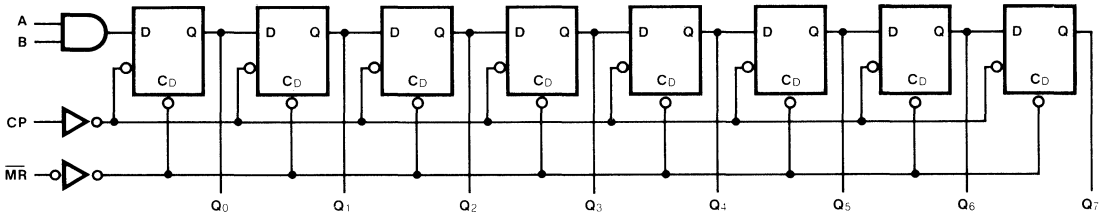
Each LOW-to-HIGH transition on the Clock (CP) input shifts data one place to the right and enters into Q_0 the logical AND of the two data inputs (A • B) that existed before the rising clock edge. A LOW level on the Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all Q outputs LOW.

Mode Select Table

Operating Mode	Inputs			Outputs	
	$\overline{MR}$	A	B	Q_0	Q_1-Q_7
Reset (Clear)	L	X	X	L	L-L
Shift	H	l	l	L	q_0-q_6
	H	l	h	L	q_0-q_6
	H	h	l	L	q_0-q_6
	H	h	h	H	q_0-q_6

H(h) = HIGH Voltage Levels
L(l) = LOW Voltage Levels
X = Immaterial
q_n = Lower case letters indicate the state of the referenced input or output one setup time prior to the LOW-to-HIGH clock transition.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		35	55	mA	A, B = Gnd, V_{CC} = Max CP = HIGH, $\overline{MR}$ = Gnd

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$			T_A, V_{CC} = Mil $C_L = 50\ pF$		T_A, V_{CC} = Com $C_L = 50\ pF$			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	80	90		70		80		MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n	4.5 5.0	6.0 7.5	8.0 10.0	4.5 5.0	11.0 13.0	4.5 5.0	9.0 11.0	ns	3-1 3-7
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	5.5	10.5	13.0	5.5	16.0	5.5	14.0	ns	3-1 3-11

4

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW A or B to CP	7.0 7.0			7.0 7.0		7.0 7.0		ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW A or B to CP	1.0 1.0			1.0 1.0		1.0 1.0			
$t_w(H)$ $t_w(L)$	CP Pulse Width HIGH or LOW	4.0 7.0			4.0 7.0		4.0 7.0		ns	3-7
$t_w(L)$	$\overline{MR}$ Pulse Width, LOW	7.0			7.0		7.0		ns	3-11
t_{rec}	Recovery Time $\overline{MR}$ to CP	7.0			7.0		7.0		ns	3-11

54F/74F168 • 54F/74F169

4-Stage Synchronous Bidirectional Counters

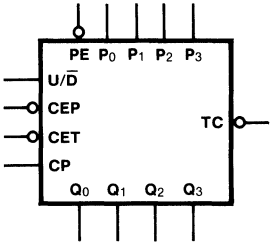
Description

The 'F168 and 'F169 are fully synchronous 4-stage up/down counters. The 'F168 is a BCD decade counter; the 'F169 is a modulo-16 binary counter. Both feature a preset capability for programmable operation, carry lookahead for easy cascading and a U/$\overline{D}$ input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the LOW-to-HIGH transition of the clock.

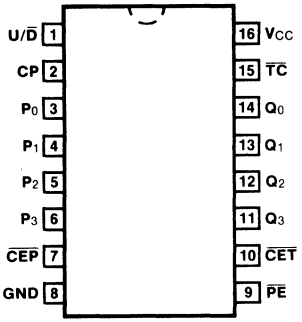
- **Asynchronous Counting and Loading**
- **Built-In Lookahead Carry Capability**
- **Presettable for Programmable Operation**

Ordering Code: See Section 5

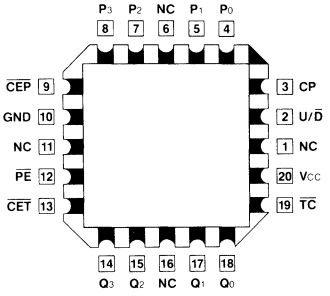
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
$\overline{CEP}$	Count Enable Parallel Input (Active LOW)	0.5/0.375
$\overline{CET}$	Count Enable Trickle Input (Active LOW)	0.5/0.75
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
P_0-P_3	Parallel Data Inputs	0.5/0.375
$\overline{PE}$	Parallel Enable Input (Active LOW)	0.5/0.375
U/$\overline{D}$	Up-Down Count Control Input	0.5/0.375
Q_0-Q_3	Flip-Flop Outputs	25/12.5
$\overline{TC}$	Terminal Count Output (Active LOW)	25/12.5

Functional Description

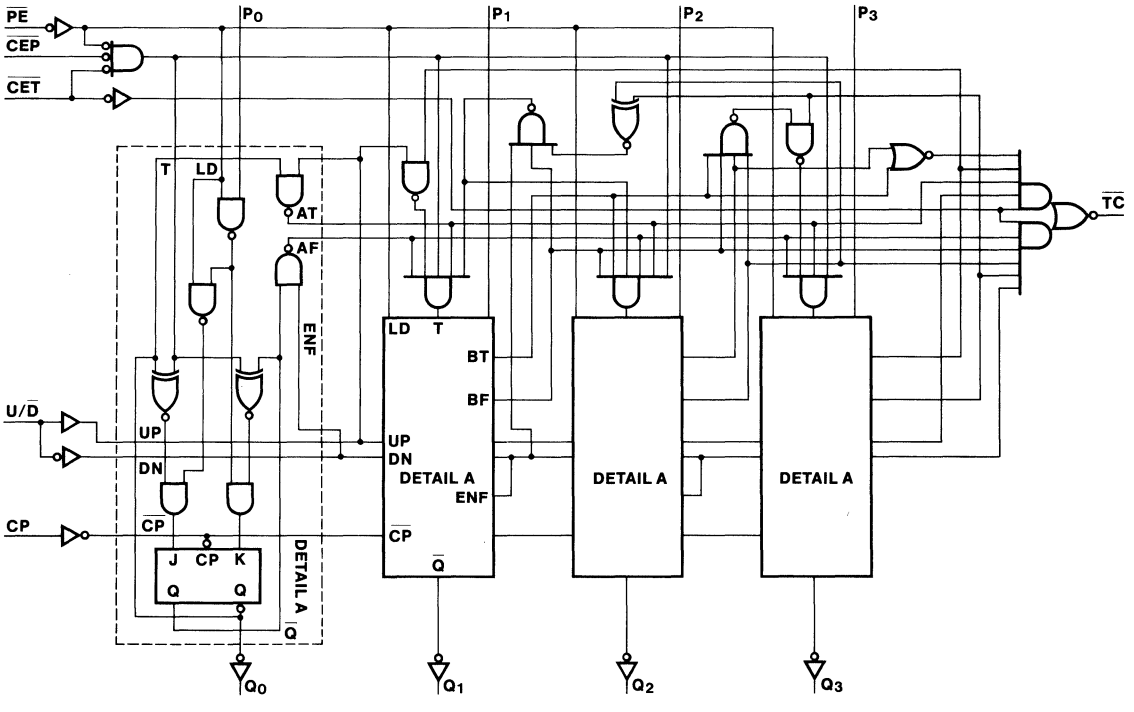
The 'F168 and 'F169 use edge-triggered J-K type flip-flops and have no constraints on changing the control or data input signals in either state of the clock. The only requirement is that the various inputs attain the desired state at least a setup time before the rising edge of the clock and remain valid for the recommended hold time thereafter. The parallel load operation takes precedence over other operations, as indicated in the Mode Select Table. When $\overline{PE}$ is LOW, the data on the P_0-P_3 inputs enters the flip-flops on the next rising edge of the clock. In order for counting to occur, both $\overline{CEP}$ and $\overline{CET}$ must be LOW and $\overline{PE}$ must be HIGH; the U/$\overline{D}$ input then determines the direction of counting. The Terminal Count ($\overline{TC}$) output is normally HIGH and goes LOW, provided that $\overline{CET}$ is LOW, when a counter reaches zero in the Count Down mode or reaches 9 (15 for the 'F169) in the Count Up mode. The $\overline{TC}$ output state is not a function of the Count Enable Parallel ($\overline{CEP}$) input level. The $\overline{TC}$ output of the 'F168 decade counter can also be LOW in the illegal states 11, 13, and 15, which can occur when power is turned on or via parallel loading. If an illegal state occurs, the 'F168 will return to the legitimate sequence within two counts. Since the $\overline{TC}$ signal is derived by decoding the flip-flop states, there exists the possibility of decoding spikes on $\overline{TC}$. For this reason the use of $\overline{TC}$ as a clock signal is not recommended (see logic equations below).

1) Count Enable = $\overline{CEP} \bullet \overline{CET} \bullet \overline{PE}$
2) Up: ('F168): $\overline{TC} = Q_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet Q_3 \bullet (\text{Up}) \bullet \overline{CET}$
   ('F169): $\overline{TC} = Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3 \bullet (\text{Up}) \bullet \overline{CET}$
3) Down: $\overline{TC} = \overline{Q}_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet \overline{Q}_3 \bullet (\text{Down}) \bullet \overline{CET}$

4

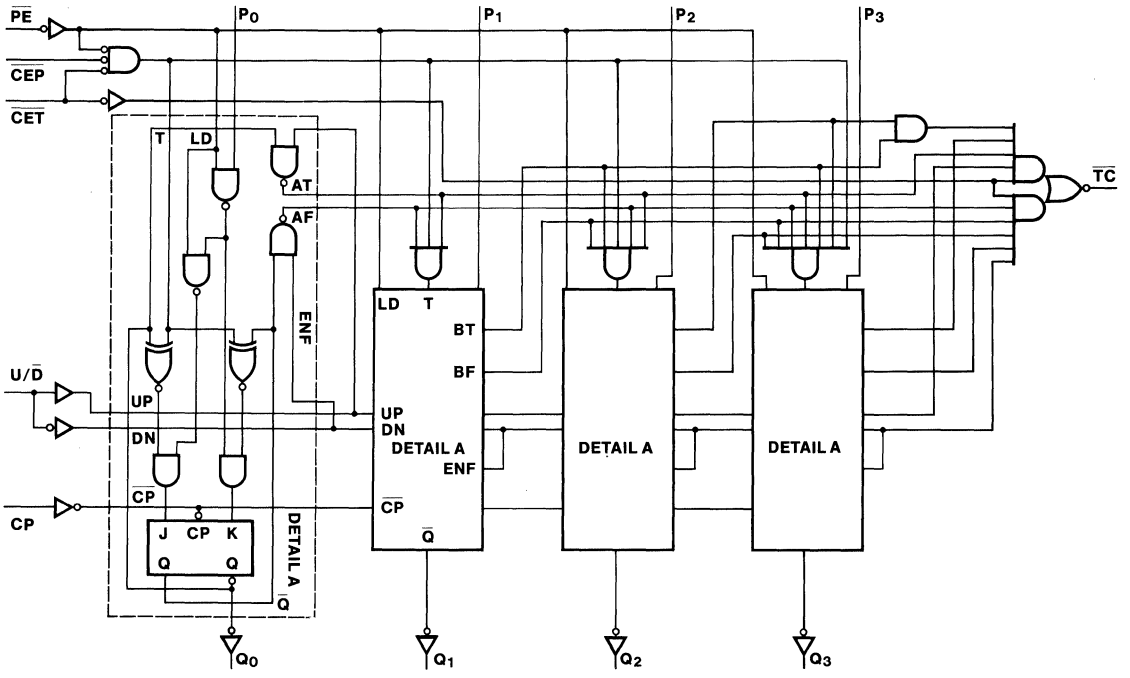
Logic Diagram

'F168



Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

'F169



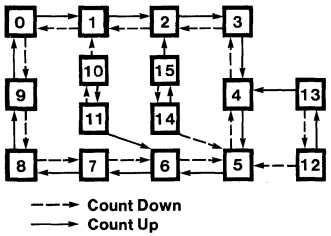
Mode Select Table

$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	U/$\overline{D}$	Action on Rising Clock Edge
L	X	X	X	Load ($P_n \rightarrow Q_n$)
H	L	L	H	Count Up (Increment)
H	L	L	L	Count Down (Decrement)
H	H	X	X	No Change (Hold)
H	X	H	X	No Change (Hold)

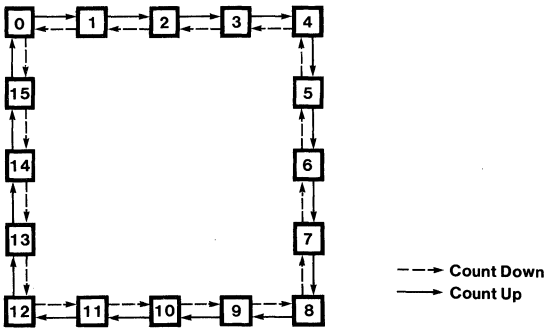
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

State Diagrams

'F168



'F169



DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		35	52	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			54F T_A, V_{CC} = Mil C_L = 50 pF		74F T_A, V_{CC} = Com C_L = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	100	115				90		MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ HIGH or LOW)	3.0 4.0	6.5 9.0	8.5 11.5			3.0 4.0	9.5 13.0	ns	3-1 3-7
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{TC}$	5.5 4.0	12.0 8.5	15.5 11.0			5.5 4.0	17.0 12.5	ns	3-1 3-7
t_{PLH} t_{PHL}	Propagation Delay $\overline{CET}$ to $\overline{TC}$	2.5 2.5	4.5 6.0	6.0 8.0			2.5 2.5	7.0 9.0	ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay ('F168) U/$\overline{D}$ to $\overline{TC}$	3.5 4.0	8.5 12.5	11.0 16.0			3.5 4.0	12.5 17.5	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay ('F169) U/$\overline{D}$ to $\overline{TC}$	3.5 4.0	8.5 8.0	11.0 10.5			3.5 4.0	12.5 12.0	ns	3-1 3-10

4

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\,V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW P_n to CP	4.0 4.0		4.5 4.5	ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW P_n to CP	3.0 3.0		3.5 3.5		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{CEP}$ or $\overline{CET}$ to CP	5.0 5.0		6.0 6.0	ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{CEP}$ or $\overline{CET}$ to CP	0 0		0 0		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{PE}$ to CP	8.0 8.0		9.0 9.0	ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{PE}$ to CP	0 0		0 0		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW U/$\overline{D}$ to CP ('F168)	11.0 16.5		12.5 18.0	ns	3-5
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW U/$\overline{D}$ to CP ('F169)	11.0 7.0		12.5 8.0		
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW U/$\overline{D}$ to CP	0 0		0 0		
$t_w(H)$ $t_w(L)$	CP Pulse Width HIGH or LOW	5.0 5.0		5.5 5.5	ns	3-7

54F/74F174

Hex D Flip-Flop With Master Reset

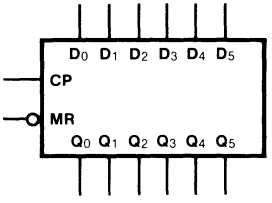
Description

The 'F174 is a high-speed hex D flip-flop. The device is used primarily as a 6-bit edge-triggered storage register. The information on the D inputs is transferred to storage during the LOW-to-HIGH clock transition. The device has a Master Reset to simultaneously clear all flip-flops.

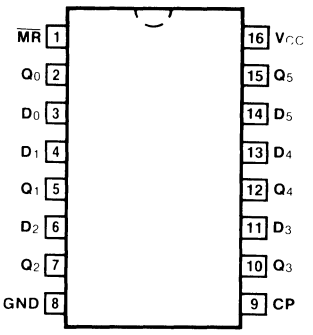
- **Edge-Triggered D-Type Inputs**
- **Buffered Positive Edge-Triggered Clock**
- **Asynchronous Common Reset**

Ordering Code: See Section 5

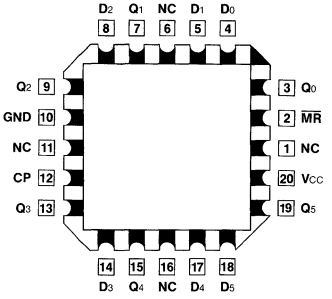
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
D_0-D_5	Data Inputs	0.5/0.375
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
$\overline{MR}$	Master Reset Input (Active LOW)	0.5/0.375
Q_0-Q_5	Outputs	25/12.5

Functional Description

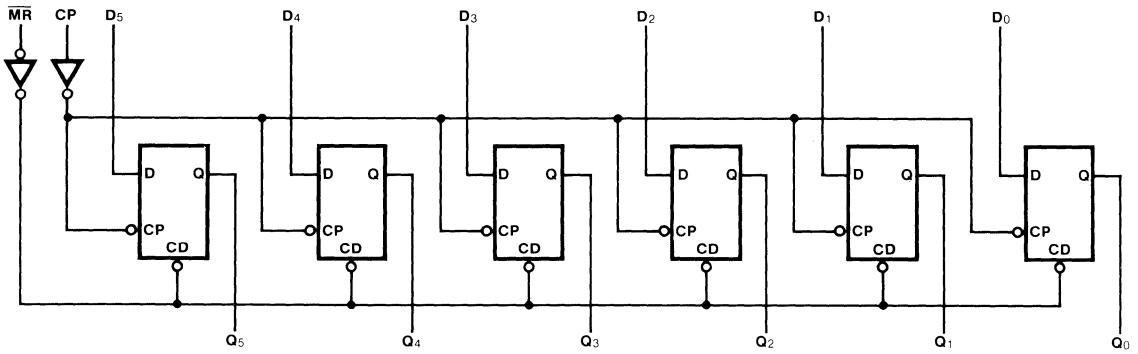
The 'F174 consists of six edge-triggered D flip-flops with individual D inputs and Q outputs. The Clock (CP) and Master Reset ($\overline{MR}$) are common to all flip-flops. Each D input's state is transferred to the corresponding flip-flop's output following the LOW-to-HIGH Clock (CP) transition. A LOW input to the Master Reset ($\overline{MR}$) will force all outputs LOW independent of Clock or Data inputs. The 'F174 is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

Truth Table

Inputs	Outputs
$@t_n$, $\overline{MR}$ = H	$@t_{n+1}$
D_n	Q_n
H	H
L	L

H = HIGH Voltage Level
L = LOW Voltage Level
t_n = Bit Time before Clock Pulse
t_{n+1} = Bit Time after Clock Pulse

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		30	45	mA	V_{CC} = Max, $D_n = \overline{MR}$ = HIGH, CP = ⨍

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$	T_A, V_{CC} = Mil $C_L = 50\ pF$	T_A, V_{CC} = Com $C_L = 50\ pF$		
		Min Typ Max	Min Max	Min Max		
f_{max}	Maximum Clock Frequency	100 140		80	MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n	3.5 5.5 8.0 4.5 7.0 10.0		3.5 9.0 4.5 11.0	ns	3-1 3-7
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	5.0 10.0 14.0		5.0 15.0	ns	3-1 3-11

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW D_n to CP	4.0 4.0		4.0 4.0	ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D_n to CP	0 0		0 0		
$t_w(H)$ $t_w(L)$	CP Pulse Width HIGH or LOW	4.0 6.0		4.0 6.0	ns	3-7
$t_w(L)$	$\overline{MR}$ Pulse Width, LOW	5.0		5.0	ns	3-11
t_{rec}	Recovery Time, $\overline{MR}$ to CP	5.0		5.0	ns	3-11

54F/74F175

Quad D Flip-Flop

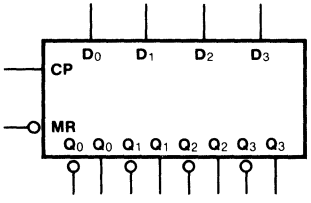
Description

The 'F175 is a high-speed quad D flip-flop. The device is useful for general flip-flop requirements where clock and clear inputs are common. The information on the D inputs is stored during the LOW-to-HIGH clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input resets all flip-flops, independent of the Clock or D inputs, when LOW.

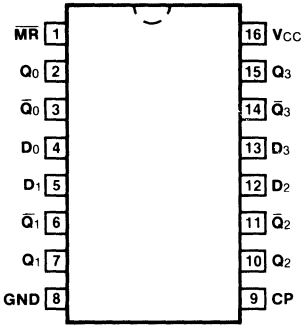
- **Edge-Triggered D-Type Inputs**
- **Buffered Positive Edge-Triggered Clock**
- **Asynchronous Common Reset**
- **True and Complement Output**

Ordering Code: See Section 5

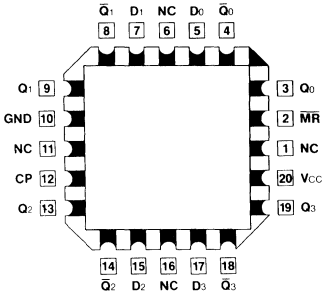
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
D_0-D_3	Data Inputs	0.5/0.375
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
$\overline{MR}$	Master Reset Input (Active LOW)	0.5/0.375
Q_0-Q_3	True Outputs	25/12.5
$\overline{Q}_0$-$\overline{Q}_3$	Complement Outputs	25/12.5

Functional Description

The 'F175 consists of four edge-triggered D flip-flops with individual D inputs and Q and $\overline{Q}$ outputs. The Clock and Master Reset are common. The four flip-flops will store the state of their individual D inputs on the LOW-to-HIGH clock (CP) transition, causing individual Q and $\overline{Q}$ outputs to follow. A LOW input on the Master Reset ($\overline{MR}$) will force all Q outputs LOW and $\overline{Q}$ outputs HIGH independent of Clock or Data inputs. The 'F175 is useful for general logic applications where a common Master Reset and Clock are acceptable.

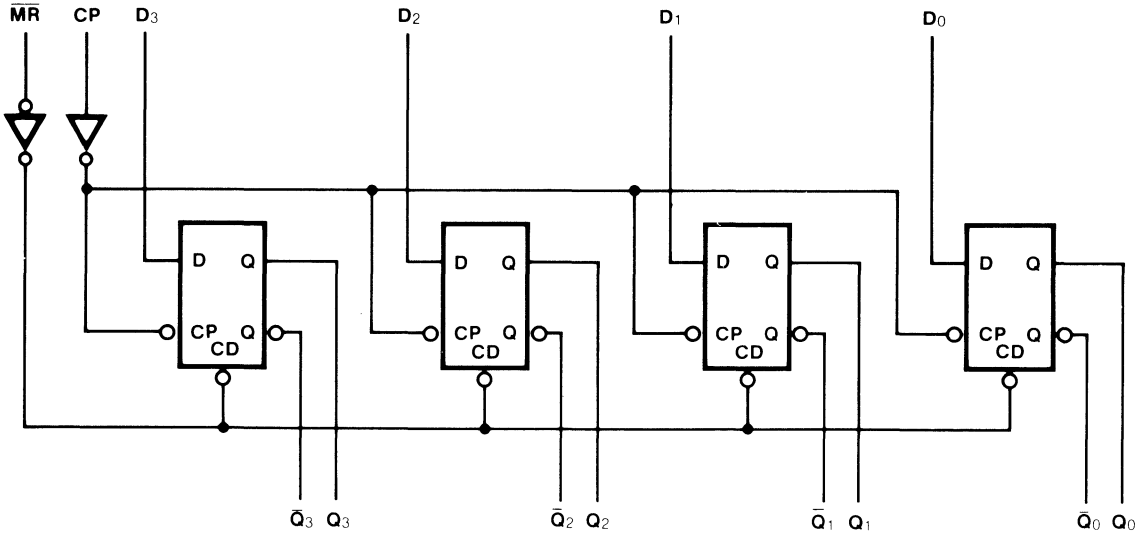
Truth Table

Inputs	Outputs	
@t_n, $\overline{MR}$ = H	@t_{n+1}	
D_n	Q_n	$\overline{Q}_n$
L	L	H
H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
t_n = Bit Time before Clock Pulse
t_{n+1} = Bit Time after Clock Pulse

4

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		22.5	34.0	mA	V_{CC} = Max D_n = $\overline{MR}$ = HIGH CP = ∫

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$, $V_{CC} = +5.0\ V$, $C_L = 50\ pF$			T_A, V_{CC} = Mil, $C_L = 50\ pF$		T_A, V_{CC} = Com, $C_L = 50\ pF$			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	100	140		100		100		MHz	3-1
t_{PHL} t_{PLH}	Propagation Delay CP to Q_n or $\overline{Q}_n$	4.0 4.0	5.0 6.5	6.5 8.5	3.5 4.0	8.5 10.5	4.0 4.0	7.5 9.5	ns	3-1 3-7
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	4.5	9.0	11.5	4.5	15.0	4.5	13.0	ns	3-1 3-11
t_{PLH}	Propagation Delay $\overline{MR}$ to $\overline{Q}_n$	4.0	6.5	8.5	4.0	10.0	4.0	9.0	ns	3-1 3-11

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$, $V_{CC} = +5.0\ V$			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW D_n to CP	3.0 3.0			3.0 3.0		3.0 3.0		ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D_n to CP	1.0 1.0			1.0 1.0		1.0 1.0			
$t_w(H)$ $t_w(L)$	CP Pulse Width HIGH or LOW	4.0 5.0			4.0 5.0		4.0 5.0		ns	3-7
$t_w(L)$	$\overline{MR}$ Pulse Width, LOW	5.0			5.0		5.0		ns	3-11
t_{rec}	Recovery Time, $\overline{MR}$ to CP	5.0			5.0		5.0		ns	3-11

54F/74F181

4-Bit Arithmetic Logic Unit

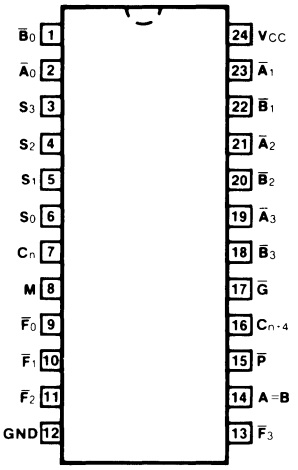
Description

The 'F181 is a 4-bit Arithmetic logic Unit (ALU) which can perform all the possible 16 logic operations on two variables and a variety of arithmetic operations. It is 40% faster than the Schottky ALU and only consumes 30% as much power.

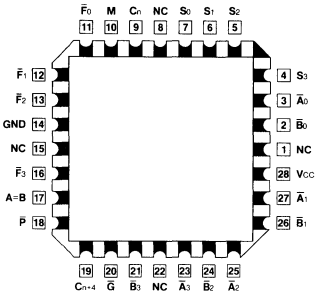
- **Full Lookahead for High-Speed Arithmetic Operation on Long Words**

Ordering Code: See Section 5

Connection Diagrams



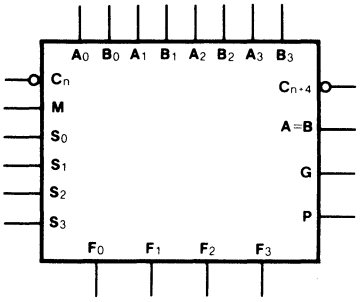
Pin Assignment for DIP and SOIC



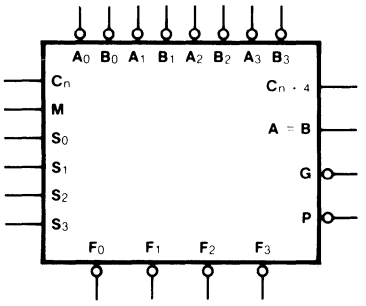
Pin Assignment for LCC and PCC

Logic Symbols

Active-HIGH Operands



Active-LOW Operands



Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
$\overline{A}_0$-$\overline{A}_3$	A Operand Inputs (Active LOW)	0.5/1.125
$\overline{B}_0$-$\overline{B}_3$	B Operand Inputs (Active LOW)	0.5/1.125
S_0-S_3	Function Select Inputs	0.5/1.50
M	Mode Control Input	0.5/0.375
C_n	Carry Input	0.5/1.875
$\overline{F}_0$-$\overline{F}_3$	Function Outputs (Active LOW)	25/12.5
A = B	Comparator Output	OC*/12.5
$\overline{G}$	Carry Generate Output (Active LOW)	25/12.5
$\overline{P}$	Carry Propagate Output (Active LOW)	25/12.5
C_{n+4}	Carry Output	25/12.5

*OC-Open Collector

Functional Description

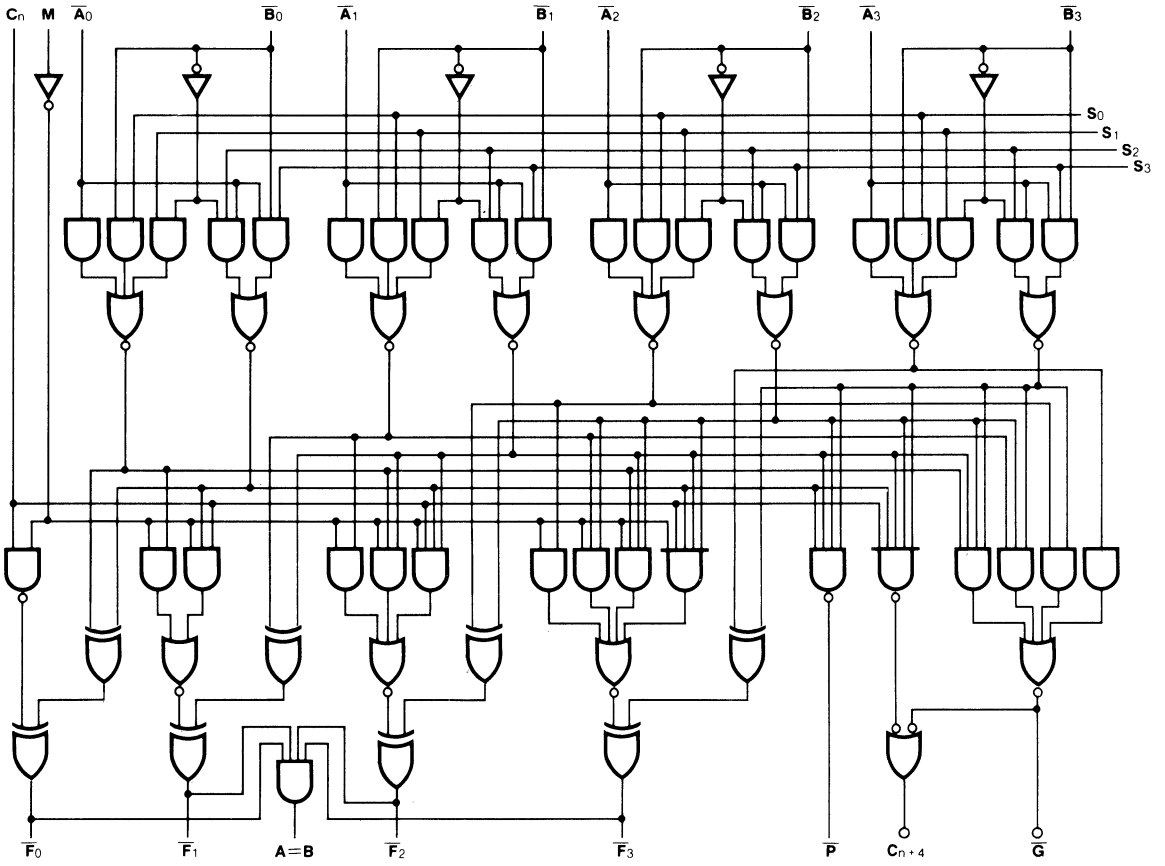
The 'F181 is a 4-bit high-speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select inputs (S_0-S_3) and the Mode Control input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on Active HIGH or Active LOW operands. The Function Table lists these operations.

When the Mode Control input (M) is HIGH, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control input is LOW, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry lookahead and provides for either ripple carry between devices using the C_{n+4} output, or for carry lookahead between packages using the signals $\overline{P}$ (Carry Propagate) and $\overline{G}$ (Carry Generate). In the Add mode, $\overline{P}$ indicates that $\overline{F}$ is 15 or more, while $\overline{G}$ indicates that $\overline{F}$ is 16 or more. In the Subtract mode $\overline{P}$ indicates that $\overline{F}$ is zero or less, while $\overline{G}$ indicates that $\overline{F}$ is less than zero. $\overline{P}$ and $\overline{G}$ are not affected by carry in. When speed requirements are not stringent, the 'F181 can be used in a simple Ripple Carry mode by connecting the Carry output (C_{n+4}) signal to the Carry input (C_n) of the next unit. For high speed operation the device is used in conjunction with a carry lookahead circuit. One carry lookahead package is required for each group of four 'F181 devices. Carry lookahead can be provided at various levels and offers high speed capability over extremely long word lengths.

The A = B output from the device goes HIGH when all four $\overline{F}$ outputs are HIGH and can be used to indicate logic equivalence over four bits when the unit is in the Subtract mode. The A = B output is open collector and can be wired AND with other A = B outputs to give a comparison for more than four bits. The A = B signal can also be used with the C_{n+4} signal to indicate A > B and A < B.

The Function Table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus, select code LHHL generates A minus B minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied. Because subtraction is actually performed by complementary addition (1s complement), a carry out means $\overline{\text{borrow}}$; thus a carry is generated when there is no underflow and no carry is generated when there is underflow. As indicated, this device can be used with either active LOW inputs producing active LOW outputs or with active HIGH inputs producing active HIGH outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Function Table

Mode Select Inputs				Active LOW Operands & F_n Outputs		Active HIGH Operands & F_n Outputs	
S_3	S_2	S_1	S_0	Logic (M = H)	Arithmetic** (M = L) (C_n = L)	Logic (M = H)	Arithmetic** (M = L) (C_n = H)
L	L	L	L	$\overline{A}$	A minus 1	$\overline{A}$	A
L	L	L	H	$\overline{AB}$	AB minus 1	$\overline{A+B}$	A + B
L	L	H	L	$\overline{A}+B$	$A\overline{B}$ minus 1	$\overline{A}B$	$A+\overline{B}$
L	L	H	H	Logic 1	minus 1	Logic 0	minus 1
L	H	L	L	$\overline{A+B}$	A plus $(A+\overline{B})$	$\overline{A}\overline{B}$	A plus $A\overline{B}$
L	H	L	H	$\overline{B}$	AB plus $(A+\overline{B})$	$\overline{B}$	$(A+B)$ plus $A\overline{B}$
L	H	H	L	$\overline{A \oplus B}$	A minus B minus 1	$A \oplus B$	A minus B minus 1
L	H	H	H	$A+\overline{B}$	$A+\overline{B}$	$A\overline{B}$	$A\overline{B}$ minus 1
H	L	L	L	$\overline{A}B$	A plus (A + B)	$\overline{A+B}$	A plus AB
H	L	L	H	$A \oplus B$	A plus B	$\overline{A \oplus B}$	A plus B
H	L	H	L	B	$A\overline{B}$ plus (A + B)	B	$(A+\overline{B})$ plus AB
H	L	H	H	A + B	A + B	AB	AB minus 1
H	H	L	L	Logic 0	A plus A*	Logic 1	A plus A*
H	H	L	H	$A\overline{B}$	AB plus A	$A+\overline{B}$	$(A+B)$ plus A
H	H	H	L	AB	$A\overline{B}$ minus A	A + B	$(A+\overline{B})$ plus A
H	H	H	H	A	A	A	A minus 1

*each bit is shifted to the next more significant position
**arithmetic operations expressed in 2s complement notation
H = HIGH Voltage Level
L = LOW Voltage Level

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{OH}	Output HIGH Current A = B			250	μA	V_{OH} = 4.5 V V_{CC} = Min
I_{CC}	Power Supply Current		43	65	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter		54F/74F $T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$			54F $T_A, V_{CC} =$ Mil $C_L = 50\ pF$		74F $T_A, V_{CC} =$ Com $C_L = 50\ pF$		Units	Fig. No.
	Path	Mode	Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay C_n to C_{n+4}		3.0 3.0	6.4 6.1	8.5 8.0			3.0 3.0	9.5 9.0	ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}$ or $\overline{B}$ to C_{n+4}	Sum	5.0 5.0	10.0 9.4	13.0 12.0			5.0 5.0	14.0 13.0	ns	3-1 3-3
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}$ or $\overline{B}$ to C_{n+4}	Dif	5.0 5.0	10.8 10.0	14.0 13.0			5.0 5.0	15.0 14.0	ns	3-1 3-3
t_{PLH} t_{PHL}	Propagation Delay C_n to $\overline{F}$	Any	3.0 3.0	6.7 6.5	8.5 8.5			3.0 3.0	9.5 9.5	ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{G}$	Sum	3.0 3.0	5.7 5.8	7.5 7.5			3.0 3.0	8.5 8.5	ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{G}$	Dif	3.0 3.0	6.5 7.3	8.5 9.5			3.0 3.0	9.5 10.5	ns	3-1 3-3
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{P}$	Sum	3.0 3.0	5.0 5.5	7.0 7.5			3.0 3.0	8.0 8.5	ns	3-1 3-3
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{P}$	Dif	4.0 4.0	5.8 6.5	7.5 8.5			4.0 4.0	8.5 9.5	ns	3-1 3-3
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$	Sum	3.0 3.0	7.0 7.2	9.0 10.0			3.0 3.0	10.0 10.0	ns	3-1, 3-3 3-4
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$	Dif	3.0 3.0	8.2 5.0	11.0 11.0			3.0 3.0	12.0 12.0	ns	3-1, 3-3 3-4
t_{PLH} t_{PHL}	Propagation Delay Any $\overline{A}$ or $\overline{B}$ to Any $\overline{F}$	Sum	4.0 4.0	8.0 7.8	10.5 10.0			4.0 4.0	11.5 11.0	ns	3-1, 3-3 3-4
t_{PLH} t_{PHL}	Propagation Delay Any $\overline{A}$ or $\overline{B}$ to Any $\overline{F}$	Dif	4.5 4.5	9.4 9.4	12.0 12.0			4.5 4.5	13.0 13.0	ns	3-1, 3-3 3-4
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{F}$	Logic	4.0 4.0	6.0 6.0	9.0 10.0			4.0 4.0	10.0 11.0	ns	3-1, 3-3 3-4
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}$ or $\overline{B}$ to A = B	Dif	11.0 7.0	18.5 9.8	27.0 12.5			11.0 7.0	29.0 13.5	ns	3-1, 3-3 3-4

54F/74F182

Carry Lookahead Generator

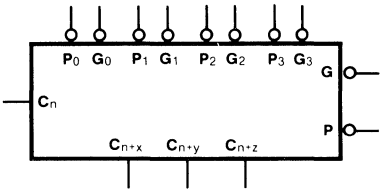
Description

The 'F182 is a high-speed carry lookahead generator. It is generally used with the 'F181, 'F381 or 29F01 4-bit arithmetic logic unit to provide high-speed lookahead over word lengths of more than four bits.

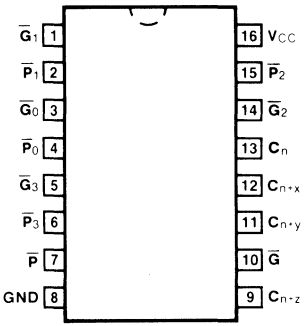
- **Provides Lookahead Carries Across a Group of Four ALUs**
- **Multi-Level Lookahead High-Speed Arithmetic Operation over Long Word Lengths**

Ordering Code: See Section 5

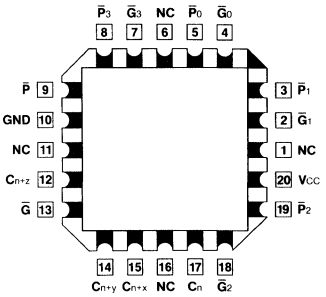
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
C_n	Carry Input	0.5/0.75
$\overline{G}_0$, $\overline{G}_2$	Carry Generate Inputs (Active LOW)	0.5/5.25
$\overline{G}_1$	Carry Generate Input (Active LOW)	0.5/6.0
$\overline{G}_3$	Carry Generate Input (Active LOW)	0.5/3.0
$\overline{P}_0$, $\overline{P}_1$	Carry Propagate Inputs (Active LOW)	0.5/3.0
$\overline{P}_2$	Carry Propagate Input (Active LOW)	0.5/2.25
$\overline{P}_3$	Carry Propagate Input (Active LOW)	0.5/1.5
C_{n+x}-C_{n+z}	Carry Outputs	25/12.5
$\overline{G}$	Carry Generate Output (Active LOW)	25/12.5
$\overline{P}$	Carry Propagate Output (Active LOW)	25/12.5

Functional Description

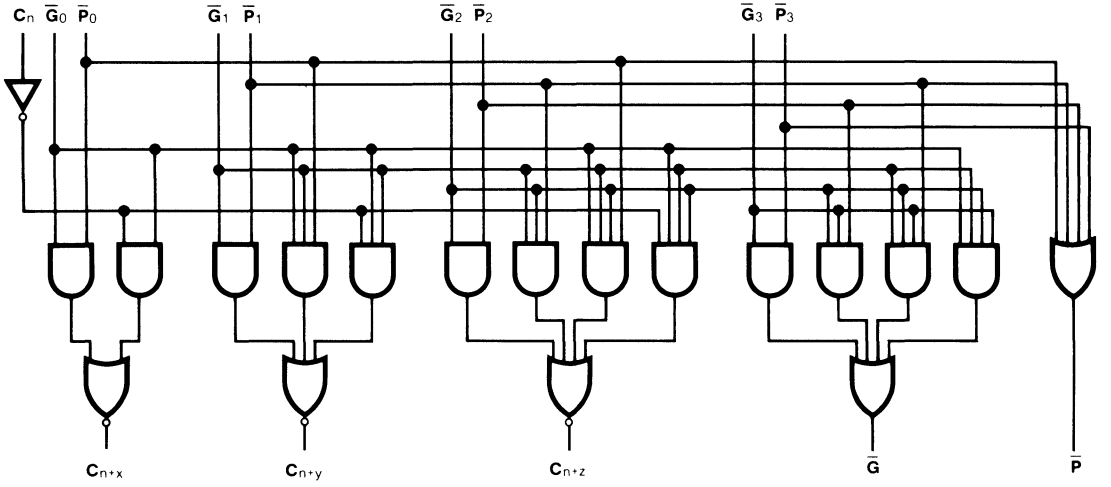
The 'F182 carry lookahead generator accepts up to four pairs of Active LOW Carry Propagate ($\overline{P}_0$-$\overline{P}_3$) and Carry Generate ($\overline{G}_0$-$\overline{G}_3$) signals and an Active HIGH Carry input (C_n) and provides anticipated Active HIGH carries (C_{n+x}, C_{n+y}, C_{n+z}) across four groups of binary adders. The 'F182 also has Active LOW Carry Propagate ($\overline{P}$) and Carry Generate ($\overline{G}$) outputs which may be used for further levels of lookahead. The logic equations provided at the outputs are:

$$C_{n+x} = G_0 + P_0C_n$$
$$C_{n+y} = G_1 + P_1G_0 + P_1P_0C_n$$
$$C_{n+z} = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$$
$$G = \overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$$
$$P = \overline{P_3P_2P_1P_0}$$

Also, the 'F182 can be used with binary ALUs in an active LOW or active HIGH input operand mode. The connections (Figure a) to and from the ALU to the carry lookahead generator are identical in both cases. Carries are rippled between lookahead blocks. The critical speed path follows the circled numbers. There are several possible arrangements for the carry interconnects, but all achieve about the same speed. A 28-bit ALU is formed by dropping the last 'F181 or 'F381.

4

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Truth Table

Inputs									Outputs				
C_n	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	C_{n+x}	C_{n+y}	C_{n+z}	$\overline{G}$	$\overline{P}$
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	X	X	H	H					L		
X	X	X	H	H	H	X					L		
X	H	H	H	X	H	X					L		
L	H	X	H	X	H	X					L		
X	X	X	X	X	L	X					H		
X	X	X	L	X	X	L					H		
X	L	X	X	L	X	L					H		
H	X	L	X	L	X	L					H		
	X		X	X	X	X	H	H				H	
	X		X	X	H	H	H	X				H	
	X		H	H	H	X	H	X				H	
	H		H	X	H	X	H	X				H	
	X		X	X	X	X	L	X				L	
	X		X	X	L	X	X	L				L	
	X		L	X	X	L	X	L				L	
	L		X	L	X	L	X	L				L	
		H		X		X		X					H
		X		H		X		X					H
		X		X		H		X					H
		X		X		X		H					H
		L		L		L		L					L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

DC Characteristics over Operating Temperature Range (unless otherwise specified)

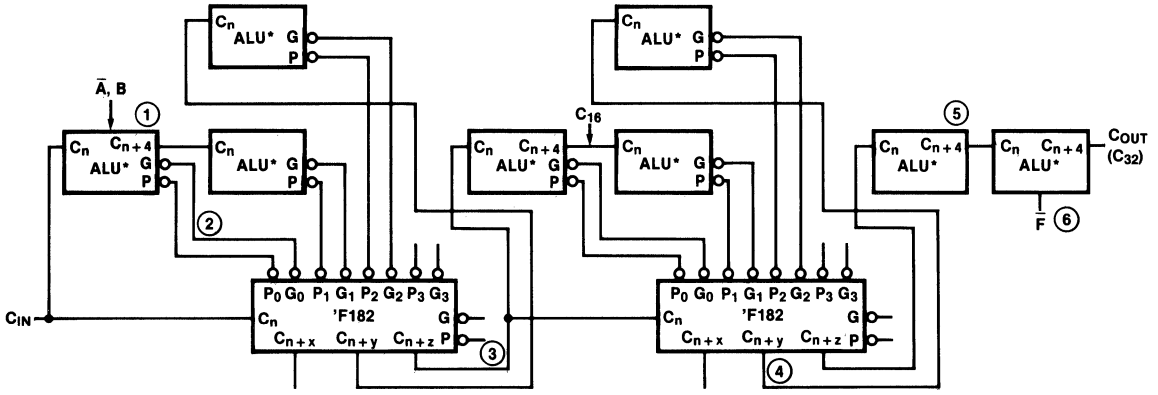
Symbol	Parameter	54F/74F			Units	Conditions	
		Min	Typ	Max			
I_{CCH}	Power Supply Current		18.4	28.0	mA	All Outputs HIGH $\overline{P}_3, \overline{G}_3 = 4.5$ V	V_{CC} = Max
I_{CCL}			23.5	36.0		All Outputs LOW $\overline{G}_0, \overline{G}_1, \overline{G}_2 =$ 4.5 V	All Other Inputs = Gnd

4

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F $T_A = +25°C$, $V_{CC} = +5.0$ V, $C_L = 50$ pF			54F T_A, V_{CC} = Mil, $C_L = 50$ pF		74F T_A, V_{CC} = Com, $C_L = 50$ pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay C_n to C_{n+x}, C_{n+y}, C_{n+z}	3.0 3.0	6.6 6.8	8.5 9.0			3.0 3.0	9.5 10.0	ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay $\overline{P}_0$, $\overline{P}_1$, or $\overline{P}_2$ to C_{n+x}, C_{n+y}, or C_{n+z}	2.5 2.0	6.2 3.7	8.0 5.0			2.5 2.0	9.0 6.0	ns	3-1 3-3
t_{PLH} t_{PHL}	Propagation Delay $\overline{G}_0$, $\overline{G}_1$, or $\overline{G}_2$ to C_{n+x}, C_{n+y}, or C_{n+z}	2.5 2.0	6.5 3.9	8.5 5.2			2.5 2.0	9.5 6.0	ns	3-1 3-3
t_{PLH} t_{PHL}	Propagation Delay $\overline{P}_1$, $\overline{P}_2$, or $\overline{P}_3$ to $\overline{G}$	3.0 3.0	7.9 6.0	10.0 8.0			3.0 3.0	11.0 9.0	ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay $\overline{G}_n$ to $\overline{G}$	3.0 3.0	8.3 5.7	10.5 7.5			3.0 3.0	11.5 8.5	ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay $\overline{P}_n$ to $\overline{P}$	3.0 2.5	5.7 4.1	7.5 5.5			3.0 2.5	8.5 6.5	ns	3-1 3-4

Fig. a 32-Bit ALU with Ripple Carry between 16-Bit Lookahead ALUs



ALUs may be either 'F181, 'F381 or 29F01

54F/74F189

64-Bit Random Access Memory With 3-State Outputs

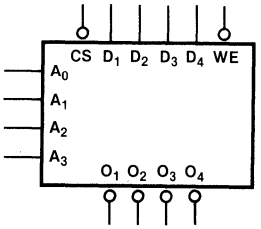
Description

The 'F189 is a high-speed 64-bit RAM organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading and are fully decoded on-chip. The outputs are 3-state and are in the high impedance state whenever the Chip Select ($\overline{CS}$) input is HIGH. The outputs are active only in the Read mode and the output data is the complement of the stored data.

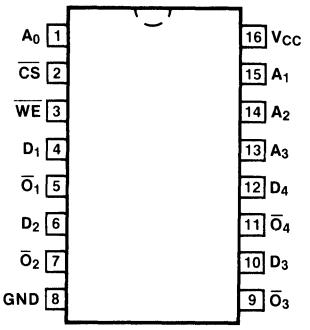
- **3-State Outputs for Data Bus Applications**
- **Buffered Inputs Minimize Loading**
- **Address Decoding On-Chip**
- **Diode Clamped Inputs Minimize Ringing**

Ordering Code: See Section 5

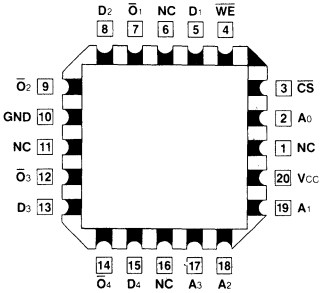
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

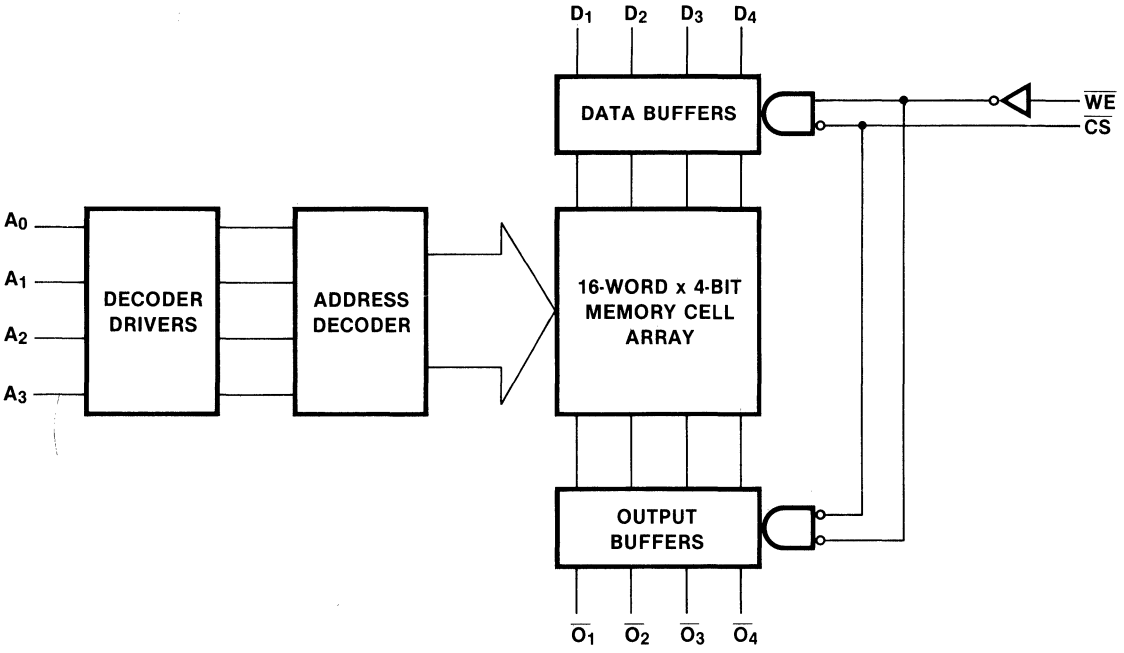
Pin Names	Description	54F/74F(U.L.) HIGH/LOW
A_0-A_3	Address Inputs	0.5/0.375
$\overline{CS}$	Chip Select Input (Active LOW)	0.5/0.75
$\overline{WE}$	Write Enable Input (Active LOW)	0.5/0.375
D_1-D_4	Data Inputs	0.5/0.375
$\overline{O}_1$-$\overline{O}_4$	Inverted Data Outputs	25/12.5

Function Table

Inputs		Operation	Condition of Outputs
$\overline{CS}$	$\overline{WE}$		
L	L	Write	High Impedance
L	H	Read	Complement of Stored Data
H	X	Inhibit	High Impedance

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Block Diagram



DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		37	55	mA	V_{CC} = Max; $\overline{WE}$, $\overline{CS}$ = Gnd

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$			T_A, V_{CC} = Mil $C_L = 50\ pF$		T_A, V_{CC} = Com $C_L = 50\ pF$			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Access Time, HIGH or LOW	11.0	18.5	26.0	9.0	32.0	11.0	27.0	ns	3-1
t_{PHL}	A_n to $\overline{O}_n$	8.0	13.5	19.0	8.0	23.0	8.0	20.0		3-10
t_{PZH}	Access Time, HIGH or LOW	3.5	6.0	8.5	3.5	10.5	3.5	9.5	ns	3-1, 3-12
t_{PZL}	$\overline{CS}$ to $\overline{O}_n$	5.0	9.0	13.0	5.0	15.0	5.0	14.0		3-13
t_{PHZ}	Disable Time, HIGH or LOW	2.0	4.0	6.0	2.0	8.0	2.0	7.0	ns	3-1, 3-12
t_{PLZ}	$\overline{CS}$ to $\overline{O}_n$	3.0	5.5	8.0	2.5	10.0	3.0	9.0		3-13
t_{PZH}	Write Recovery Time,	6.5	20.0	28.0	6.5	37.5	6.5	29.0	ns	3-1, 3-12
t_{PZL}	HIGH or LOW $\overline{WE}$ to $\overline{O}_n$	6.5	11.0	15.5	6.5	17.5	6.5	16.5		3-13
t_{PHZ}	Disable Time, HIGH or LOW	4.0	7.0	10.0	3.5	12.0	4.0	11.0	ns	3-1, 3-12
t_{PLZ}	$\overline{WE}$ to $\overline{O}_n$	5.0	9.0	13.0	5.0	15.0	5.0	14.0		3-13

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
$t_s(H)$	Setup Time, HIGH or LOW	0			0		0		ns	3-16
$t_s(L)$	A_n to $\overline{WE}E$	0			0		0			
$t_h(H)$	Hold Time, HIGH or LOW	2.0			2.0		2.0			
$t_h(L)$	A_n to $\overline{WE}$	2.0			2.0		2.0			
$t_s(H)$	Setup Time, HIGH or LOW	10.0			11.0		10.0		ns	3-14
$t_s(L)$	D_n to $\overline{WE}$	10.0			11.0		10.0			
$t_h(H)$	Hold Time, HIGH or LOW	0			2.0		0			
$t_h(L)$	D_n to $\overline{WE}$	0			2.0		0			
$t_s(L)$	Setup Time, LOW $\overline{CS}$ to$\overline{WE}$	0			0		0		ns	3-14
$t_h(L)$	Hold Time, LOW $\overline{CS}$ to $\overline{WE}$	6.0			7.5		6.0			
$t_w(L)$	$\overline{WE}$ Pulse Width, LOW	6.0			7.5		6.0		ns	3-16

54F/74F190

Up/Down Decade Counter With Preset and Ripple Clock

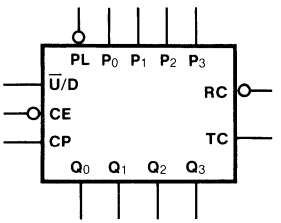
Description

The 'F190 is a reversible BCD (8421) decade counter featuring synchronous counting and asynchronous presetting. The preset feature allows the 'F190 to be used in programmable dividers. The Count Enable input, the Terminal Count output and the Ripple Clock output make possible a variety of methods of implementing multistage counters. In the counting modes, state changes are initiated by the rising edge of the clock.

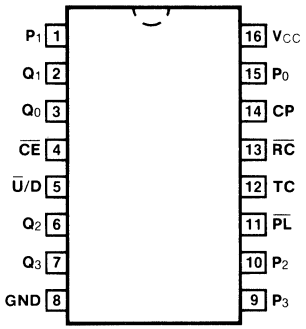
- **High-speed—125 MHz Typical Count Frequency**
- **Synchronous Counting**
- **Asynchronous Parallel Load**
- **Cascadable**

Ordering Code: See Section 5

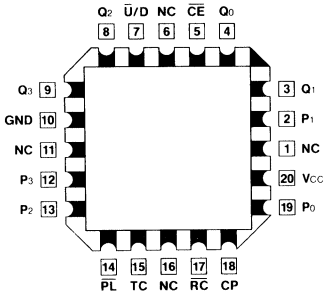
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
$\overline{CE}$	Count Enable Input (Active LOW)	0.5/1.125
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
P_0-P_3	Parallel Data Inputs	0.5/0.375
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)	0.5/0.375
$\overline{U}$/D	Up/Down Count Control Input	0.5/0.375
Q_0-Q_3	Flip-Flop Outputs	25/12.5
$\overline{RC}$	Ripple Clock Output (Active LOW)	25/12.5
TC	Terminal Count Output (Active HIGH)	25/12.5

Functional Description

The 'F190 is a synchronous up/down BCD decade counter containing four edge-triggered flip-flops, with internal gating and steering logic to provide individual preset, count-up and count-down operations. It has an asynchronous parallel load capability permitting the counter to be preset to any desired number. When the Parallel Load ($\overline{PL}$) input is LOW, information present on the Parallel Data inputs (P_0-P_3) is loaded into the counter and appears on the Q outputs. This operation overrides the counting functions, as indicated in the Mode Select Table. A HIGH signal on the $\overline{CE}$ input inhibits counting. When $\overline{CE}$ is LOW, internal state changes are initiated synchronously by the LOW-to-HIGH transition of the clock input. The direction of counting is determined by the $\overline{U}$/D input signal, as indicated in the Mode Select Table, $\overline{CE}$ and $\overline{U}$/D can be changed with the clock in either state, provided only that the recommended setup and hold times are observed.

Two types of outputs are provided as overflow/underflow indicators. The Terminal Count (TC) output is normally LOW and goes HIGH when a circuit reaches zero in the count-down mode or reaches 9 in the count-up mode. The TC output will then remain HIGH until a state change occurs, whether by counting or presetting or until $\overline{U}$/D is changed. The TC output should not be used as a clock signal because it is subject to decoding spikes. The TC signal is also used internally to enable the Ripple Clock ($\overline{RC}$) output. The $\overline{RC}$ output is normally HIGH. When $\overline{CE}$ is LOW and TC is HIGH, the $\overline{RC}$ output will go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again. This feature simplifies the design of multistage counters. For a discussion and illustrations of the various methods of implementing multistage counters, please see the 'F191 data sheet.

4

$\overline{RC}$ Truth Table

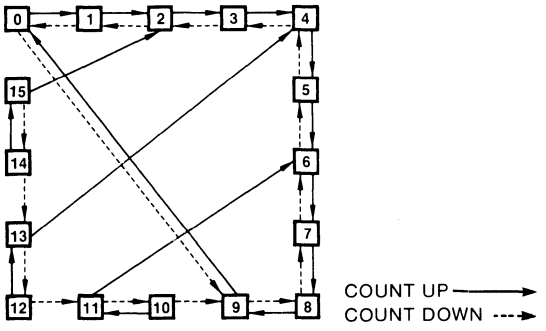
Inputs			Output
$\overline{CE}$	TC*	CP	$\overline{RC}$
L	H	⊓	⊓
H	X	X	H
X	L	X	H

*TC is generated internally
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

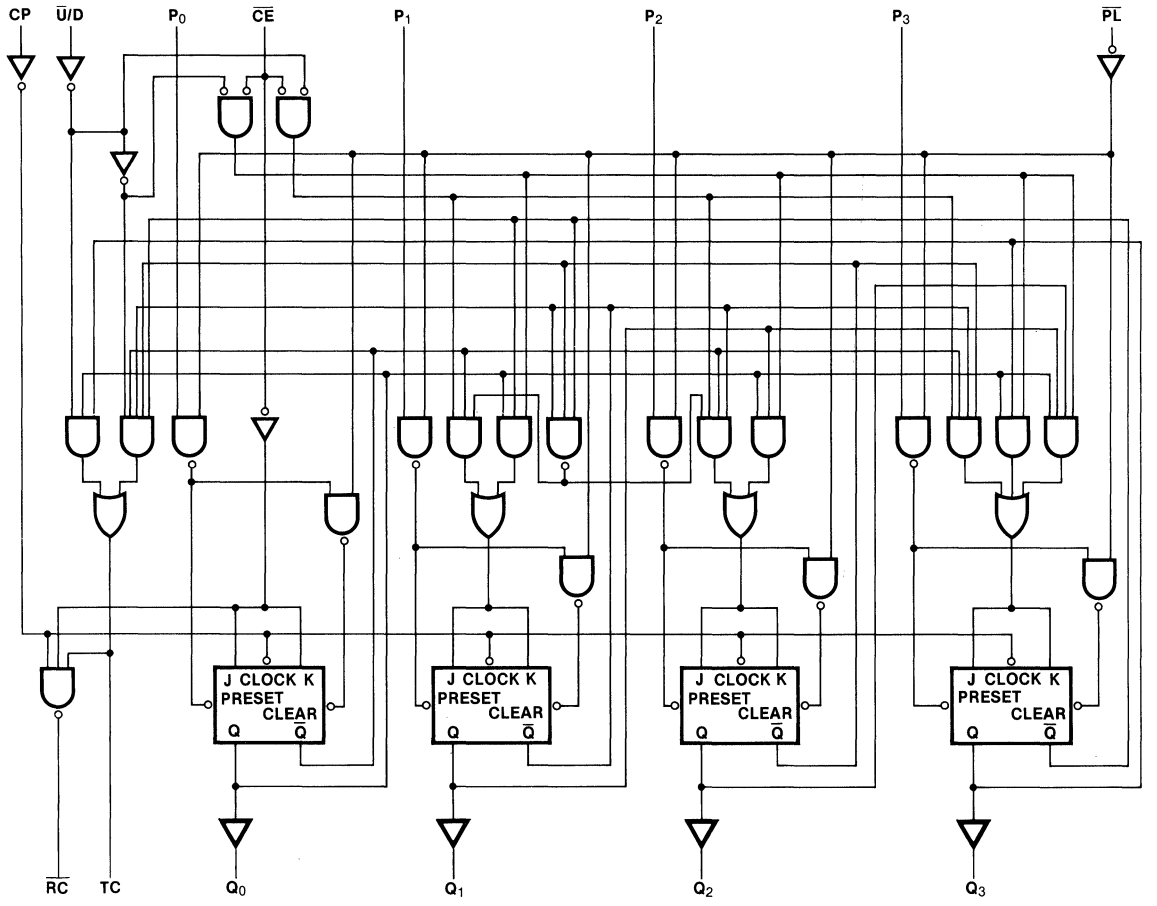
Mode Select Table

Inputs				Mode
$\overline{PL}$	$\overline{CE}$	$\overline{U}$/D	CP	
H	L	L	∫	Count Up
H	L	H	∫	Count Down
L	X	X	X	Preset (Asyn.)
H	H	X	X	No Change (Hold)

State Diagram



Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		38	55	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$			$T_A, V_{CC} =$ Mil $C_L = 50\ pF$		$T_A, V_{CC} =$ Com $C_L = 50\ pF$			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Count Frequency	100	125		75		90		MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n	3.0 5.0	5.5 8.5	7.5 11.0	1.5 3.5	12.0 16.0	3.0 5.0	8.5 12.0	ns	3-1, 3-7
t_{PLH} t_{PHL}	Propagation Delay CP to TC	6.0 5.0	10.0 8.5	13.0 11.0	5.0 4.5	20.0 16.0	6.0 5.0	14.0 12.0		
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{RC}$	3.0 3.0	5.5 5.0	7.5 7.0	1.5 1.5	11.5 12.5	3.0 3.0	8.5 8.0	ns	3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay $\overline{CE}$ to $\overline{RC}$	3.0 3.0	5.0 5.5	7.0 7.0	3.0 3.0	8.5 8.5	3.0 3.0	8.0 8.0		
t_{PLH} t_{PHL}	Propagation Delay $\overline{U}/D$ to $\overline{RC}$	7.0 5.5	11.0 9.0	18.0 12.0	7.0 5.5	22.5 13.5	7.0 5.5	20.0 13.0	ns	3-1, 3-2
t_{PLH} t_{PHL}	Propagation Delay $\overline{U}/D$ to TC	4.0 4.0	7.0 6.5	10.0 10.0	4.0 4.0	13.0 12.0	4.0 4.0	11.0 11.0		
t_{PLH} t_{PHL}	Propagation Delay P_n to Q_n	3.0 6.0	4.5 10.0	7.0 13.0	1.5 6.0	11.0 16.0	3.0 6.0	8.0 14.0	ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to Q_n	5.0 5.5	8.5 9.0	11.0 12.0	5.0 5.5	13.0 14.0	5.0 5.5	12.0 13.0	ns	3-1 3-11

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\,V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW P_n to $\overline{PL}$	4.5 4.5	6.0 6.0	5.0 5.0	ns	3-14
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW P_n to $\overline{PL}$	2.0 2.0	2.0 2.0	2.0 2.0		
$t_s(L)$	Setup Time, LOW $\overline{CE}$ to CP	10.0	10.5	10.0	ns	3-5
$t_h(L)$	Hold Time, LOW $\overline{CE}$ to CP	0	0	0		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{U}/D$ to CP	12.0 12.0	12.0 12.0	12.0 12.0	ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{U}/D$ to CP	0 0	0 0	0 0		
$t_w(L)$	$\overline{PL}$ Pulse Width, LOW	6.0	8.5	6.0	ns	3-11
$t_w(L)$	CP Pulse Width, LOW	5.0	7.0	5.0	ns	3-7
t_{rec}	Recovery Time $\overline{PL}$ to CP	6.0	7.5	6.0	ns	3-11

54F/74F191

Up/Down Binary Counter With Preset and Ripple Clock

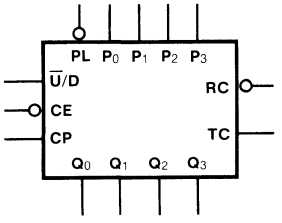
Description

The 'F191 is a reversible modulo-16 binary counter featuring synchronous counting and asynchronous presetting. The preset feature allows the 'F191 to be used in programmable dividers. The Count Enable input, the Terminal Count output and the Ripple Clock output make possible a variety of methods of implementing multistage counters. In the counting modes, state changes are initiated by the rising edge of the clock.

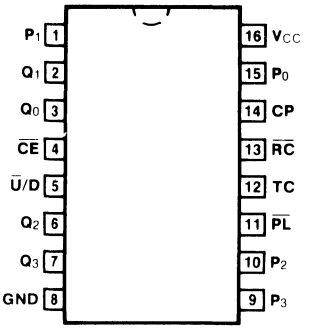
- **High-Speed—125 MHz Typical Count Frequency**
- **Synchronous Counting**
- **Asynchronous Parallel Load**
- **Cascadable**

Ordering Code: See Section 5

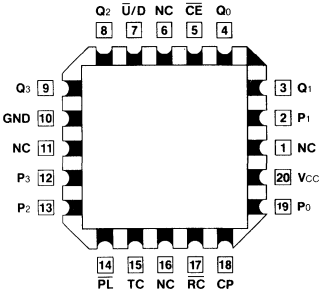
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
$\overline{CE}$	Count Enable Input (Active LOW)	0.5/1.125
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
P_0-P_3	Parallel Data Inputs	0.5/0.375
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)	0.5/0.375
$\overline{U}$/D	Up/Down Count Control Input	0.5/0.375
Q_0-Q_3	Flip-Flop Outputs	25/12.5
$\overline{RC}$	Ripple Clock Output (Active LOW)	25/12.5
TC	Terminal Count Output (Active HIGH)	25/12.5

Functional Description

The 'F191 is a synchronous up/down 4-bit binary counter. It contains four edge-triggered flip-flops, with internal gating and steering logic to provide individual preset, count-up and count-down operations.

Each circuit has an asynchronous parallel load capability permitting the counter to be preset to any desired number. When the Parallel Load ($\overline{PL}$) input is LOW, information present on the Parallel Data inputs (P_0-P_3) is loaded into the counter and appears on the Q outputs. This operation overrides the counting functions, as indicated in the Mode Select Table.

A HIGH signal on the $\overline{CE}$ input inhibits counting. When $\overline{CE}$ is LOW, internal state changes are initiated synchronously by the LOW-to-HIGH transition of the clock input. The direction of counting is determined by the $\overline{U}$/D input signal, as indicated in the Mode Select Table. $\overline{CE}$ and $\overline{U}$/D can be changed with the clock in either state, provided only that the recommended setup and hold times are observed.

Two types of outputs are provided as overflow/underflow indicators. The Terminal Count (TC) output is normally LOW and goes HIGH when a circuit reaches zero in the count-down mode or reaches 15 in the count-up mode. The TC output will then remain HIGH until a state change occurs, whether by counting or presetting or until $\overline{U}$/D is changed. The TC output should not be used as a clock signal because it is subject to decoding spikes.

The TC signal is also used internally to enable the Ripple Clock ($\overline{RC}$) output. The $\overline{RC}$ output is normally HIGH. When $\overline{CE}$ is LOW and TC is HIGH, the $\overline{RC}$ output will go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again. This feature simplifies the design of multistage counters, as indicated in Figures a and b. In Figure a, each $\overline{RC}$ output is used as the clock input for the next higher stage. This configuration is particularly advantageous when the clock source has a limited drive capability, since it drives only the first stage. To prevent counting in all stages it is only necessary to inhibit the first stage, since a HIGH signal on $\overline{CE}$ inhibits the $\overline{RC}$ output pulse, as indicated in the $\overline{RC}$ Truth Table. A disadvantage of this configuration, in some applications, is the timing skew between state changes in the first and last stages. This represents the cumulative delay of the clock as it ripples through the preceding stages.

A method of causing state changes to occur simultaneously in all stages is shown in Figure b. All clock inputs are driven in parallel and the $\overline{RC}$ outputs propagate the carry/borrow signals in ripple fashion. In this configuration the LOW state duration of the clock must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes HIGH. There is no such restriction on the HIGH state duration of the clock, since the $\overline{RC}$ output of any device goes HIGH shortly after its CP input goes HIGH.

The configuration shown in Figure c avoids ripple delays and their associated restrictions. The $\overline{CE}$ input for a given stage is formed by combining the TC signals from all the preceding stages. Note that in order to inhibit counting an enable signal must be included in each carry gate. The simple inhibit scheme of Figures a and b doesn't apply, because the TC output of a given stage is not affected by its own $\overline{CE}$.

Mode Select Table

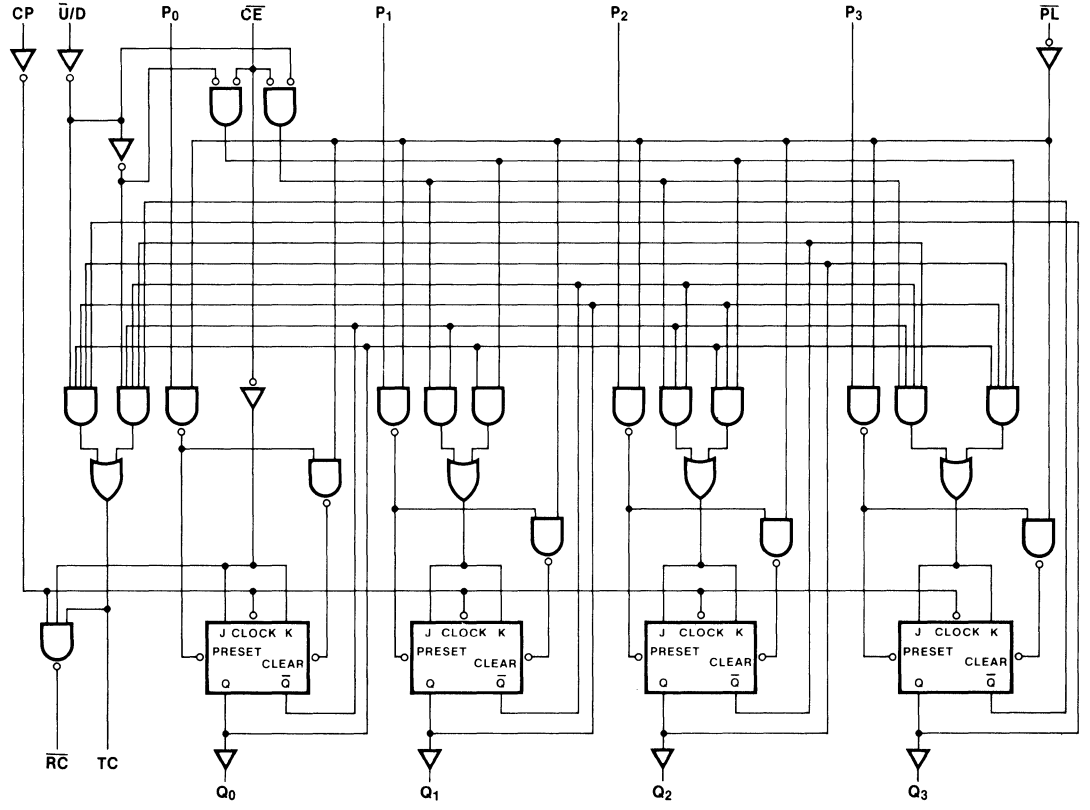
Inputs				Mode
$\overline{PL}$	$\overline{CE}$	$\overline{U}$/D	CP	
H	L	L	⌐	Count Up
H	L	H	⌐	Count Down
L	X	X	X	Preset (Asyn.)
H	H	X	X	No Change (Hold)

$\overline{RC}$ Truth Table

Inputs			Output
$\overline{CE}$	TC*	CP	$\overline{RC}$
L	H	⌐⌐	⌐⌐
H	X	X	H
X	L	X	H

*TC is generated internally
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Fig. a n-Stage Counter Using Ripple Clock

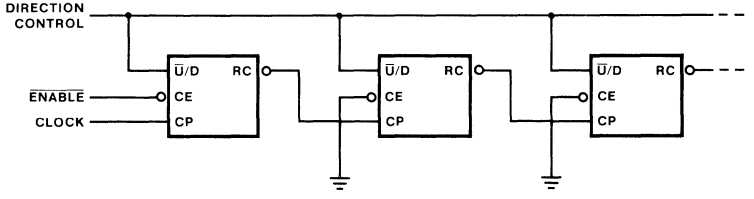


Fig. b Synchronous n-Stage Counter Using Ripple Carry/Borrow

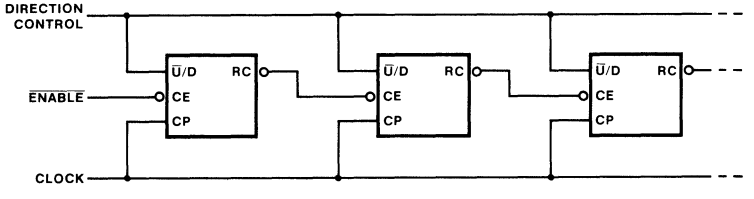
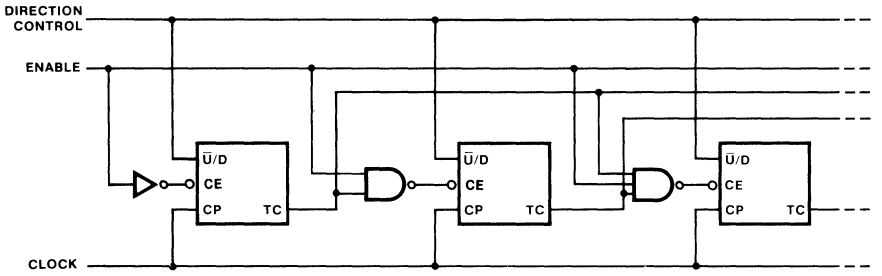


Fig. c Synchronous n-Stage Counter with Parallel Gated Carry/Borrow



DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		38	55	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			54F T_A, V_{CC} = Mil C_L = 50 pF		74F T_A, V_{CC} = Com C_L = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Count Frequency	100	125		75		90		MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n	3.0 5.0	5.5 8.5	7.5 11.0	1.5 3.5	12.0 16.0	3.0 5.0	8.5 12.0	ns	3-1, 3-7
t_{PLH} t_{PHL}	Propagation Delay CP to TC	6.0 5.0	10.0 8.5	13.0 11.0	5.0 4.5	20.0 16.0	6.0 5.0	14.0 12.0		
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{RC}$	3.0 3.0	5.5 5.0	7.5 7.0	1.5 1.5	11.5 12.5	3.0 3.0	8.5 8.0	ns	3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay $\overline{CE}$ to $\overline{RC}$	3.0 3.0	5.0 5.5	7.0 7.0	3.0 3.0	8.5 8.5	3.0 3.0	8.0 8.0		
t_{PLH} t_{PHL}	Propagation Delay $\overline{U}$/D to $\overline{RC}$	7.0 5.5	11.0 9.0	18.0 12.0	7.0 5.5	22.5 13.5	7.0 5.5	20.0 13.0	ns	3-1, 3-2
t_{PLH} t_{PHL}	Propagation Delay $\overline{U}$/D to TC	4.0 4.0	7.0 6.5	10.0 10.0	4.0 4.0	13.0 12.0	4.0 4.0	11.0 11.0		
t_{PLH} t_{PHL}	Propagation Delay P_n to Q_n	3.0 6.0	4.5 10.0	7.0 13.0	1.5 6.0	11.0 16.0	3.0 6.0	8.0 14.0	ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to Q_n	5.0 5.5	8.5 9.0	11.0 12.0	5.0 5.5	13.0 14.0	5.0 5.5	12.0 13.0	ns	3-1 3-11

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW P_n to $\overline{PL}$	4.5 4.5	6.0 6.0	5.0 5.0	ns	3-14
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW P_n to $\overline{PL}$	2.0 2.0	2.0 2.0	2.0 2.0		
$t_s(L)$	Setup Time LOW $\overline{CE}$ to CP	10.0	10.5	10.0	ns	3-5
$t_h(L)$	Hold Time LOW $\overline{CE}$ to CP	0	0	0		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{U}$/D to CP	12.0 12.0	12.0 12.0	12.0 12.0	ns	3.5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{U}$/D to CP	0 0	0 0	0 0		
$t_w(L)$	$\overline{PL}$ Pulse Width LOW	6.0	8.5	6.0	ns	3-11
$t_w(L)$	CP Pulse Width LOW	5.0	7.0	5.0	ns	3-7
t_{rec}	Recovery Time $\overline{PL}$ to CP	6.0	7.5	6.0	ns	3-11

54F/74F192

Up/Down Decade Counter With Separate Up/Down Clocks

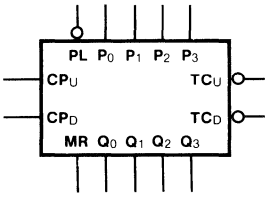
Description

The 'F192 is an up/down BCD decade (8421) counter. Separate Count Up and Count Down Clocks are used, and in either counting mode the circuits operate synchronously. The outputs change state synchronously with the LOW-to-HIGH transitions on the clock inputs.

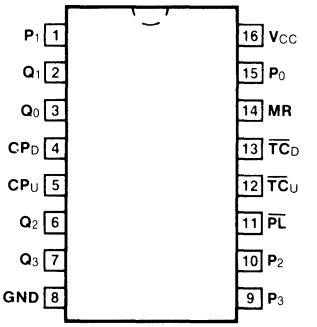
Separate Terminal Count Up and Terminal Count Down outputs are used as the clocks for a subsequent stage without extra logic, thus simplifying multistage counter designs. Individual preset inputs allow the circuit to be used as a programmable counter. Both the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs asynchronously override the clocks.

Ordering Code: See Section 5

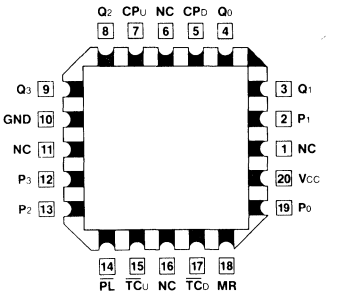
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
CP_U	Count Up Clock Input (Active Rising Edge)	0.5/1.125
CP_D	Count Down Clock Input (Active Rising Edge)	0.5/1.125
MR	Asynchronous Master Reset Input (Active HIGH)	0.5/0.375
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)	0.5/0.375
P_0-P_3	Parallel Data Inputs	0.5/0.375
Q_0-Q_3	Flip-Flop Outputs	25/12.5
$\overline{TC}_D$	Terminal Count Down (Borrow) Output (Active LOW)	25/12.5
$\overline{TC}_U$	Terminal Count Up (Carry) Output (Active LOW)	25/12.5

Functional Description

The 'F192 is an asynchronously presettable decade counter. It contains four edge-triggered flip-flops, with internal gating and steering logic to provide master reset, individual preset, count up and count down operations.

A LOW-to-HIGH transition on the CP input to each flip-flop causes the output to change state. Synchronous switching, as opposed to ripple counting, is achieved by driving the steering gates of all stages from a common Count Up line and a common Count Down line, thereby causing all state changes to be initiated simultaneously. A LOW-to-HIGH transition on the Count Up input will advance the count by one; a similar transition on the Count Down input will decrease the count by one. While counting with one clock input, the other should be held HIGH, as indicated in the Function Table. Otherwise, the circuit will either count by twos or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either clock input is LOW.

The Terminal Count Up ($\overline{TC}_U$) and Terminal Count Down ($\overline{TC}_D$) outputs are normally HIGH. When the circuit has reached the maximum count state 9, the next HIGH-to-LOW transition of the Count Up Clock will cause $\overline{TC}_U$ to go LOW. $\overline{TC}_U$ will stay LOW until CP_U goes HIGH again, thus effectively repeating the Count Up Clock, but delayed by two gate delays. Similarly, the $\overline{TC}_D$ output will go LOW when the circuit is in the zero state and the Count Down Clock goes LOW. Since the $\overline{TC}$ outputs repeat the clock waveforms, they can be used as the clock input signals to the next higher order circuit in a multistage counter.

$$\overline{TC}_U = Q_0 \bullet Q_3 \bullet \overline{CP}_U$$
$$\overline{TC}_D = \overline{Q}_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet \overline{Q}_3 \bullet \overline{CP}_D$$

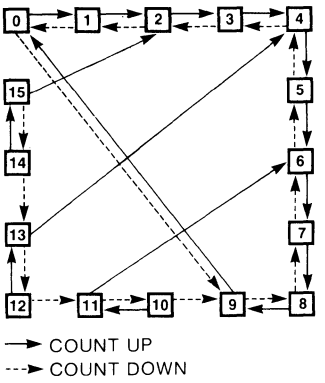
The 'F192 has an asynchronous parallel load capability permitting the counter to be preset. When the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs are LOW, information present on the Parallel Data input (P_0-P_3) is loaded into the counter and appears on the outputs regardless of the conditions of the clock inputs. A HIGH signal on the Master Reset input will disable the preset gates, override both clock inputs, and latch each Q output in the LOW state. If one of the clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that clock will be interpreted as a legitimate signal and will be counted.

Function Table

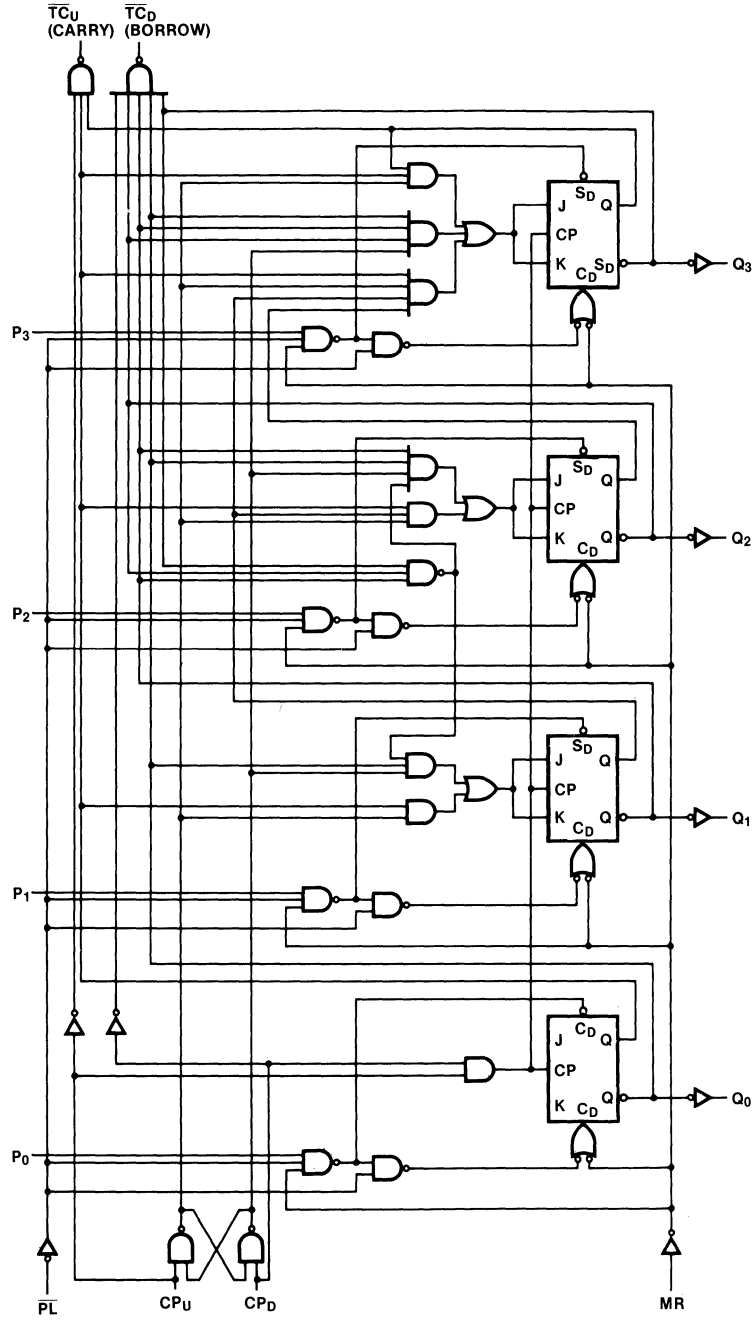
MR	$\overline{PL}$	CP_U	CP_D	Mode
H	X	X	X	Reset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	⎍	H	Count Up
L	H	H	⎍	Count Down

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

State Diagram



Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		38	55	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Count Frequency	100	125		75		90		MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay CP_U or CP_D to $\overline{TC}_U$ or $\overline{TC}_D$	4.0 3.5	7.0 6.0	9.0 8.0	4.0 3.5	10.5 9.5	4.0 3.5	10.0 9.0	ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay CP_U or CP_D to Q_n	4.0 5.5	6.5 9.5	8.5 12.5	4.0 5.5	10.0 14.0	4.0 5.5	9.5 13.5	ns	3-1 3-7
t_{PLH} t_{PHL}	Propagation Delay P_n to Q_n	3.0 6.0	4.5 11.0	7.0 14.5	3.0 6.0	8.5 16.5	3.0 6.0	8.0 15.5	ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to Q_n	5.0 5.5	8.5 10.0	11.0 13.0	5.0 5.5	13.5 15.0	5.0 5.5	12.0 14.0	ns	3-1 3-10
t_{PHL}	Propagation Delay MR to Q_n	6.5	11.0	14.5	6.5	16.0	6.5	15.5	ns	3-1 3-11
t_{PLH}	Propagation Delay MR to $\overline{TC}_U$	6.0	10.5	13.5	6.0	15.0	6.0	14.5		
t_{PHL}	Propagation Delay MR to $\overline{TC}_D$	7.0	11.5	14.5	7.0	16.0	7.0	15.5		
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to $\overline{TC}_U$ or $\overline{TC}_D$	7.0 7.0	12.0 11.5	15.5 14.5	7.0 7.0	18.5 17.5	7.0 7.0	16.5 15.5	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay P_n to $\overline{TC}_U$ or $\overline{TC}_D$	7.0 6.5	11.5 11.0	14.5 14.0	7.0 6.5	16.5 16.5	7.0 6.5	15.5 15.0	ns	3-1 3-10

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\,V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW P_n to $\overline{PL}$	4.5 4.5	6.0 6.0	5.0 5.0	ns	3-14
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW P_n to $\overline{PL}$	2.0 2.0	2.0 2.0	2.0 2.0		
$t_w(L)$	$\overline{PL}$ Pulse Width, LOW	6.0	7.5	6.0	ns	3-11
$t_w(L)$	CP_U or CP_D Pulse Width, LOW	5.0	7.0	5.0	ns	3-7
$t_w(L)$	CP_U or CP_D Pulse Width, LOW (Change of Direction)	10.0	12.0	10.0	ns	3-7
$t_w(H)$	MR Pulse Width, HIGH	6.0	6.0	6.0	ns	3-11
t_{rec}	Recovery Time $\overline{PL}$ to CP_U or CP_D	6.0	8.0	6.0	ns	3-11
t_{rec}	Recovery Time MR to CP_U or CP_D	4.0	4.5	4.0	ns	3-11

54F/74F193

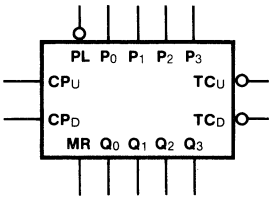
Up/Down Binary Counter
With Separate Up/Down Clocks

Description

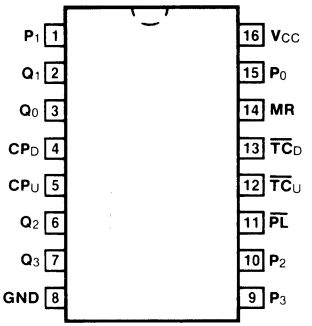
The 'F193 is an up/down modulo-16 binary counter. Separate Count Up and Count Down Clocks are used, and in either counting mode the circuits operate synchronously. The outputs change state synchronously with the LOW-to-HIGH transitions on the clock inputs. Separate Terminal Count Up and Terminal Count Down outputs are provided that are used as the clocks for subsequent stages without extra logic, thus simplifying multistage counter designs. Individual preset inputs allow the circuit to be used as a programmable counter. Both the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs asynchronously override the clocks.

Ordering Code: See Section 5

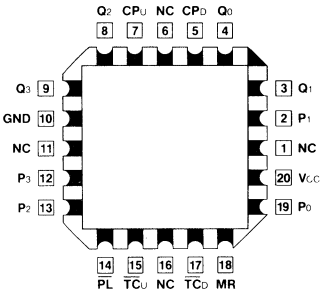
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
CP_U	Count Up Clock Input (Active Rising Edge)	0.5/1.125
CP_D	Count Down Clock Input (Active Rising Edge)	0.5/1.125
MR	Asynchronous Master Reset Input (Active HIGH)	0.5/0.375
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)	0.5/0.375
P_0-P_3	Parallel Data Inputs	0.5/0.375
Q_0-Q_3	Flip-Flop Outputs	25/12.5
$\overline{TC}_D$	Terminal Count Down (Borrow) Output (Active LOW)	25/12.5
$\overline{TC}_U$	Terminal Count Up (Carry) Output (Active LOW)	25/12.5

Functional Description

The 'F193 is a 4-bit binary synchronous up/down (reversible) counter. It contains four edge-triggered flip-flops, with internal gating and steering logic to provide master reset, individual preset, count up and count down operations.

A LOW-to-HIGH transition on the CP input to each flip-flop causes the output to change state. Synchronous switching, as opposed to ripple counting, is achieved by driving the steering gates of all stages from a common Count Up line and a common Count Down line, thereby causing all state changes to be initiated simultaneously. A LOW-to-HIGH transition on the Count Up input will advance the count by one; a similar transition on the Count Down input will decrease the count by one. While counting with one clock input, the other should be held HIGH, as indicated in the Function Table. Otherwise, the circuit will either count by twos or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either clock input is LOW.

The Terminal Count Up ($\overline{TC}_U$) and Terminal Count Down ($\overline{TC}_D$) outputs are normally HIGH. When the circuit has reached the maximum count state 15, the next HIGH-to-LOW transition of the Count Up Clock will cause $\overline{TC}_U$ to go LOW. $\overline{TC}_U$ will stay LOW until CP_U goes HIGH again, thus effectively repeating the Count Up Clock, but delayed by two gate delays. Similarly, the $\overline{TC}_D$ output will go LOW when the circuit is in the zero state and the Count Down Clock goes LOW. Since the $\overline{TC}$ outputs repeat the clock waveforms, they can be used as the clock input signals to the next higher order circuit in a multistage counter.

$$\overline{TC}_U = Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3 \bullet \overline{CP}_U$$
$$\overline{TC}_D = \overline{Q}_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet \overline{Q}_3 \bullet \overline{CP}_D$$

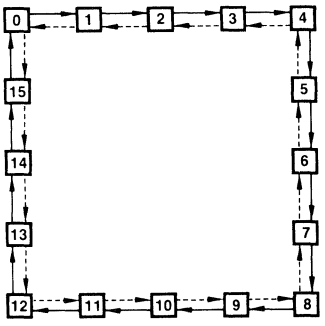
The 'F193 has an asynchronous parallel load capability permitting the counter to be preset. When the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs are LOW, information present on the Parallel Data input (P_0-P_3) is loaded into the counter and appears on the outputs regardless of the conditions of the clock inputs. A HIGH signal on the Master Reset input will disable the preset gates, override both clock inputs, and latch each Q output in the LOW state. If one of the clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that clock will be interpreted as a legitimate signal and will be counted.

Function Table

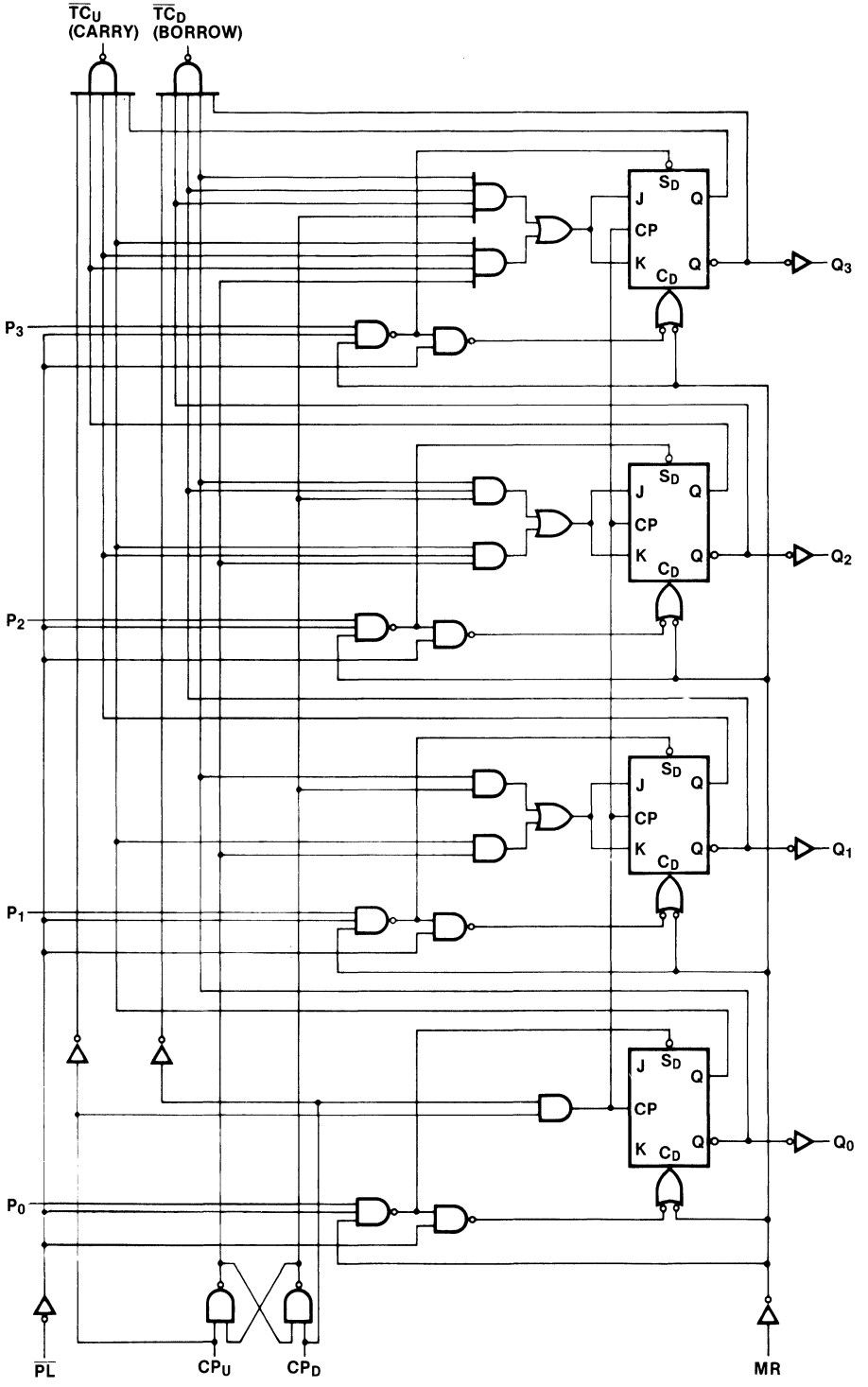
MR	$\overline{PL}$	CP_U	CP_D	Mode
H	X	X	X	Reset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	⌐	H	Count Up
L	H	H	⌐	Count Down

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

State Diagram



Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		38	55	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			54F T_A, V_{CC} = Mil C_L = 50 pF		74F T_A, V_{CC} = Com C_L = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Count Frequency	100	125		75		90		MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay CP_U or CP_D to $\overline{TC}_U$ or $\overline{TC}_D$	4.0 3.5	7.0 6.0	9.0 8.0	4.0 3.5	10.5 9.5	4.0 3.5	10.0 9.0	ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay CP_U or CP_D to Q_n	4.0 5.5	6.5 9.5	8.5 12.5	4.0 5.5	10.0 14.0	4.0 5.5	9.5 13.5	ns	3-1 3-7
t_{PLH} t_{PHL}	Propagation Delay P_n to Q_n	3.0 6.0	4.5 11.0	7.0 14.5	3.0 6.0	8.5 16.5	3.0 6.0	8.0 15.5	ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to Q_n	5.0 5.5	8.5 10.0	11.0 13.0	5.0 5.5	13.5 15.0	5.0 5.5	12.0 14.0	ns	3-1 3-10
t_{PHL}	Propagation Delay MR to Q_n	6.5	11.0	14.5	6.5	16.0	6.5	15.5	ns	3-1 3-11
t_{PLH}	Propagation Delay MR to $\overline{TC}_U$	6.0	10.5	13.5	6.0	15.0	6.0	14.5		
t_{PHL}	Propagation Delay MR to $\overline{TC}_D$	7.0	11.5	14.5	7.0	16.0	7.0	15.5		
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to $\overline{TC}_U$ or $\overline{TC}_D$	7.0 7.0	12.0 11.5	15.5 14.5	7.0 7.0	18.5 17.5	7.0 7.0	16.5 15.5	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay P_n to $\overline{TC}_U$ or $\overline{TC}_D$	7.0 6.5	11.5 11.0	14.5 14.0	7.0 6.5	16.5 16.5	7.0 6.5	15.5 15.0	ns	3-1 3-10

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW P_n to $\overline{PL}$	4.5 4.5	6.0 6.0	5.0 5.0	ns	3-14
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW P_n to $\overline{PL}$	2.0 2.0	2.0 2.0	2.0 2.0		
$t_w(L)$	$\overline{PL}$ Pulse Width, LOW	6.0	7.5	6.0	ns	3-11
$t_w(L)$	CP_U or CP_D Pulse Width, LOW	5.0	7.0	5.0	ns	3-7
$t_w(L)$	CP_U or CP_D Pulse Width, LOW (Change of Direction)	10.0	12.0	10.0	ns	3-7
$t_w(H)$	MR Pulse Width, HIGH	6.0	6.0	6.0	ns	3-11
t_{rec}	Recovery Time $\overline{PL}$ to CP_U or CP_D	6.0	8.0	6.0	ns	3-11
t_{rec}	Recovery Time MR to CP_U or CP_D	4.0	4.5	4.0	ns	3-11

54F/74F194

4-Bit Bidirectional Universal Shift Register

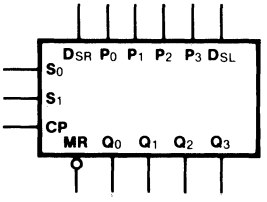
Description

The 'F194 is a high-speed 4-bit bidirectional universal shift register. As a high-speed, multifunctional, sequential building block, it is useful in a wide variety of applications. It may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial, and parallel-parallel data register transfers. The 'F194 is similar in operation to the 'F195 universal shift register, with added features of shift left without external connections and hold (do nothing) modes of operation.

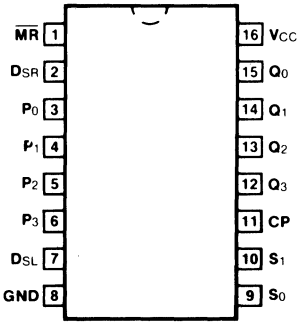
- **Typical Shift Frequency of 150 MHz**
- **Asynchronous Master Reset**
- **Hold (Do Nothing) Mode**
- **Fully Synchronous Serial or Parallel Data Transfers**

Ordering Code: See Section 5

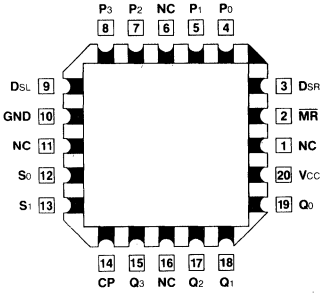
Logic Diagram



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
S_0, S_1	Mode Control Inputs	0.5/0.375
P_0-P_3	Parallel Data Inputs	0.5/0.375
D_{SR}	Serial Data Input (Shift Right)	0.5/0.375
D_{SL}	Serial Data Input (Shift Left)	0.5/0.375
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)	0.5/0.375
Q_0-Q_3	Parallel Outputs	25/12.5

Functional Description

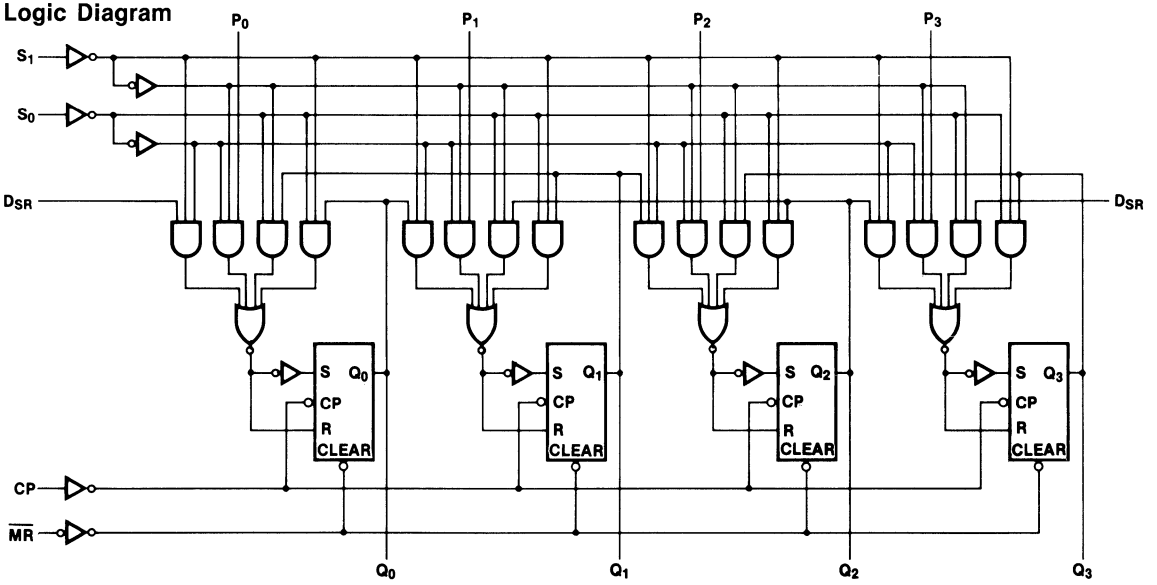
The 'F194 contains four edge-triggered D flip-flops and the necessary interstage logic to synchronously perform shift right, shift left, parallel load and hold operations. Signals applied to the Select (S_0, S_1) inputs determine the type of operation, as shown in the Mode Select Table. Signals on the Select, Parallel data (P_0-P_3) and Serial data (D_{SR}, D_{SL}) inputs can change when the clock is in either state, provided only that the recommended setup and hold times, with respect to the clock rising edge, are observed. A LOW signal on Master Reset ($\overline{MR}$) overrides all other inputs and forces the outputs LOW.

Mode Select Table

Operating Mode	Inputs						Outputs			
	$\overline{MR}$	S_1	S_0	D_{SR}	D_{SL}	P_n	Q_0	Q_1	Q_2	Q_3
Reset	L	X	X	X	X	X	L	L	L	L
Hold	H	l	l	X	X	X	q_0	q_1	q_2	q_3
Shift Left	H	h	l	X	l	X	q_1	q_2	q_3	L
	H	h	l	X	h	X	q_1	q_2	q_3	H
Shift Right	H	l	h	l	X	X	L	q_0	q_1	q_2
	H	l	h	h	X	X	H	q_0	q_1	q_2
Parallel Load	H	h	h	X	X	p_n	p_0	p_1	p_2	p_3

H = HIGH Voltage Level
L = LOW Voltage Level
$p_n(q_n)$ = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH clock transition.
X = Immaterial

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		33	46	mA	V_{CC} = Max S_n, $\overline{MR}$, D_{SR}, D_{SL} = HIGH P_n = Gnd, CP = ⎍

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			54F T_A, V_{CC} = Mil C_L = 50 pF		74F T_A, V_{CC} = Com C_L = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Shift Frequency	105	150		90		90		MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n	3.5 3.5	5.2 5.5	7.0 7.0	3.0 3.0	8.5 8.5	3.5 3.5	8.0 8.0	ns	3-1 3-7
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	4.5	8.6	12.0	4.5	14.5	4.5	14.0	ns	3-1 3-11

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F T_A = +25°C V_{CC} = +5.0 V			54F T_A, V_{CC} = Mil		74F T_A, V_{CC} = Com		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_s(H) t_s(L)	Setup Time, HIGH or LOW P_n or D_{SR} or D_{SL} to CP	4.0 4.0			4.0 4.0		4.0 4.0		ns	3-5
t_h(H) t_h(L)	Hold Time, HIGH or LOW P_n or D_{SR} or D_{SL} to CP	0 0			1.0 1.0		1.0 1.0			
t_s(H) t_s(L)	Setup Time, HIGH or LOW S_n to CP	8.0 8.0			9.5 8.0		9.0 8.0		ns	3-5
t_h(H) t_h(L)	Hold Time, HIGH or LOW S_n to CP	0 0			0 0		0 0			
t_w(H)	CP Pulse Width, HIGH	5.0			5.5		5.5		ns	3-7
t_w(L)	$\overline{MR}$ Pulse Width, LOW	5.0			5.0		5.0		ns	3-11
t_{rec}	Recovery Time $\overline{MR}$ to CP	7.0			9.0		8.0		ns	3-11

54F/74F195

4-Bit Parallel Access Shift Register

Description

The functional characteristics of the 'F195 4-Bit Parallel Access Shift Register are indicated in the Logic Diagram and Function Table. The device is useful in a wide variety of shifting, counting and storage applications. It performs serial, parallel, serial-to-parallel, or parallel-to-serial data transfers at very high speeds.

The 'F195 operates on two primary modes: shift right (Q_0-Q_1) and parallel load, which are controlled by the state of the Parallel Enable ($\overline{PE}$) input. Serial data enters the first flip-flop (Q_0) via the J and $\overline{K}$ inputs when the $\overline{PE}$ input is HIGH, and is shifted 1 bit in the direction Q_0-Q_1-Q_2-Q_3 following each LOW-to-HIGH clock transition. The J and $\overline{K}$ inputs provide the flexibility of the J$\overline{K}$ type input for special applications and, by tying the two pins together, the simple D-type input for general applications. The device appears as four common clocked D flip-flops when the $\overline{PE}$ input is LOW. After the LOW-to-HIGH clock transition, data on the parallel inputs (D_0-D_3) is transferred to the respective Q_0-Q_3 outputs. Shift left operation (Q_3-Q_2) can be achieved by tying the Q_n outputs to the D_{n-1} inputs and holding the $\overline{PE}$ input LOW.

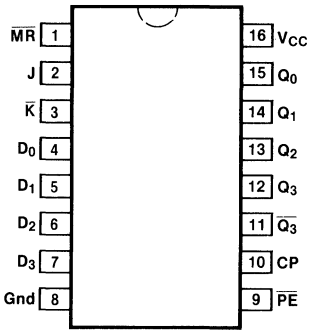
All parallel and serial data transfers are synchronous, occurring after each LOW-to-HIGH clock transition. The 'F195 utilizes edge-triggering, therefore, there is no restriction on the activity of the J, $\overline{K}$, D_n, and $\overline{PE}$ inputs for logic operation, other than the setup and release time requirements.

A LOW on the asynchronous Master Reset ($\overline{MR}$) input sets all Q outputs LOW, independent of any other input condition.

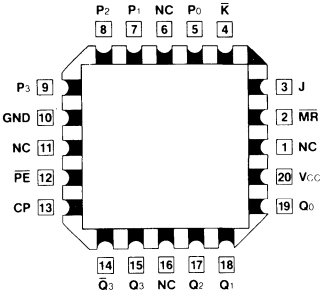
- **Shift Right and Parallel Load Capability**
- **J-$\overline{K}$ (D-Type) Inputs to First Stage**
- **Complement Output from Last Stage**
- **Asynchronous Master Reset**

Ordering Code: See Section 5

Connection Diagrams

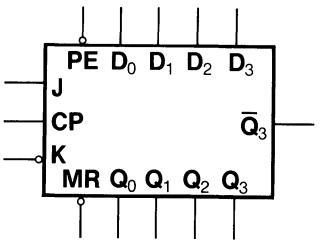


Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Logic Symbol



Input Loading/Fan-Out: See Section 3 for U.L. definitions

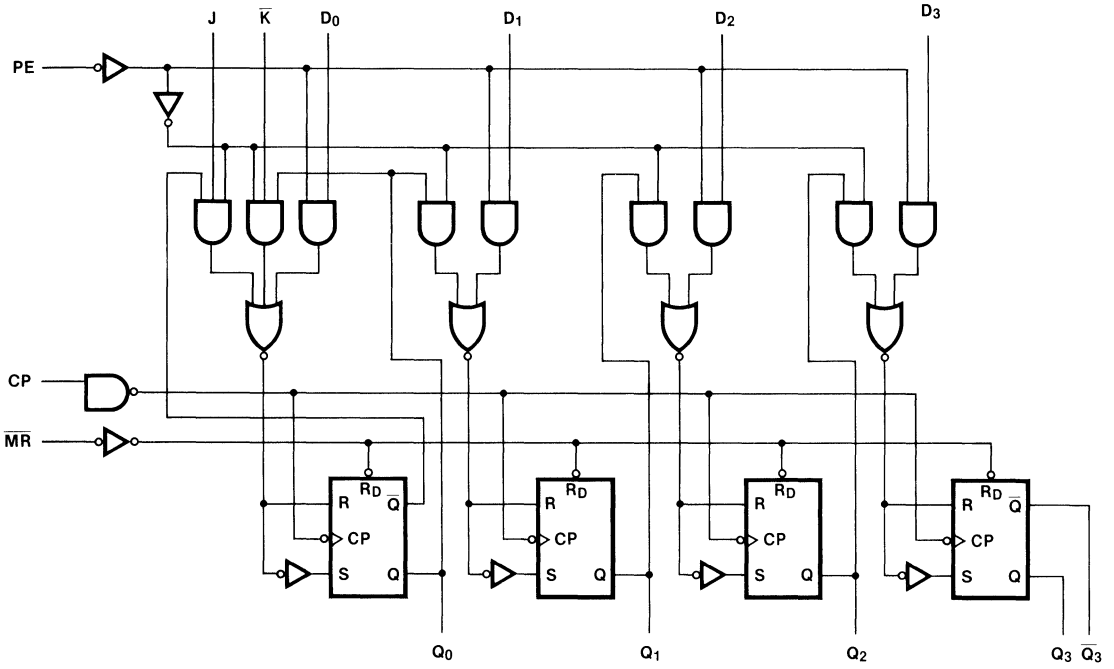
Pin Names	Description	54F/74F(U.L.) HIGH/LOW
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
D_0-D_3	Parallel Data Inputs	0.5/0.375
$\overline{PE}$	Parallel Enable Input	0.5/0.375
$\overline{MR}$	Asynchronous Master Reset	0.5/0.375
J, $\overline{K}$	J-$\overline{K}$ or D Type Serial Inputs	0.5/0.375
Q_0-Q_3,$\overline{Q}_3$	Outputs	25/0.375

Mode Select-Function Table

Operating Modes	Inputs						Outputs				
	$\overline{MR}$	CP	$\overline{PE}$	J	$\overline{K}$	D_n	Q_0	Q_1	Q_2	Q_3	$\overline{Q}_3$
Asynchronous Reset	L	X	X	X	X	X	L	L	L	L	H
Shift, Set First Stage	H	↑	h	h	h	X	H	q_0	q_1	q_2	$\overline{q}_2$
Shift, Reset First Stage	H	↑	h	l	l	X	L	q_0	q_1	q_2	$\overline{q}_2$
Shift, Toggle First Stage	H	↑	h	h	l	X	$\overline{q}_0$	q_0	q_1	q_2	$\overline{q}_2$
Shift, Retain First Stage	H	↑	h	l	h	X	q_0	q_0	q_1	q_2	$\overline{q}_2$
Parallel Load	H	↑	l	X	X	d_n	d_0	d_1	d_2	d_3	$\overline{d}_3$

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH clock transition.
↑ = LOW-to-HIGH clock transition.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current				mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	105	150						MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay Clock to Output			7.0 7.0					ns	3-1 3-7
t_{PHL}	Propagation Delay $\overline{MR}$ to Output			12.0					ns	3-1 3-11

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW J, $\overline{K}$ and D_n to CP	4.0 4.0							ns	3.5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW J, $\overline{K}$ or D_n to CP	0 0							ns	3-5
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{PE}$ to CP	8.0 8.0							ns	3-14
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{PE}$ to CP	0 0							ns	3-14
$t_w(H)$	Clock Pulse Width, HIGH	5.0							ns	3-7
$t_w(L)$	$\overline{MR}$ Pulse Width, LOW	5.0							ns	3-11
t_{rec}	Recovery Time, $\overline{MR}$ to CP	7.0							ns	3-11

54F/74F211

144-Bit Random Access Memory With 3-State Outputs

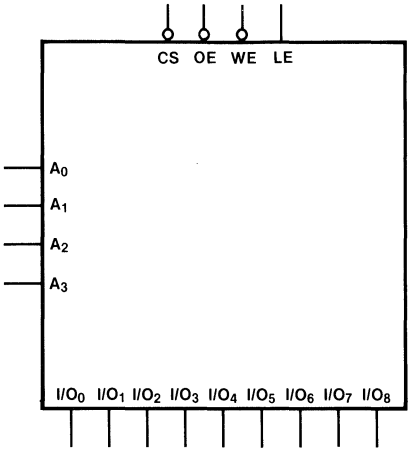
Description

The 'F211 is a high-speed 144-bit Random Access Memory (RAM) organized as a 16-word by 9-bit array. It contains output latches that are transparent when the Latch Enable (LE) is HIGH. Inputs are buffered to minimize loading and are fully decoded on chip. The output buffers are active only in the Read mode when Chip Select ($\overline{CS}$) and Output Enable ($\overline{OE}$) are LOW, and Write Enable ($\overline{WE}$) is HIGH; otherwise, the outputs are in the high-impedance state.

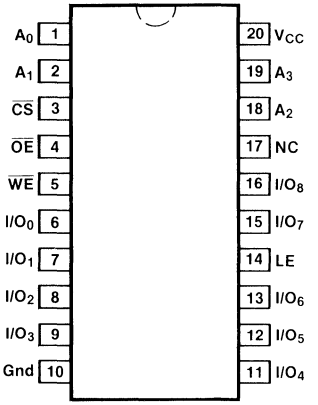
- **3-State Outputs for Bus Applications**
- **Buffered Inputs for Minimum Loading**
- **Address Decoding on Chip**
- **Address Access Time 15 ns Typ**
- **Chip Select Access Time 8 ns Typ**
- **Supply Current 80 mA Typ**

Ordering Code: See Section 5

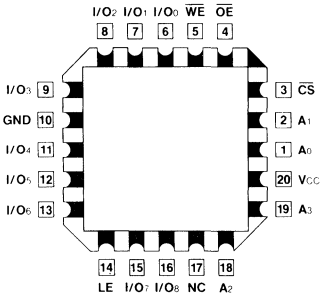
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC

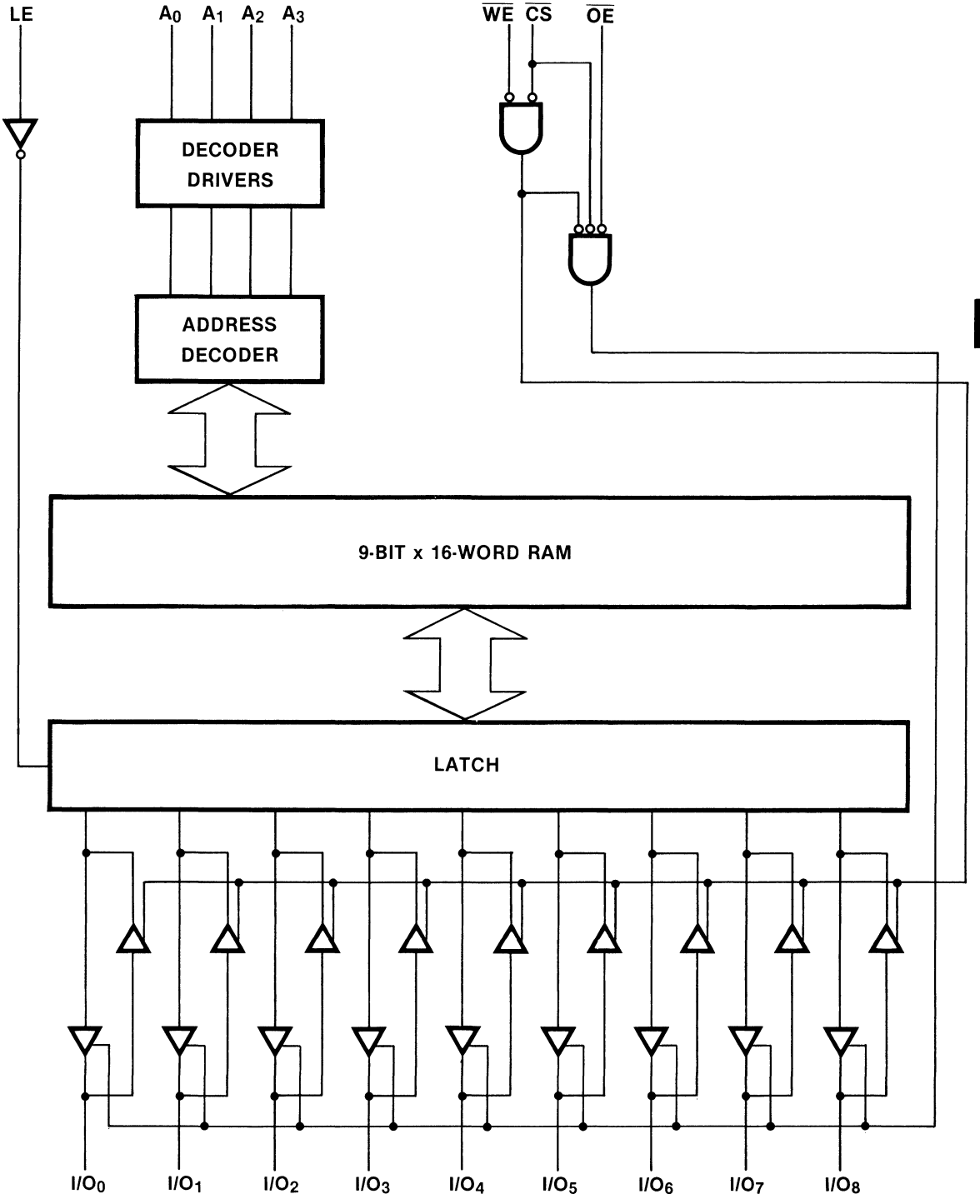


Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
$\overline{CS}$	Chip Select	0.5/0.75
$\overline{OE}$	Output Enable	0.5/0.375
$\overline{WE}$	Write Enable	0.5/0.375
A_n	Address Inputs	0.5/0.375
I/O_0-I/O_8	Parallel Data Inputs	1.75/0.406
	or 3-State Parallel Outputs	75/15 (12.5)
LE	Latch Enable	0.5/0.375

Block Diagram



Function Table

Inputs				Operation	Output
$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	LE		
H	X	X	X	Inhibit	High Impedance
L	L	X	X	Write	High Impedance
L	H	H	X	Read	High Impedance
L	H	L	L	Read	Contents of Latch Buffers
L	H	L	H	Read	Contents of Memory Location Addressed

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		80	120	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n to O_n		21.0 28.0						ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay LE to O_n		16.0 12.0						ns	3-1 3-10
t_{PZH} t_{PZL}	Enable Time $\overline{CS}$ to O_n		13.0 13.0						ns	3-1, 3-12 3-13
t_{PHZ} t_{PLZ}	Disable Time $\overline{CS}$ to O_n		11.0 11.0						ns	3-1, 3-12 3-13
t_{PZH} t_{PZL}	Enable Time $\overline{OE}$ to O_n		13.0 13.0						ns	3-1, 3-12 3-13
t_{PHZ} t_{PLZ}	Disable Time $\overline{OE}$ to O_n		11.0 11.0						ns	3-1, 3-12 3-13
t_{PZH} t_{PZL}	Enable Time $\overline{WE}$ to O_n		16.0 16.0						ns	3-1, 3-12 3-13
t_{PHZ} t_{PLZ}	Disable Time $\overline{WE}$ to O_n		13.0 13.0						ns	3-1, 3-12 3-13

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW A_n to $\overline{WE}$	0 0			ns	3-16
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW A_n to $\overline{WE}$	0 0				
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW I/O to $\overline{WE}$	5.0 5.0			ns	3-14
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW I/O to $\overline{WE}$	0 0				
$t_s(L)$	Setup Time, LOW $\overline{CS}$ to $\overline{WE}$	5.0			ns	3-14
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW A_n to LE	15.0 15.0			ns	3-16
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW A_n to LE	0 0				
$t_w(L)$	$\overline{WE}$ Pulse Width, LOW	5.0			ns	3-16

54F/74F212

144-Bit Random Access Memory With 3-State Outputs

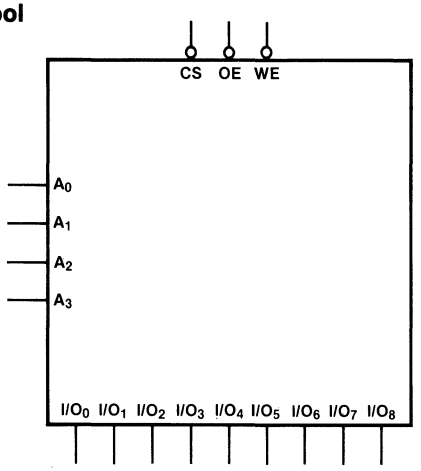
Description

The 'F212 is a high-speed 144-bit Random Access Memory (RAM) organized as a 16-word by 9-bit array. Address inputs are buffered to minimize loading and are fully decoded on chip. The output buffers are active only in the Read mode when Chip Select ($\overline{CS}$) and Output Enable ($\overline{OE}$) are LOW, and Write Enable ($\overline{WE}$) is HIGH; otherwise, the outputs are in the high-impedance state.

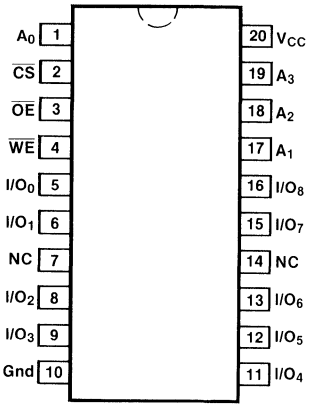
- **3-State Outputs for Bus Applications**
- **Buffered Inputs for Minimum Loading**
- **Address Decoding on Chip**
- **Address Access Time 15 ns Typ**
- **Chip Select Access Time 8 ns Typ**
- **Supply Current 80 mA Typ**

Ordering Code: See Section 5

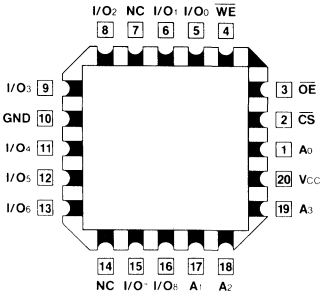
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC

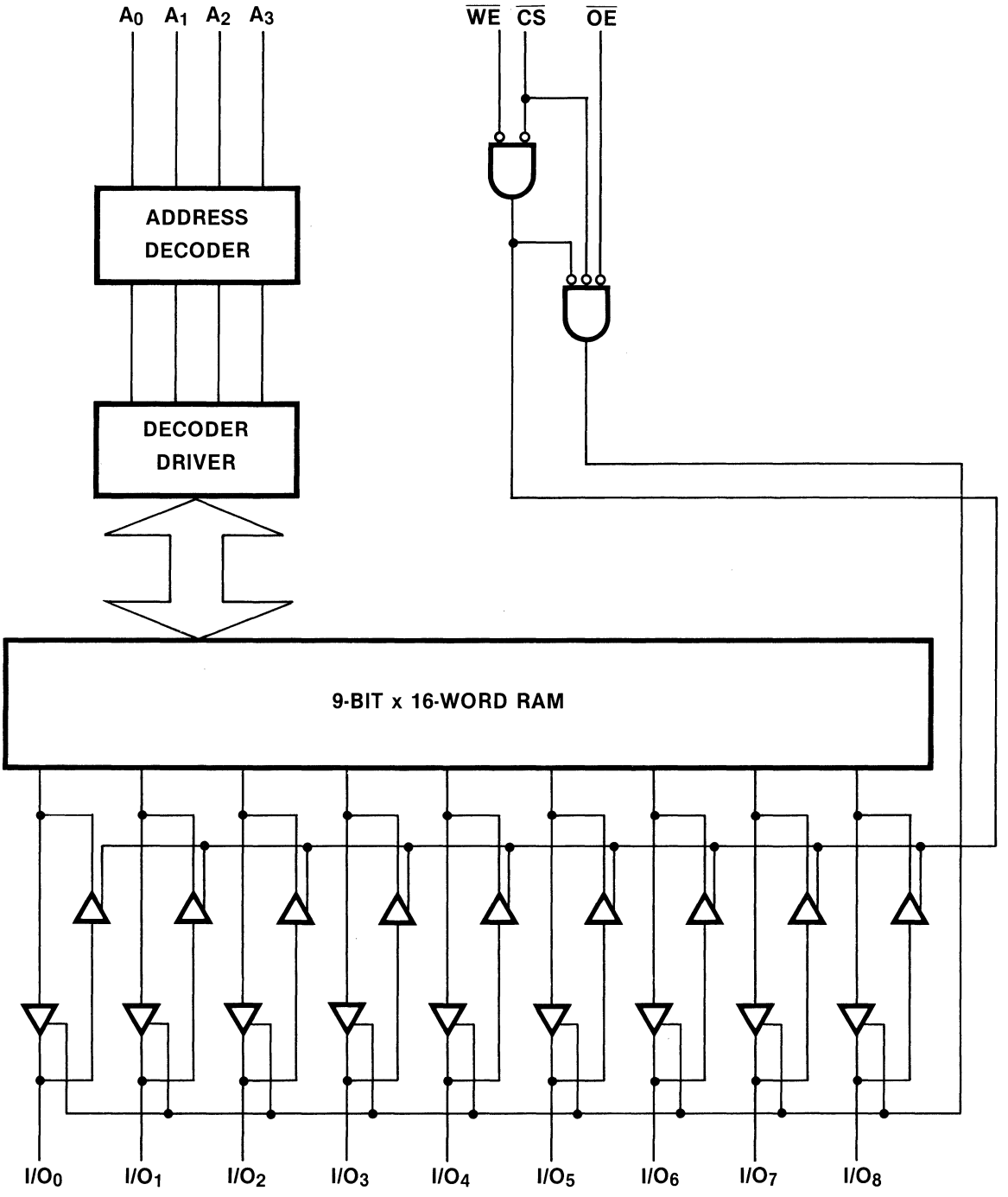


Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
$\overline{CS}$	Chip Select	0.5/.75
$\overline{OE}$	Output Enable	0.5/.375
$\overline{WE}$	Write Enable	0.5/.375
A_n	Address Inputs	0.5/.375
I/O_0-I/O_8	Parallel Data Inputs	1.75/0.406
	or 3-State Parallel Outputs	75/15 (12.5)

Block Diagram



Function Table

Inputs			Operation	Output
$\overline{CS}$	$\overline{OE}$	$\overline{WE}$		
H	X	X	Inhibit	High Impedance
L	X	L	Write	High Impedance
L	H	H	Read	High Impedance
L	L	H	Read	Read Addressed Memory Location

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		80	120	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n to O_n		21.0 28.0						ns	3-1 3-10
t_{PZH} t_{PZL}	Enable Time $\overline{CS}$ to O_n		13.0 13.0						ns	3-1, 3-12 3-13
t_{PHZ} t_{PLZ}	Disable Time $\overline{CS}$ to O_n		11.0 11.0						ns	3-1, 3-12 3-13
t_{PZH} t_{PZL}	Enable Time $\overline{OE}$ to O_n		13.0 13.0						ns	3-1, 3-12 3-13
t_{PHZ} t_{PLZ}	Disable Time $\overline{OE}$ to O_n		11.0 11.0						ns	3-1, 3-12 3-13
t_{PZH} t_{PZL}	Enable Time $\overline{WE}$ to O_n		16.0 16.0						ns	3-1, 3-12 3-13
t_{PHZ} t_{PLZ}	Disable Time $\overline{WE}$ to O_n		13.0 13.0						ns	3-1, 3-12 3-13

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW A_n to $\overline{WE}$	0 0			ns	3-16
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW A_n to $\overline{WE}$	0 0				
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW I/O to $\overline{WE}$	5.0 5.0			ns	3-14
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW I/O to $\overline{WE}$	0 0				
$t_s(L)$	Setup Time, LOW $\overline{CS}$ to $\overline{WE}$	5.0			ns	3-14
$t_w(L)$	$\overline{WE}$ Pulse Width, LOW	5.0			ns	3-16

54F/74F213

192-Bit Random Access Memory With 3-State Outputs

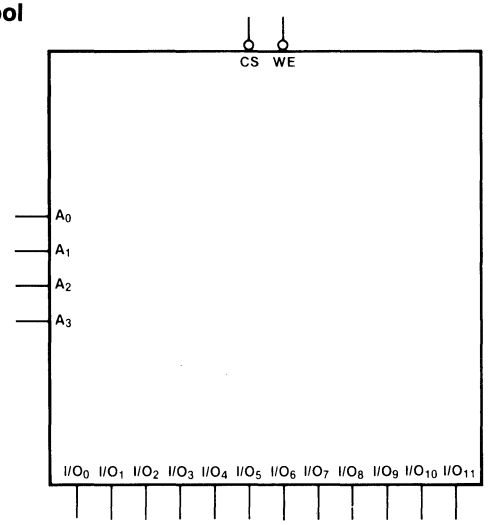
Description

The 'F213 is a high-speed 192-bit Random Access Memory (RAM) organized as a 16-word by 12-bit array. Inputs are buffered to minimize loading and are fully decoded on chip. The output buffers are active only in the Read mode when Chip Select ($\overline{CS}$) is LOW and Write Enable ($\overline{WE}$) is HIGH; otherwise, the outputs are in the high-impedance state.

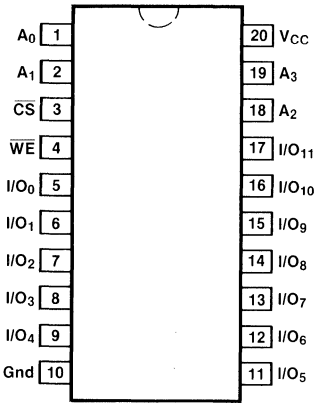
- **3-State Outputs for Bus Applications**
- **Buffered Inputs for Minimum Loading**
- **Address Decoding on Chip**
- **Address Access Time 15 ns Typ**
- **Chip Select Access Time 8 ns Typ**
- **Supply Current 80 mA Typ**

Ordering Code: See Section 5

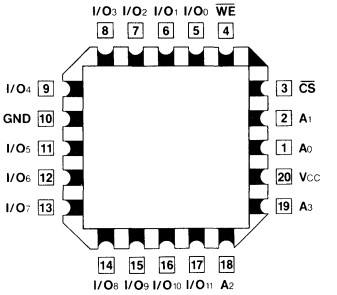
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

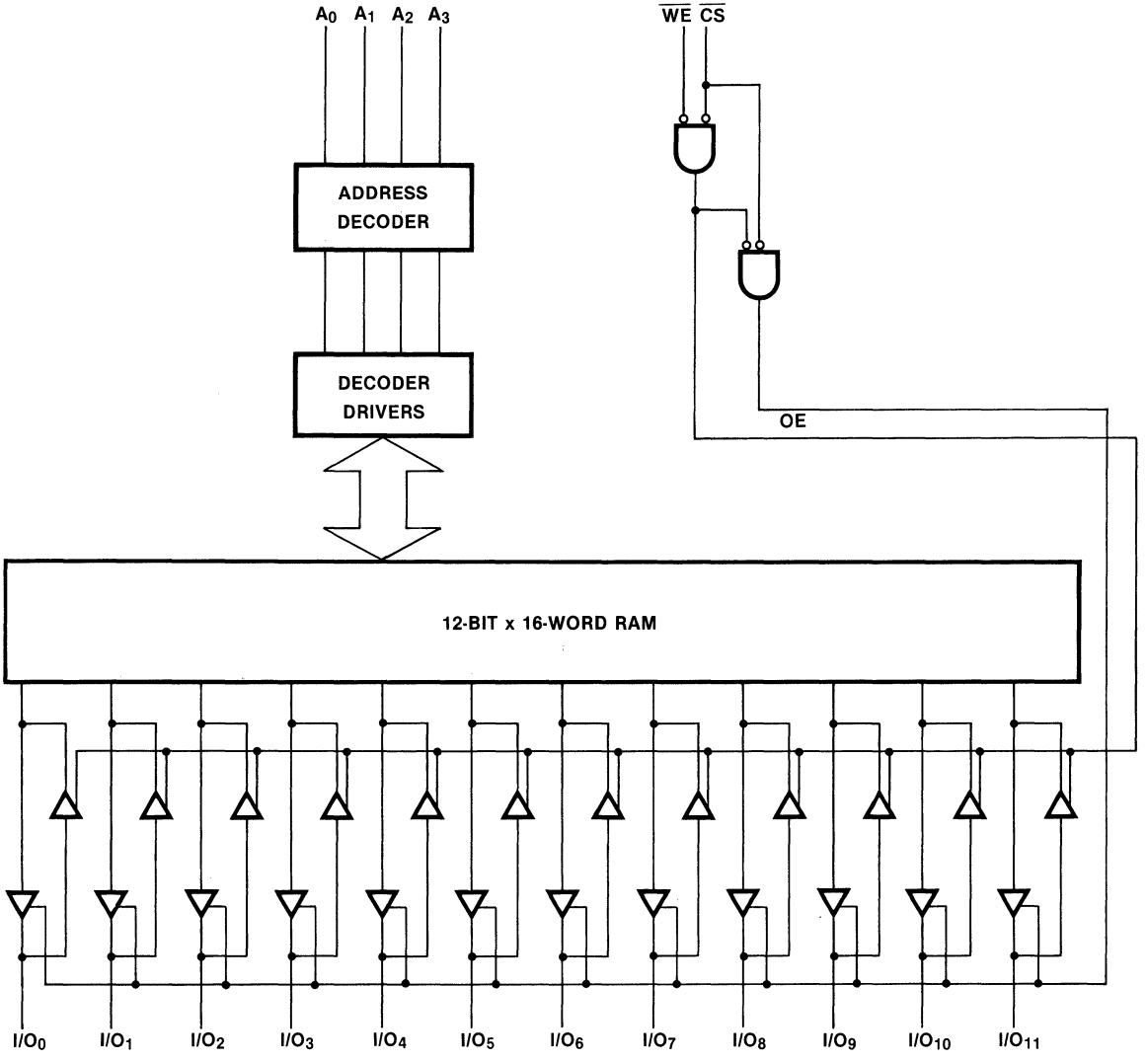
Pin Names	Description	54F/74F(U.L.) HIGH/LOW
$\overline{CS}$	Chip Select	0.5/.75
$\overline{WE}$	Write Enable	0.5/.375
A_n	Address Inputs	0.5/.375
I/O_0-I/O_8	Parallel Data Inputs or 3-State Parallel Outputs	1.75/0.406 75/15 (12.5)

Function Table

Inputs		Operation	Output
$\overline{CS}$	$\overline{WE}$		
H	X	Inhibit	High Impedance
L	L	Write	High Impedance
L	H	Read	Read Addressed Memory Location

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Block Diagram



DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		80	120	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF	T_A, V_{CC} = Mil, C_L = 50 pF	T_A, V_{CC} = Com, C_L = 50 pF		
		Min Typ Max	Min Max	Min Max		
t_{PLH} t_{PHL}	Propagation Delay A_n to O_n	21.0 28.0			ns	3-1 3-10
t_{PZH} t_{PZL}	Enable Time $\overline{CS}$ to O_n	13.0 13.0			ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Disable Time $\overline{CS}$ to O_n	11.0 11.0				
t_{PZH} t_{PZL}	Enable Time $\overline{WE}$ to O_n	16.0 16.0			ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Disable Time $\overline{WE}$ to O_n	13.0 13.0				

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
t_s(H) t_s(L)	Setup Time, HIGH or LOW A_n to $\overline{WE}$	0 0			ns	3-16
t_h(H) t_h(L)	Hold Time, HIGH or LOW A_n to $\overline{WE}$	0 0				
t_s(H) t_s(L)	Setup Time, HIGH or LOW I/O to $\overline{WE}$	5.0 5.0			ns	3-14
t_h(H) t_h(L)	Hold Time, HIGH or LOW I/O to $\overline{WE}$	0 0				
t_s(L)	Setup Time, LOW $\overline{CS}$ to $\overline{WE}$	5.0			ns	3-14
t_w(L)	$\overline{WE}$ Pulse Width, LOW	5.0			ns	3-16

54F/74F219

64-Bit Random Access Memory With 3-State Outputs

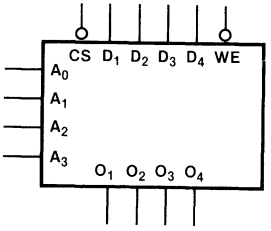
Description

The 'F219 is a high-speed 64-bit RAM organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading and are fully decoded on-chip. The outputs are 3-state and are in the high-impedance state whenever the Chip Select ($\overline{CS}$) input is HIGH. The outputs are active only in the Read mode. This device is similar to the 'F189 but features non-inverting, rather than inverting, data outputs.

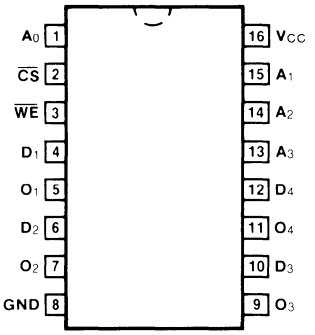
- **3-State Outputs for Data Bus Applications**
- **Buffered Inputs Minimize Loading**
- **Address Decoding On-Chip**
- **Diode Clamped Inputs Minimize Ringing**

Ordering Code: See Section 5

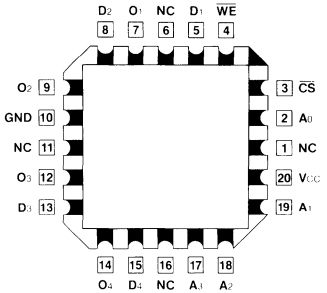
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

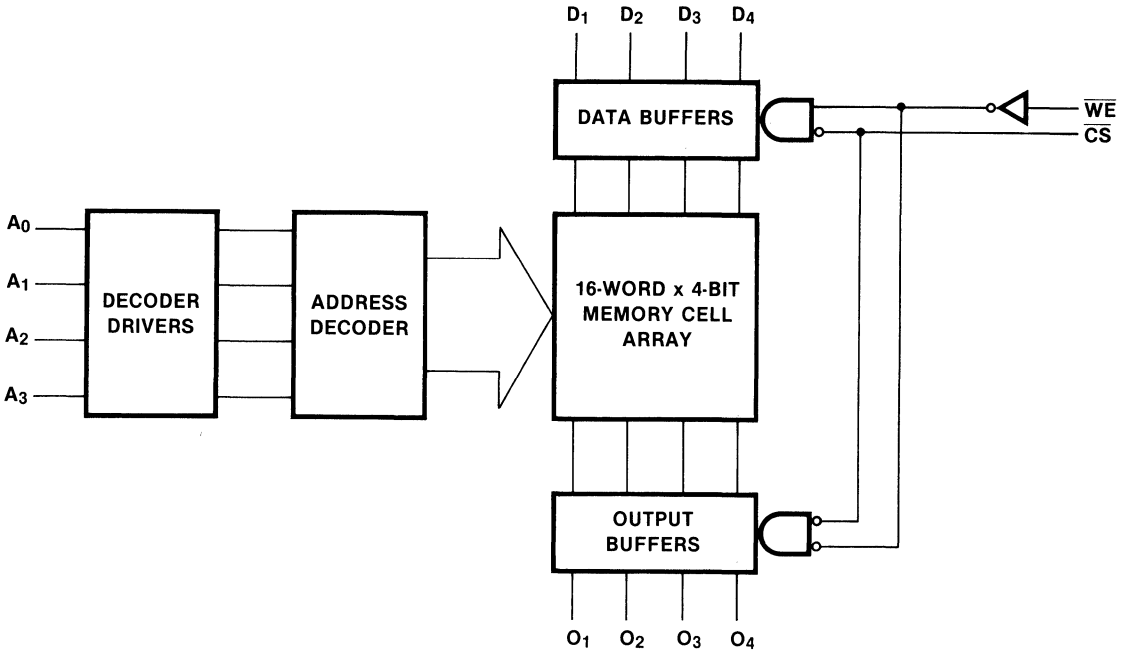
Pin Names	Description	54F/74F(U.L.) HIGH/LOW
A_0-A_3	Address Inputs	0.5/0.375
$\overline{CS}$	Chip Select Input (Active LOW)	0.5/0.75
$\overline{WE}$	Write Enable Input (Active LOW)	0.5/0.375
D_1-D_4	Data Inputs	0.5/0.375
O_1-O_4	3-State Data Outputs	75/15 (12.5)

Function Table

Inputs		Operation	Condition of Outputs
$\overline{CS}$	$\overline{WE}$		
L	L	Write	High Impedance
L	H	Read	True Stored Data
H	X	Inhibit	High Impedance

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Block Diagram



DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		37	55	mA	V_{CC} = Max; $\overline{WE}$, $\overline{CS}$ = Gnd

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$	T_A, V_{CC} = Mil $C_L = 50\ pF$	T_A, V_{CC} = Com $C_L = 50\ pF$		
		Min Typ Max	Min Max	Min Max		
t_{PLH} t_{PHL}	Access Time, HIGH or LOW A_n to O_n	11.0 18.5 26.0 8.0 13.5 19.0	9.0 32.0 8.0 23.0	11.0 27.0 8.0 20.0	ns	3-1 3-10
t_{PZH} t_{PZL}	Access Time, HIGH or LOW $\overline{CS}$ to O_n	3.5 6.0 8.5 5.0 9.0 13.0	3.5 10.5 5.0 15.0	3.5 9.5 5.0 14.0	ns	3-1, 3-12 3-13
t_{PHZ} t_{PLZ}	Disable Time, HIGH or LOW $\overline{CS}$ to O_n	2.0 4.0 6.0 3.0 5.5 8.0	2.0 8.0 2.5 10.0	2.0 7.0 3.0 9.0		
t_{PZH} t_{PZL}	Write Recovery Time HIGH or LOW, $\overline{WE}$ to O_n	6.5 20.0 28.0 6.5 11.0 15.5	6.5 37.5 6.5 17.5	6.5 29.0 6.5 16.5	ns	3-1, 3-12 3-13
t_{PHZ} t_{PLZ}	Disable time, HIGH or LOW $\overline{WE}$ to O_n	4.0 7.0 10.0 5.0 9.0 13.0	3.5 12.0 5.0 15.0	4.0 11.0 5.0 14.0		

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW A_n to $\overline{WE}$	0 0	0 0	0 0	ns	3-16
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW A_n to $\overline{WE}$	2.0 2.0	2.0 2.0	2.0 2.0		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW D_n to $\overline{WE}$	10.0 10.0	11.0 11.0	10.0 10.0	ns	3-14
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D_n to $\overline{WE}$	0 0	2.0 2.0	0 0		
$t_s(L)$	Setup Time, LOW $\overline{CS}$ to $\overline{WE}$	0	0	0	ns	3-14
$t_h(L)$	Hold Time, LOW $\overline{CS}$ to $\overline{WE}$	6.0	7.5	6.0		
$t_w(L)$	$\overline{WE}$ Pulse Width, LOW	6.0	7.5	6.0	ns	3-16

54F/74F240 • 54F/74F241 • 54F/74F244

Octal Buffers/Line Drivers With 3-State Outputs

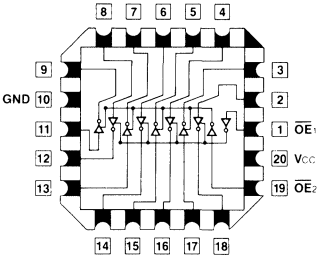
Description

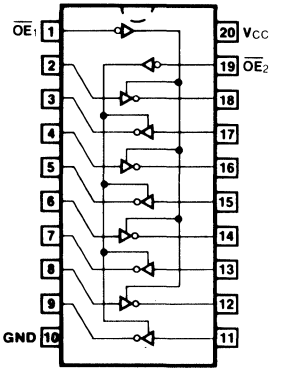
The 'F240, 'F241 and 'F244 are octal buffers and line drivers designed to be employed as memory and address drivers, clock drivers and bus-oriented transmitters/receivers which provide improved PC and board density.

- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Outputs Sink 64 mA**
- **15 mA Source Current**
- **Input Clamp Diodes Limit High-Speed Termination Effects**

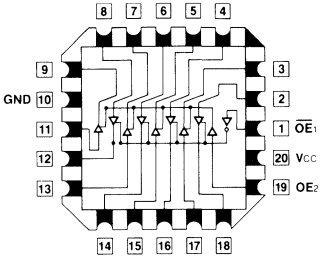
Ordering Code: See Section 5

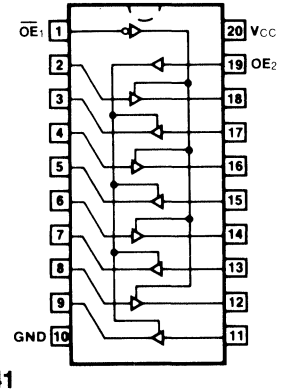
Connection Diagrams



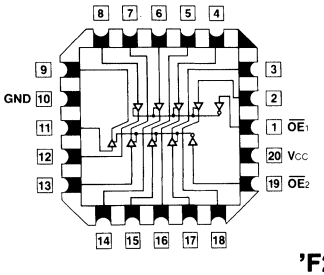


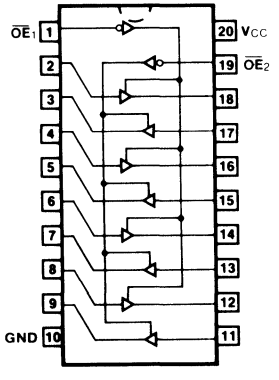
'F240





'F241





'F244

Pin Assignment for LCC and PCC

Pin Assignment for DIP and SOIC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
$\overline{OE}_1$, $\overline{OE}_2$	3-State Output Enable Input (Active LOW)	0.5/0.625
OE_2	3-State Output Enable Input (Active HIGH)	0.5/0.625
	Inputs ('F240)	0.5/0.625*
	Inputs ('F241, 'F244)	0.5/1.0*
	Outputs	75/40 (30)

*Worst-case 'F240 enabled; 'F241, 'F244 disabled

Truth Tables

'F240

Inputs		Output
$\overline{OE}_1$, $\overline{OE}_2$	D	
L	L	H
L	H	L
H	X	Z

'F244

Inputs		Output
$\overline{OE}_1$, $\overline{OE}_2$	D	
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

'F241

Inputs			Output
$\overline{OE}_1$	OE_2	D	
L	H	L	L
L	H	H	H
H	L	X	Z

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F Min	54F/74F Typ	54F/74F Max	Units	Conditions	
I_{CCH}	Power Supply Current 'F240		19	29	mA	Outputs HIGH	V_{CC} = Max
I_{CCL}			50	75		Outputs LOW	
I_{CCZ}			42	63		Outputs OFF	
I_{CCH}	Power Supply Current ('F241, 'F244)		40	60	mA	Outputs HIGH	
I_{CCL}			60	90		Outputs LOW	
I_{CCZ}			60	90		Outputs OFF	

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF Min	Typ	Max	54F T_A, V_{CC} = Mil, C_L = 50 pF Min	Max	74F T_A, V_{CC} = Com, C_L = 50 pF Min	Max	Units	Fig. No.
t_{PLH}	Propagation Delay	3.0	5.1	7.0	3.0	9.0	3.0	8.0	ns	3-1
t_{PHL}	Data to Output ('F240)	2.0	3.5	4.7	2.0	6.0	2.0	5.7		3-3
t_{PZH}	Output Enable Time ('F240)	2.0	3.5	4.7	2.0	6.5	2.0	5.7	ns	3-1
t_{PZL}		4.0	6.9	9.0	4.0	10.5	4.0	10.0		3-12
t_{PHZ}	Output Disable Time ('F240)	2.0	4.0	5.3	2.0	6.5	2.0	6.3		3-13
t_{PLZ}		2.0	6.0	8.0	2.0	12.5	2.0	9.5		
t_{PLH}	Propagation Delay	2.5	4.0	5.2	2.0	6.5	2.5	6.2	ns	3-1
t_{PHL}	Data to Output ('F241, 'F244)	2.5	4.0	5.2	2.0	7.0	2.5	6.5		3-4
t_{PZH}	Output Enable Time	2.0	4.3	5.7	2.0	7.0	2.0	6.7	ns	3-1
t_{PZL}	('F241, 'F244)	2.0	5.4	7.0	2.0	8.5	2.0	8.0		3-12
t_{PHZ}	Output Disable Time	2.0	4.5	6.0	2.0	7.0	2.0	7.0		3-13
t_{PLZ}	('F241, 'F244)	2.0	4.5	6.0	2.0	7.5	2.0	7.0		

54F/74F242 • 54F/74F243

Quad Bus Transceiver
With 3-State Outputs

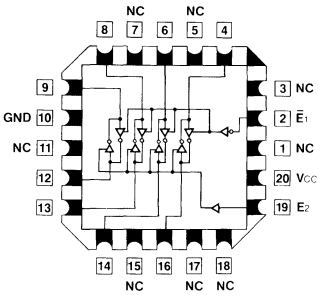
Description

The 'F242 and 'F243 are quad bus transmitters/receivers designed for 4-line asynchronous 2-way data communications between data busses.

- **2-Way Asynchronous Data Bus Communication**
- **Input Clamp Diodes Limit High-Speed Termination Effects**

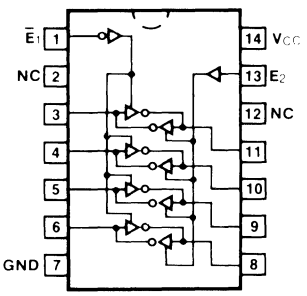
Ordering Code: See Section 5

Connection Diagrams

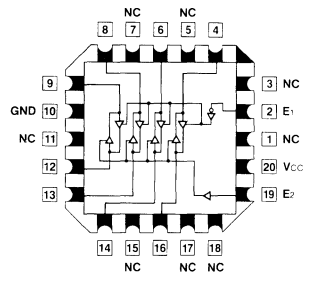


'F242

Pin Assignment for LCC and PCC

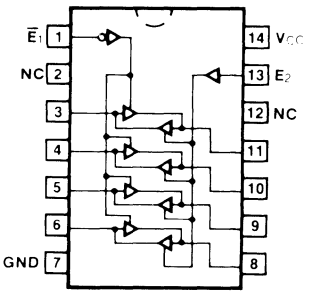


Pin Assignment for DIP and SOIC



'F243

Pin Assignment for LCC and PCC



Pin Assignment for DIP and SOIC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
$\overline{E}_1$	Enable Input (Active LOW)	0.5/0.625
E_2	Enable Input (Active HIGH)	0.5/0.625
	Inputs ('F242)	1.75/0.625*
	Inputs ('F243)	1.75/1.0*
	Outputs	75/40 (30)

*Worst-case ('F242 enabled, 'F243 disabled)

Truth Tables

'F242

Inputs		Output
$\overline{E}_1$	D	
L	L	H
L	H	L
H	X	Z

Inputs		Output
E_2	D	
L	X	Z
H	L	H
H	H	L

'F243

Inputs		Output
$\overline{E}_1$	D	
L	L	L
L	H	H
H	X	Z

Inputs		Output
E_2	D	
L	X	Z
H	L	L
H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions	
		Min	Typ	Max			
I_{CCH}	Power Supply Current 'F242		30	46	mA	Outputs HIGH	V_{CC} = Max
I_{CCL}			46	69		Outputs LOW	
I_{CCZ}			42	63		Outputs OFF	
I_{CCH}	Power Supply Current 'F243		64	80	mA	Outputs HIGH	
I_{CCL}			64	90		Outputs LOW	
I_{CCZ}			71	90		Outputs OFF	

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F $T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$			54F $T_A, V_{CC} =$ Mil $C_L = 50\ pF$		74F $T_A, V_{CC} =$ Com $C_L = 50\ pF$		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output ('F242)			7.0 4.7					ns	3-1 3-3
t_{PZH} t_{PZL}	Output Enable Time ('F242)			4.7 9.0					ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time ('F242)			5.3 6.5						

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F $T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$			54F $T_A, V_{CC} =$ Mil $C_L = 50\ pF$		74F $T_A, V_{CC} =$ Com $C_L = 50\ pF$		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output ('F243)	2.5 2.5	4.0 4.0	5.2 5.2	2.0 2.0	6.5 8.5	2.0 2.0	6.2 6.5	ns	3-1 3-4
t_{PZH} t_{PZL}	Output Enable Time ('F243)	2.0 2.0	4.3 5.8	5.7 7.5	2.0 2.0	8.0 10.5	2.0 2.0	6.7 8.5	ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time ('F243)	2.0 2.0	4.5 4.5	6.0 6.0	1.5 2.0	7.5 8.5	1.5 2.0	7.0 7.0		

54F/74F245

Octal Bidirectional Transceiver With 3-State Inputs/Outputs

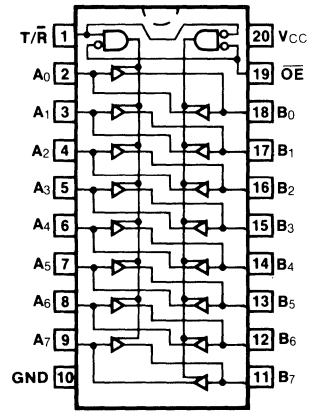
Description

The 'F245 contains eight non-inverting bidirectional buffers with 3-state outputs and is intended for bus-oriented applications. Current sinking capability is 20 mA at the A ports and 64 mA at the B ports. The Transmit/Receive ($T/\overline{R}$) input determines the direction of data flow through the bidirectional transceiver. Transmit (active HIGH) enables data from A ports to B ports; Receive (active LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a High Z condition.

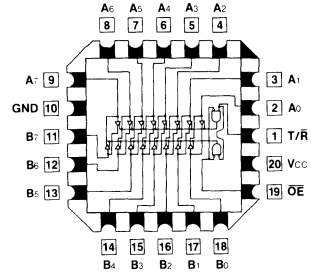
- **Non-Inverting Buffers**
- **Bidirectional Data Path**
- **B Outputs Sink 64 mA**

Ordering Code: See Section 5

Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
$\overline{OE}$	Output Enable Input (Active LOW)	0.5/0.75
$T/\overline{R}$	Transmit/Receive Input	0.5/0.75
A_0-A_7	Side A 3-State Inputs	1.75/0.406
	3-State Outputs	75/15 (12.5)
B_0-B_7	Side B 3-State Inputs or	1.75/0.406
	3-State Outputs	75/40 (30)

Truth Table

Inputs		Output
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CCH}	Power Supply Current		70	90	mA	V_{CC} = Max
I_{CCL}			95	120		
I_{CCZ}			85	110		

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	2.5	4.2	6.0	2.0	7.5	2.5	7.0	ns	3-1
t_{PHL}	A_n to B_n or B_n to A_n	2.5	4.6	6.0	2.0	7.5	2.5	7.0		3-4
t_{PZH}	Output Enable Time	3.0	5.3	7.0	2.5	9.0	3.0	8.0	ns	3-1, 3-12, 3-13
t_{PZL}		3.5	6.0	8.0	3.0	10.0	3.5	9.0		
t_{PHZ}	Output Disable Time	3.0	5.0	6.5	2.5	9.0	3.0	7.5		
t_{PLZ}		2.0	5.0	6.5	2.0	10.0	2.0	7.5		

54F/74F251A

8-Input Multiplexer With 3-State Outputs

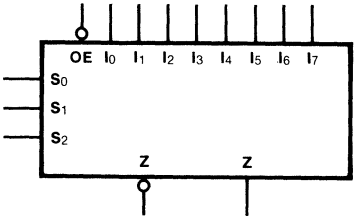
Description

The 'F251A is a high-speed 8-input digital multiplexer. It provides, in one package, the ability to select one bit of data from up to eight sources. It can be used as universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided.

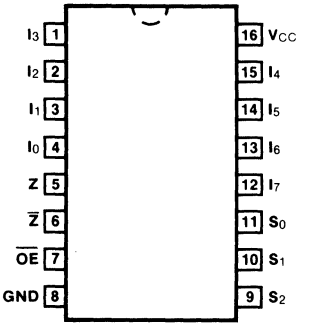
- **Multifunctional Capability**
- **On-Chip Select Logic Decoding**
- **Inverting and Non-Inverting 3-State Outputs**

Ordering Code: See Section 5

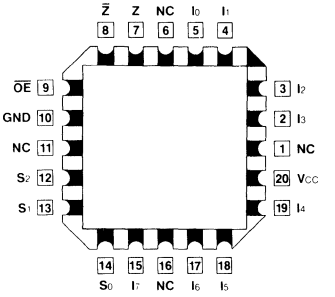
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
S_0-S_2	Select Inputs	0.5/0.375
$\overline{OE}$	3-State Output Enable Input (Active LOW)	0.5/0.375
I_0-I_7	Multiplexer Inputs	0.5/0.375
Z	3-State Multiplexer Output	75/15 (12.5)
$\overline{Z}$	Complementary 3-State Multiplexer Output	75/15 (12.5)

Functional Description

This device is a logical implementation of a single-pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0, S_1, S_2. Both assertion and negation outputs are provided. The Output Enable input ($\overline{OE}$) is active LOW. When it is activated, the logic function provided at the output is:

$$Z = \overline{OE} \bullet (I_0 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_1 \bullet S_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_2 \bullet \overline{S}_0 \bullet S_1 \bullet \overline{S}_2 + I_3 \bullet S_0 \bullet S_1 \bullet \overline{S}_2 + I_4 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet S_2 + I_5 \bullet S_0 \bullet \overline{S}_1 \bullet S_2 + I_6 \bullet \overline{S}_0 \bullet S_1 \bullet S_2 + I_7 \bullet S_0 \bullet S_1 \bullet S_2)$$

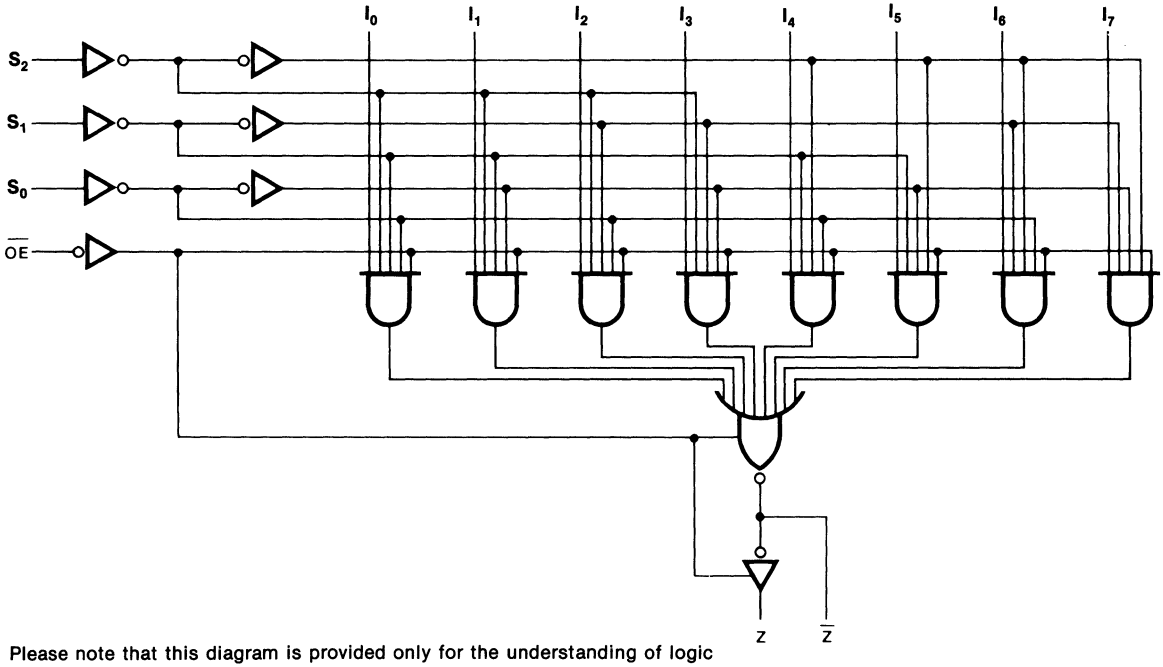
When the Output Enable is HIGH, both outputs are in the high impedance (High Z) state. This feature allows multiplexer expansion by tying the outputs of up to 128 devices together. When the outputs of the 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. The Output Enable signals should be designed to ensure there is no overlap in the active LOW portion of the enable voltages.

Truth Table

Inputs				Outputs	
$\overline{OE}$	S_2	S_1	S_0	$\overline{Z}$	Z
H	X	X	X	Z	Z
L	L	L	L	$\overline{I}_0$	I_0
L	L	L	H	$\overline{I}_1$	I_1
L	L	H	L	$\overline{I}_2$	I_2
L	L	H	H	$\overline{I}_3$	I_3
L	H	L	L	$\overline{I}_4$	I_4
L	H	L	H	$\overline{I}_5$	I_5
L	H	H	L	$\overline{I}_6$	I_6
L	H	H	H	$\overline{I}_7$	I_7

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter		54F/74F Min	54F/74F Typ	54F/74F Max	Units	Conditions	
I_{CC}	Power Supply Current	ON		15	22	mA	I_n, S_n = HIGH, $\overline{OE}$ = Gnd	V_{CC} = Max
		OFF		16	24		$\overline{OE}$, I_n = HIGH	

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF Min	Typ	Max	54F T_A, V_{CC} = Mil, C_L = 50 pF Min	Max	74F T_A, V_{CC} = Com, C_L = 50 pF Min	Max	Units	Fig. No.
t_{PLH}	Propagation Delay	3.5	6.0	9.0	3.5	11.5	3.5	9.5	ns	3-1
t_{PHL}	S_n to $\overline{Z}_n$	3.2	5.0	7.5	3.2	8.0	3.2	7.5		3-10
t_{PLH}	Propagation Delay	4.5	7.5	10.5	3.5	14.0	4.5	12.5	ns	3-1
t_{PHL}	S_n to Z_n	4.0	6.0	8.5	3.0	10.5	4.0	9.0		3-10
t_{PLH}	Propagation Delay	3.0	5.0	6.5	2.5	8.0	3.0	7.0	ns	3-1
t_{PHL}	I_n to $\overline{Z}$	1.5	2.5	4.0	1.5	6.0	1.5	5.0		3-3
t_{PLH}	Propagation Delay	3.5	5.0	7.0	2.5	9.0	2.5	8.0	ns	3-1
t_{PHL}	I_n to Z	3.5	5.5	7.0	3.5	9.0	3.5	7.5		3-4
t_{PZH}	Output Enable Time	2.5	4.3	6.0	2.0	7.0	2.5	7.0	ns	3-1
t_{PZL}	$\overline{OE}$ to $\overline{Z}$	2.5	4.3	6.0	2.5	7.5	2.5	6.5		3-12
t_{PHZ}	Output Disable Time	2.5	4.0	5.5	2.5	6.0	2.5	6.0		3-13
t_{PLZ}	$\overline{OE}$ to $\overline{Z}$	1.5	3.0	4.5	1.5	5.0	1.5	4.5		
t_{PZH}	Output Enable Time	3.5	5.0	7.0	3.0	8.5	3.0	7.5	ns	3-1
t_{PZL}	$\overline{OE}$ to Z	3.5	5.5	7.5	3.5	9.0	3.5	8.0		3-12
t_{PHZ}	Output Disable time	2.0	3.8	5.5	2.0	5.5	2.0	5.5		3-13
t_{PLZ}	$\overline{OE}$ to Z	1.5	3.0	4.5	1.5	5.5	1.5	4.5		

54F/74F253

Dual 4-Input Multiplexer With 3-State Outputs

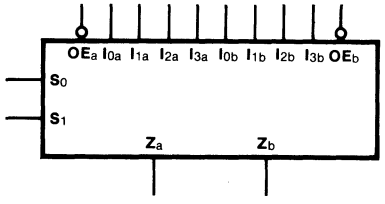
Description

The 'F253 is a dual 4-input multiplexer with 3-state outputs. It can select two bits of data from four sources using common select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output Enable ($\overline{OE}$) inputs, allowing the outputs to interface directly with bus oriented systems.

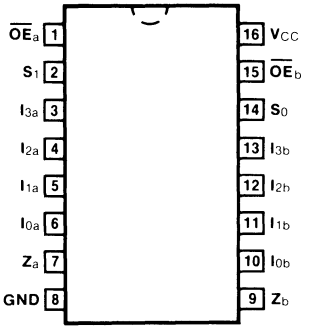
- **FAST Process for High Speed**
- **Multifunction Capability**
- **Non-Inverting 3-State Outputs**

Ordering Code: See Section 5

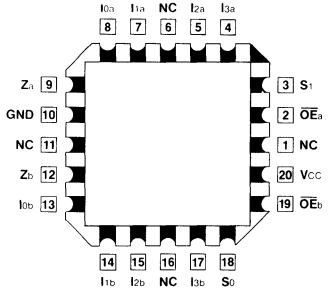
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
I_{0a}-I_{3a}	Side A Data Inputs	0.5/0.375
I_{0b}-I_{3b}	Side B Data Inputs	0.5/0.375
S_0, S_1	Common Select Inputs	0.5/0.375
$\overline{OE}_a$	Side A Output Enable Input (Active LOW)	0.5/0.375
$\overline{OE}_b$	Side B Output Enable Input (Active LOW)	0.5/0.375
Z_a, Z_b	3-State Outputs	75/15 (12.5)

Functional Description

This device contains two identical 4-input multiplexers with 3-state outputs. They select two bits from four sources selected by common Select inputs (S_0, S_1). The 4-input multiplexers have individual Output Enable ($\overline{OE}_a$, $\overline{OE}_b$) inputs which, when HIGH, force the outputs to a high impedance (High Z) state. This device is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two select inputs. The logic equations for the outputs are shown below:

$$Z_a = \overline{OE}_a \bullet (I_{0a} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1a} \bullet \overline{S}_1 \bullet S_0 + I_{2a} \bullet S_1 \bullet \overline{S}_0 + I_{3a} \bullet S_1 \bullet S_0)$$

$$Z_b = \overline{OE}_b \bullet (I_{0b} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1b} \bullet \overline{S}_1 \bullet S_0 + I_{2b} \bullet S_1 \bullet \overline{S}_0 + I_{3b} \bullet S_1 \bullet S_0)$$

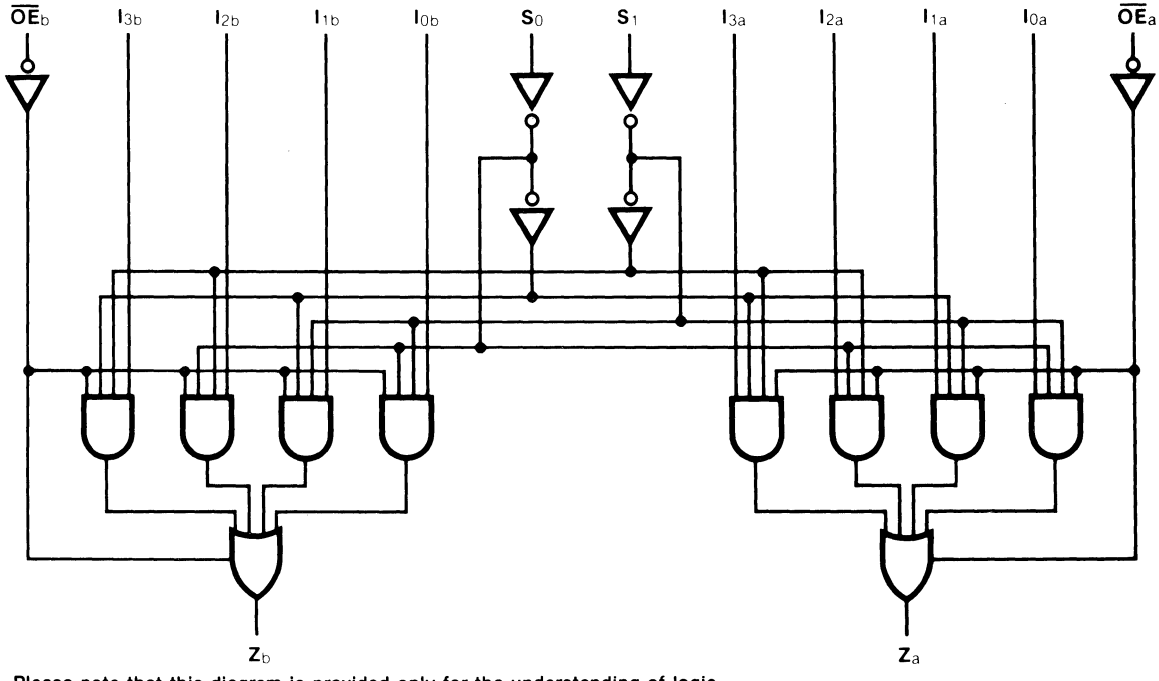
If the outputs of 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so that there is no overlap.

Truth Table

Select Inputs		Data Inputs				Output Enable	Output
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{OE}$	Z
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs S_0 and S_1 are common to both sections.
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CCH}	Power Supply Current		11.5	16.0	mA	V_{CC} = Max, $\overline{OE}_n$ = Gnd I_3, S_n = HIGH; I_0-I_2 = Gnd
I_{CCL}			16.0	23.0		V_{CC} = Max I_n, S_n, $\overline{OE}_n$ = Gnd
I_{CCZ}			16.0	23.0		V_{CC} = Max, $\overline{OE}_n$ = HIGH I_n, S_n = Gnd

4

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			54F T_A, V_{CC} = Mil C_L = 50 pF		74F T_A, V_{CC} = Com C_L = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay S_n to Z_n	4.5 3.0	8.5 6.5	11.5 9.0	3.5 2.5	15.0 11.0	4.5 3.0	13.0 10.0	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay I_n to Z_n	3.0 2.5	5.5 4.5	7.0 6.0	2.5 2.5	9.0 8.0	3.0 2.5	8.0 7.0	ns	3-1 3-4
t_{PZH} t_{PZL}	Output Enable Time	3.0 3.0	6.0 6.0	8.0 8.0	2.5 2.5	10.0 10.0	3.0 3.0	9.0 9.0	ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time	2.0 2.0	3.7 4.4	5.0 6.0	2.0 2.0	6.5 8.0	2.0 2.0	6.0 7.0		

54F/74F256

Dual 4-Bit Addressable Latch

Description

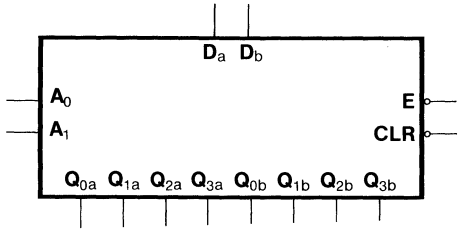
The 'F256 dual addressable latch has four distinct modes of operation which are selectable by controlling the Clear and Enable inputs (see Function Table). In the addressable latch mode, data at the Data (D) inputs is written into the addressed latches. The addressed latches will follow the Data input with all unaddressed latches remaining in their previous states.

In the memory mode, all latches remain in their previous states and are unaffected by the Data or Address inputs. To eliminate the possibility of entering erroneous data in the latches, the enable should be held HIGH (inactive) while the address lines are changing. In the dual 1-of-4 decoding or demultiplexing mode ($\overline{MR} = \overline{E} =$ LOW), addressed outputs will follow the level of the D inputs with all other outputs LOW. In the clear mode, all outputs are LOW and unaffected by the Address and Data inputs.

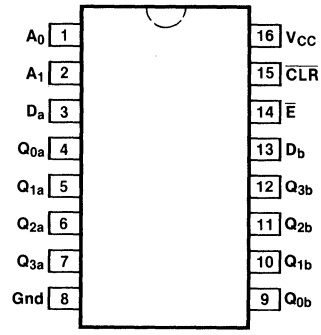
- **Combines Dual Demultiplexer and 8-Bit Latch**
- **Serial-to-Parallel Capability**
- **Output from Each Storage Bit Available**
- **Random (Addressable) Data Entry**
- **Easily Expandable**
- **Common Clear Input**
- **Useful as Dual 1-of-4 Active HIGH Decoder**

Ordering Code: See Section 5

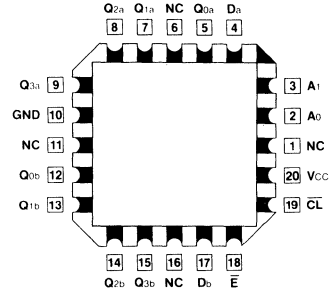
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

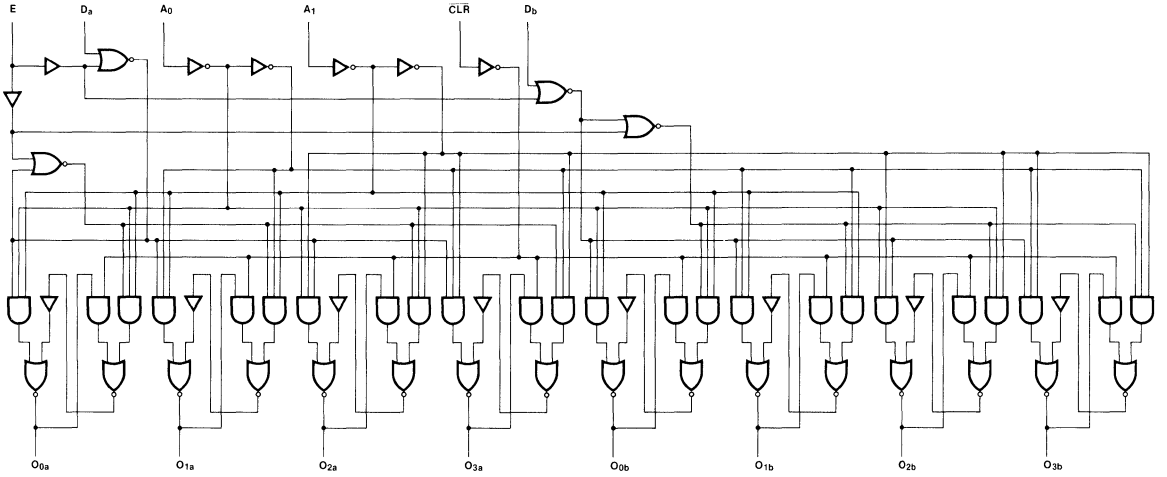
Pin Names	Description	54F/74F(U.L.) HIGH/LOW
D_a, D_b	Side A, Side B Data Inputs	0.5/0.375
A_0, A_1	Address Inputs	0.5/0.375
$\overline{E}$	Enable Input	1.0/0.75
$\overline{MR}$	Master Reset	0.5/0.375
Q_{0a}-Q_{3a}	Side A Outputs	25/12.5
Q_{0b}-Q_{3b}	Side B Outputs	25/12.5

Mode Select-Function Table

Operating Mode	Inputs					Outputs			
	$\overline{MR}$	$\overline{E}$	D	A_0	A_1	Q_0	Q_1	Q_2	Q_3
Master Reset	L	H	X	X	X	L	L	L	L
Demultiplex (Active HIGH Decoder when D = H)	L	L	d	L	L	Q = d	L	L	L
	L	L	d	H	L	L	Q = d	L	L
	L	L	d	L	H	L	L	Q = d	L
	L	L	d	H	H	L	L	L	Q = d
Store (Do Nothing)	H	H	X	X	X	q_0	q_1	q_2	q_3
Addressable Latch	H	L	d	L	L	Q = d	q_1	q_2	q_3
	H	L	d	H	L	q_0	Q = d	q_2	q_3
	H	L	d	L	H	q_0	q_1	Q = d	q_3
	H	L	d	H	H	q_0	q_1	q_2	Q = d

H = HIGH Voltage Level Steady State
L = LOW Voltage Level Steady State
X = Immaterial
d = HIGH or LOW Data one setup time prior to the LOW-to-HIGH Enable transition
q = Lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions	
		Min	Typ	Max			
I_{CCH}	Power Supply Current			40	mA	Output HIGH	V_{CC} = Max
I_{CCL}				60		Output LOW	

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Q_n		10.5 7.0						ns	3-1 3-8
t_{PLH} t_{PHL}	Propagation Delay D_n to Q_n		9.0 7.0						ns	3-1 3-3
t_{PLH} t_{PHL}	Propagation Delay A_n to Q_n		14.0 9.5						ns	3-1 3-10
t_{PHL}	Propagation Delay $\overline{CLR}$ to Q_n		9.0						ns	3-1 3-9

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW D_n to $\overline{E}$	4.0 4.0			ns	3-14
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D_n to $\overline{E}$	1.0 1.0				
$t_s(H)$ $t_s(L)$	Setup Time A to $\overline{E}$ [a]	4.0 4.0			ns	3-16
$t_h(H)$ $t_h(L)$	Hold Time A to $\overline{E}$[b]	0 0				
$t_w(H)$ $t_w(L)$	$\overline{E}$ Pulse Width HIGH or LOW	4.0 4.0			ns	3-8
$t_w(H)$ $t_w(L)$	$\overline{MR}$ Pulse Width HIGH or LOW	4.0 4.0			ns	3-9

a. The Address to Enable setup time is the time before the HIGH-to-LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.

b. The Address to Enable hold time is the time after the LOW-to-HIGH Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.

54F/74F257

Quad 2-Input Multiplexer With 3-State Outputs

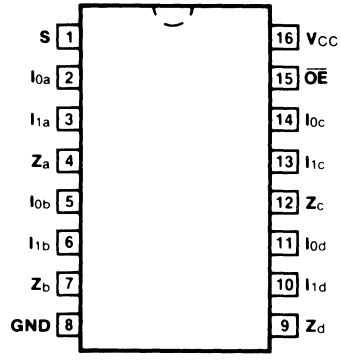
Description

The 'F257 is a quad 2-input multiplexer with 3-state outputs. Four bits of data from two sources can be selected using a Common Data Select input. The four outputs present the selected data in true (non-inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Output Enable ($\overline{OE}$) input, allowing the outputs to interface directly with bus-oriented systems.

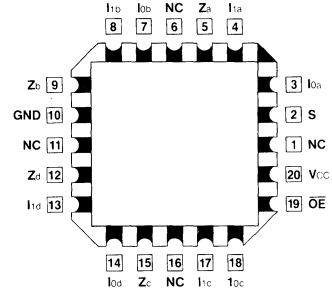
- **Multiplexer Expansion by Tying Outputs Together**
- **Non-Inverting 3-State Outputs**
- **Input Clamp Diodes Limit High-Speed Termination Effects**

Ordering Code: See Section 5

Connection Diagrams

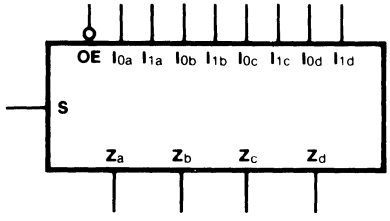


Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Logic Symbol



Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
S	Common Data Select Input	0.5/0.375
$\overline{OE}$	3-State Output Enable Input (Active LOW)	0.5/0.375
I_{0a}-I_{0d}	Data Inputs from Source 0	0.5/0.375
I_{1a}-I_{1d}	Data Inputs from Source 1	0.5/0.375
Z_a-Z_d	3-State Multiplexer Outputs	75/15 (12.5)

Functional Description

The 'F257 is a quad 2-input multiplexer with 3-state outputs. It selects four bits of data from two sources under control of a Common Data Select input. When the Select input is LOW, the I_{0x} inputs are selected and when Select is HIGH, the I_{1x} inputs are selected. The data on the selected inputs appears at the outputs in true (non-inverted) form. The device is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$Z_a = \overline{OE} \bullet (I_{1a} \bullet S + I_{0a} \bullet \overline{S})$$
$$Z_b = \overline{OE} \bullet (I_{1b} \bullet S + I_{0b} \bullet \overline{S})$$
$$Z_c = \overline{OE} \bullet (I_{1c} \bullet S + I_{0c} \bullet \overline{S})$$
$$Z_d = \overline{OE} \bullet (I_{1d} \bullet S + I_{0d} \bullet \overline{S})$$

When the Output Enable input ($\overline{OE}$) is HIGH, the outputs are forced to a high impedance OFF state. If the outputs are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure the Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

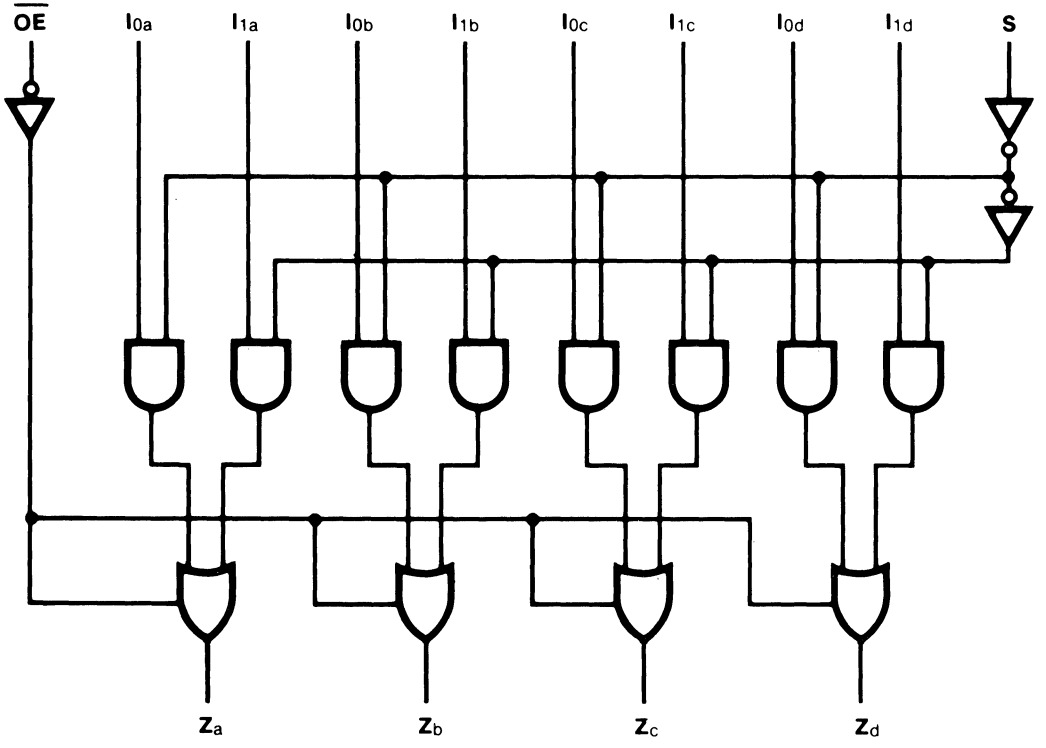
Truth Table

Output Enable	Select Input	Data Inputs		Output
$\overline{OE}$	S	I_0	I_1	Z
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

4

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter		54F/74F			Units	Conditions
			Min	Typ	Max		
I_{CCH}	Power Supply Current	HIGH		9.0	15	mA	V_{CC} = Max; S, I_{1X} = HIGH $\overline{OE}$, I_{0X} = Gnd
I_{CCL}		LOW		14.5	22		V_{CC} = Max; I_{1X} = HIGH $\overline{OE}$, I_{0X}, S = Gnd
I_{CCZ}		OFF		15	23		V_{CC} = Max; S, I_{0X} = Gnd $\overline{OE}$, I_{1X} = HIGH

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$			T_A, V_{CC} = Mil $C_L = 50\ pF$		T_A, V_{CC} = Com $C_L = 50\ pF$			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	3.0	4.5	6.0	3.0	8.0	3.0	7.0	ns	3-1
t_{PHL}	I_n to Z_n	2.0	4.2	5.5	1.5	8.0	2.0	6.5		3-4
t_{PLH}	Propagation Delay	4.5	10.1	13.0	4.5	15.5	4.5	15.0	ns	3-1
t_{PHL}	S to Z_n	3.5	6.5	8.5	3.5	10.5	3.5	9.5		3-10
t_{PZH}	Output Enable Time	3.0	5.9	7.5	3.0	9.5	3.0	8.5	ns	3-1
t_{PZL}		3.0	5.5	7.5	3.0	10.0	3.0	8.5		3-12
t_{PHZ}	Output Disable Time	2.0	4.3	6.0	2.0	7.0	2.0	7.0		3-13
t_{PLZ}		2.0	4.5	6.0	2.0	9.5	2.0	7.0		

54F/74F258

Quad 2-Input Multiplexer With 3-State Outputs

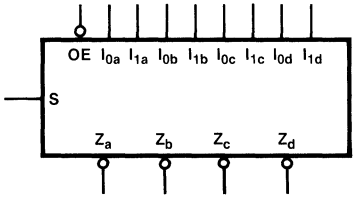
Description

The 'F258 is a quad 2-input multiplexer with 3-state outputs. Four bits of data from two sources can be selected using a common data select input. The four outputs present the selected data in the complement (inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Output Enable ($\overline{OE}$) input, allowing the outputs to interface directly with bus-oriented systems.

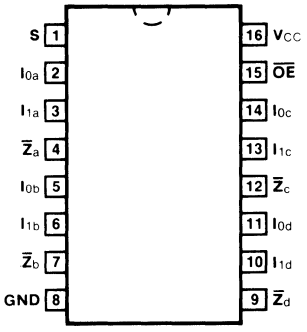
- **Multiplexer Expansion by Tying Outputs Together**
- **Inverting 3-State Outputs**

Ordering Code: See Section 5

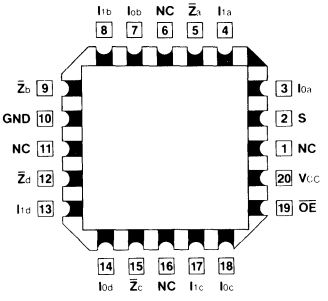
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
S	Common Data Select Input	0.5/0.375
$\overline{OE}$	3-State Output Enable Input (Active LOW)	0.5/0.375
I_{0a}-I_{0d}	Data Inputs from Source 0	0.5/0.375
I_{1a}-I_{1d}	Data Inputs from Source 1	0.5/0.375
$\overline{Z}_a$-$\overline{Z}_d$	3-State Inverting Data Outputs	75/15 (12.5)

Functional Description

The 'F258 is a quad 2-input multiplexer with 3-state outputs. It selects four bits of data from two sources under control of a common Select input (S). When the Select input is LOW, the I_{0x} inputs are selected and when Select is HIGH, the I_{1x} inputs are selected. The data on the selected inputs appears at the outputs in inverted form. The 'F258 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$\overline{Z}_a = \overline{OE} \bullet (I_{1a} \bullet S + I_{0a} \bullet \overline{S})$$
$$\overline{Z}_b = \overline{OE} \bullet (I_{1b} \bullet S + I_{0b} \bullet \overline{S})$$
$$\overline{Z}_c = \overline{OE} \bullet (I_{1c} \bullet S + I_{0c} \bullet \overline{S})$$
$$\overline{Z}_d = \overline{OE} \bullet (I_{1d} \bullet S + I_{0d} \bullet \overline{S})$$

When the Output Enable input ($\overline{OE}$) is HIGH, the outputs are forced to a high impedance OFF state. If the outputs of the 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

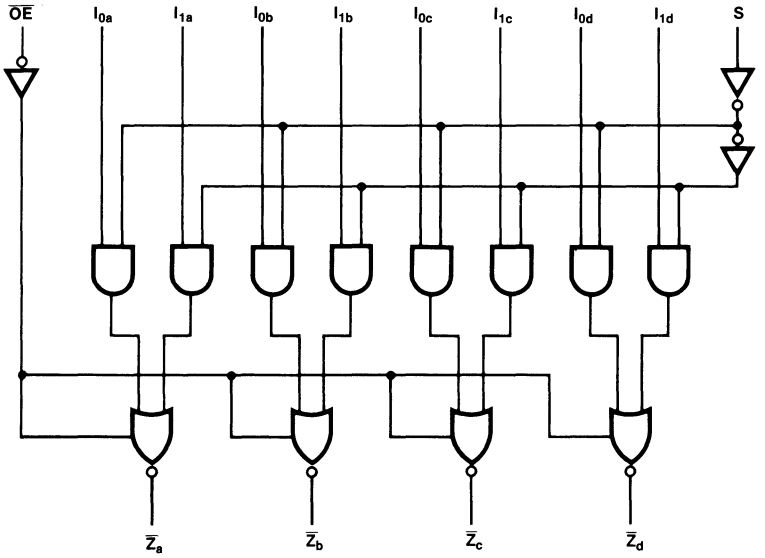
Truth Table

Output Enable	Select Input	Data Inputs		Outputs
$\overline{OE}$	S	I_0	I_1	$\overline{Z}$
H	X	X	X	Z
L	H	X	L	H
L	H	X	H	L
L	L	L	X	H
L	L	H	X	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

4

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CCH}	Power Supply Current		6.2	9.5	mA	V_{CC} = Max; I_{1X} = HIGH $\overline{OE}$, I_{0X}, S = Gnd
I_{CCL}			15.1	23		V_{CC} = Max; S, I_{1X} = HIGH $\overline{OE}$, I_{0X}, = Gnd
I_{CCZ}			11.3	17		V_{CC} = Max; S, I_{0X} = Gnd $\overline{OE}$, I_{1X} = HIGH

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			54F T_A, V_{CC} = Mil C_L = 50 pF		74F T_A, V_{CC} = Com C_L = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay I_n to $\overline{Z}_n$	1.5 1.5	4.0 3.5	5.3 4.7	1.5 1.5	7.5 6.0	1.5 1.5	6.0 5.5	ns	3-1 3-3
t_{PLH} t_{PHL}	Propagation Delay S to $\overline{Z}_n$	4.0 4.0	6.5 7.3	8.5 9.5	4.0 4.0	12.0 11.5	4.0 4.0	9.5 11.0	ns	3-1 3-10
t_{PZH} t_{PZL}	Output Enable Time	3.0 3.0	5.9 5.5	7.5 7.5	3.0 3.0	11.0 9.5	3.0 3.0	8.5 8.5	ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time	2.0 2.0	4.3 4.5	6.0 6.0	1.5 2.0	7.0 9.0	2.0 2.0	7.0 7.0		

54F/74F259

8-Bit Addressable Latch

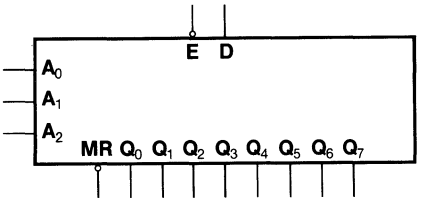
Description

The 'F259 is a high-speed 8-bit addressable latch designed for general purpose storage applications in digital systems. It is a multifunctional device capable of storing single line data in eight addressable latches, and also a 1-of-8 decoder and demultiplexer with active HIGH outputs. The device also incorporates an active LOW Common Clear for resetting all latches, as well as an active LOW Enable. It is functionally identical to the 9334 and 93L34 8-bit addressable latch.

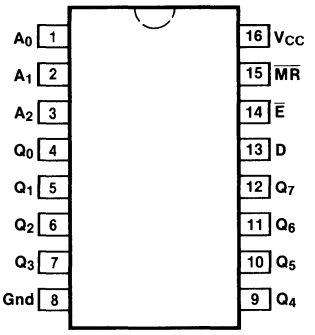
- **Serial-to-Parallel Conversion**
- **Eight Bits of Storage with Output of Each Bit Available**
- **Random (Addressable) Data Entry**
- **Active High Demultiplexing or Decoding Capability**
- **Easily Expandable**
- **Common Clear**

Ordering Code: See Section 5

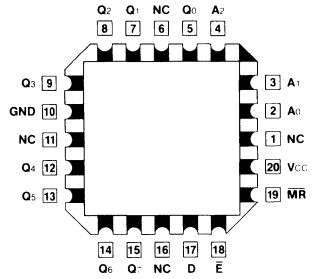
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC

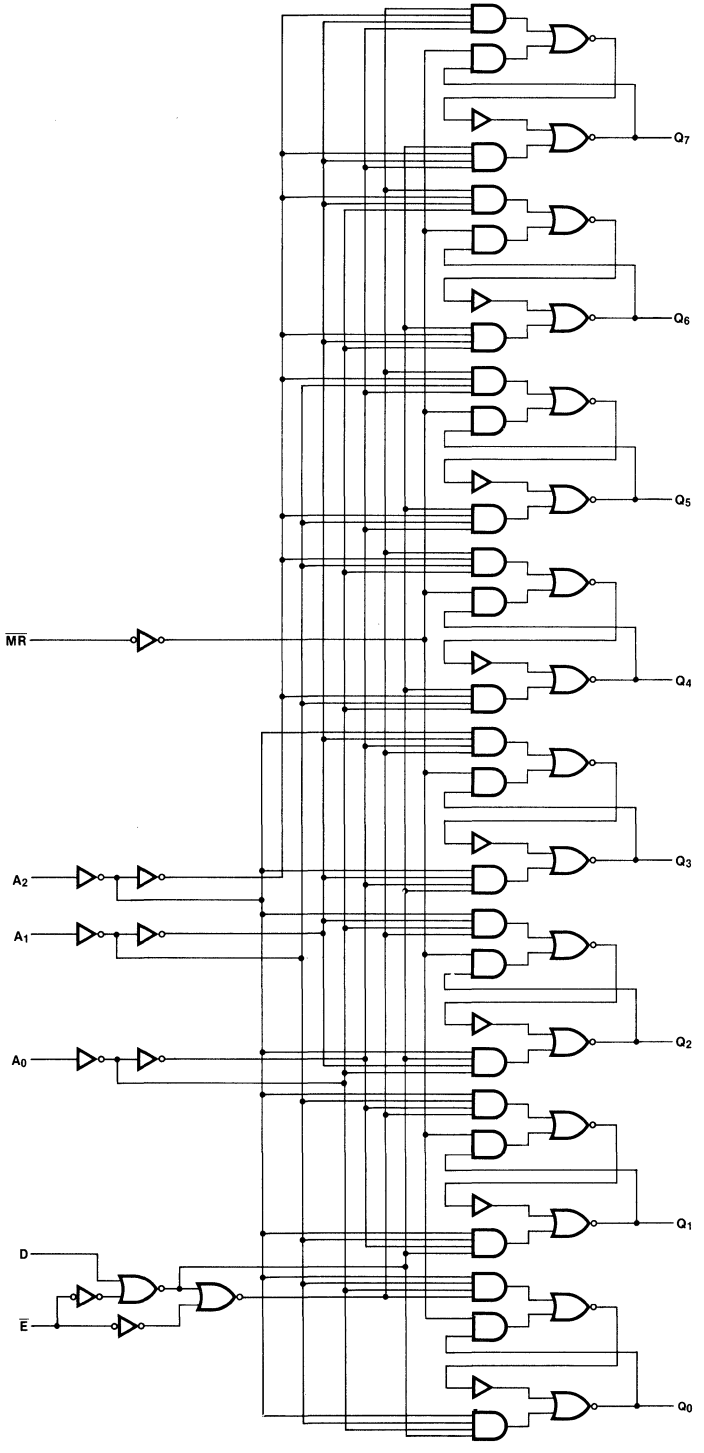


Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
A_0-A_2	Address Inputs	0.5/0.375
D	Data Input	0.5/0.375
$\overline{E}$	Enable Input (Active LOW)	1.0/0.75
$\overline{MR}$	Master Reset (Active LOW)	0.5/0.375
Q_0-Q_7	Latch Outputs	25/12.5

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Functional Description

The 'F259 has four modes of operation as shown in the Mode Selection Table. In the addressable latch mode, data on the Data line (D) is written into the addressed latch. The addressed latch will follow the data input with all non-addressed latches remaining in their previous states in the memory mode. All latches remain in their previous state and are unaffected by the Data or Address inputs.

In the one-of-eight decoding or demultiplexing mode, the addressed output will follow the state of the D input with all other outputs in the LOW state. In the clear mode all outputs are LOW and unaffected by the address and data inputs. When operating the 'F259 as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode. The Truth Table below summarizes the operations of the 'F259.

Mode Select-Function Table

Operating Mode	Inputs													
	$\overline{MR}$	$\overline{E}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7
Master Reset	L	H	X	X	X	X	L	L	L	L	L	L	L	L
Demultiplex (Active HIGH Decoder when D = H)	L	L	d	L	L	L	Q = d	L	L	L	L	L	L	L
	L	L	d	H	L	L	L	Q = d	L	L	L	L	L	L
	L	L	d	L	H	L	L	L	Q = d	L	L	L	L	L
	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	L	L	d	H	H	H	L	L	L	L	L	L	L	Q = d
Store (Do Nothing)	H	H	X	X	X	X	q_0	q_1	q_2	q_3	q_4	q_5	q_6	q_7
Addressable Latch	H	L	d	L	L	L	Q = d	q_1	q_2	q_3	q_4	q_5	q_6	q_7
	H	L	d	H	L	L	q_0	Q = d	q_2	q_3	q_4	q_5	q_6	q_7
	H	L	d	L	H	L	q_0	q_1	Q = d	q_3	q_4	q_5	q_6	q_7
	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	H	L	d	H	H	H	q_0	q_1	q_2	q_3	q_4	q_5	q_6	Q = d

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
d = HIGH or LOW data one setup time prior to the LOW-to-HIGH Enable transition.
q = Lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared.

Mode Select Table

$\overline{E}$	$\overline{MR}$	Mode
L	H	Addressable Latch
H	H	Memory
L	L	Active HIGH 8-Channel Demultiplexer
H	L	Clear

H = HIGH Voltage Level
L = LOW Voltage Level

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions	
		Min	Typ	Max			
I_{CCH}	Power Supply Current			40	mA	Output HIGH	V_{CC} = Max
I_{CCL}				75		Output LOW	

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Q_n		10.5 7.0						ns	3-1 3-8
t_{PLH} t_{PHL}	Propagation Delay D_n to Q_n		9.0 6.5						ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay A_n to Q_n		13.0 9.0						ns	3-1 3-10
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n		9.0						ns	3-1 3-11

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW D to $\overline{E}$	4.0 4.0			ns	3-14
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D to $\overline{E}$	1.0 1.0				
$t_s(L)$	Setup Time, LOW Address to Enable[a]	4.0			ns	3-16
$t_h(H)$	Hold Time, HIGH Address to Enable[b]	0				
$t_w(H)$ $t_w(L)$	$\overline{E}$ Pulse Width HIGH or LOW	4.0 4.0			ns	3-8
$t_w(H)$ $t_w(L)$	$\overline{MR}$ Pulse Width HIGH or LOW	4.0 4.0			ns	3-11

Notes

a. The Address to Enable setup time is the time before the HIGH-to-LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.

b. The Address to Enable hold time is the time after the LOW-to-HIGH Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.

54F/74F269

8-Bit Bidirectional Binary Counter

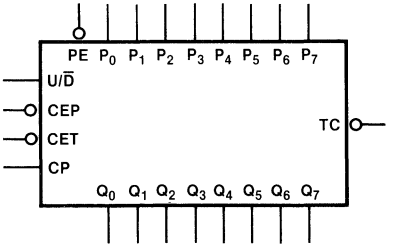
Description

The 'F269 is a fully synchronous 8-stage up/down counter featuring a preset capability for programmable operation, carry lookahead for easy cascading and a U/$\overline{D}$ input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the rising edge of the clock.

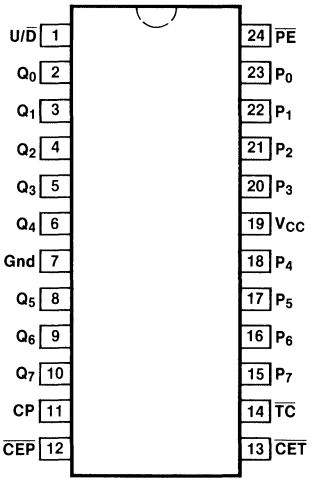
- **Synchronous Counting and Loading**
- **Built-in Lookahead Carry Capability**
- **Count Frequency 100 MHz Typ**
- **Supply Current 80 mA Typ**
- **300 mil Slimline Package**

Ordering Code: See Section 5

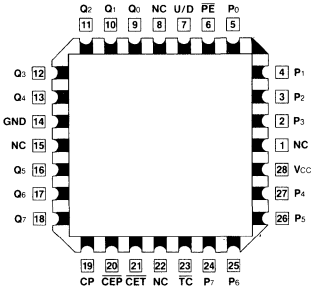
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC

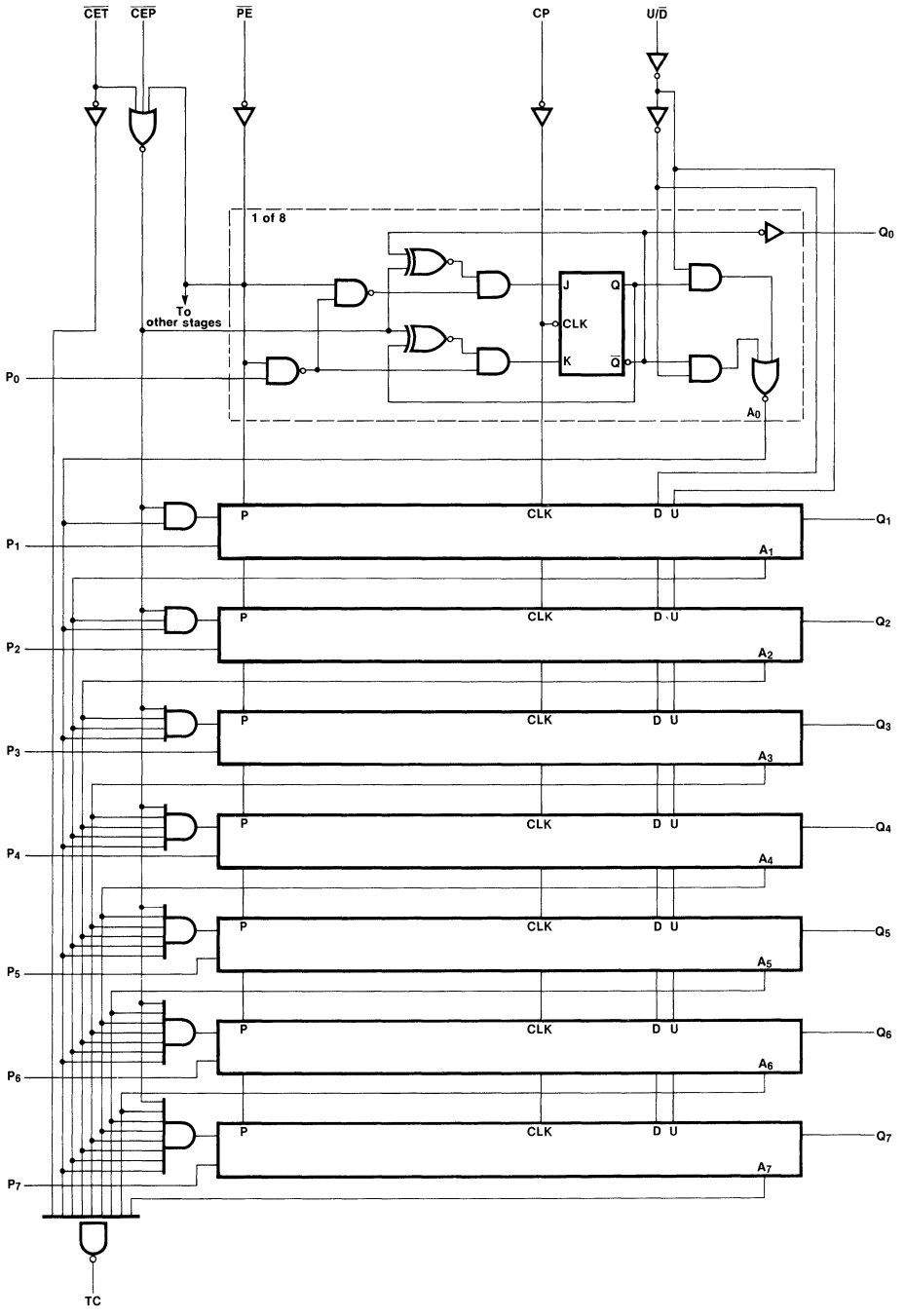


Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
P_0-P_7	Parallel Data Inputs	0.5/0.375
$\overline{PE}$	Parallel Enable Input (Active LOW)	0.5/0.375
U/$\overline{D}$	Up-Down Count Control Input	0.5/0.375
$\overline{CEP}$	Count Enable Parallel Input (Active LOW)	0.5/0.375
$\overline{CET}$	Count Enable Trickle Input (Active LOW)	0.5/0.375
CP	Clock Input	0.5/0.375
$\overline{TC}$	Terminal Count Output (Active LOW)	0.5/0.375
Q_0-Q_7	Flip-Flop Outputs	25/12.5

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Function Table

$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	U/$\overline{D}$	CP	Function
L	X	X	X	↑	Parallel Load all Flip-Flops
H	H	X	X	↑	Hold
H	X	H	X	↑	Hold ($\overline{TC}$ held HIGH)
H	L	L	H	↑	Count Up
H	L	L	L	↑	Count Down

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↑ = Transition LOW-to-HIGH

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions	
		Min	Typ	Max			
I_{CCH}	Power Supply Current		50	70	mA	Outputs HIGH	V_{CC} = Max
I_{CCL}			80	100		Outputs LOW	

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	80	100						MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n			10.0 10.0					ns	3-1 3-7
t_{PLH}	Propagation Delay U/$\overline{D}$ to $\overline{TC}$			15.0					ns	3-1 3-2
t_{PLH}	Propagation Delay $\overline{CET}$ to $\overline{TC}$			15.0					ns	3-1 3-2
t_{PHL}	Propagation Delay CP to $\overline{TC}$			15.0					ns	3-1 3-2

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW Data to CP	5.0 5.0			ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW Data to CP	0 0				
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{PE}$ to CP	12.0 12.0			ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{PE}$ to CP	0 0				
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{CET}$ or $\overline{CEP}$ to CP	10.0 10.0			ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{CET}$ or $\overline{CEP}$ to CP	0 0				
$t_w(H)$	Clock Pulse Width, HIGH	5.0			ns	3-7

54F/74F273

Octal D Flip-Flop

Description

The 'F273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

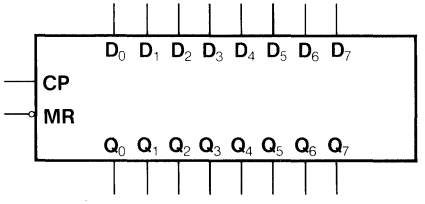
The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

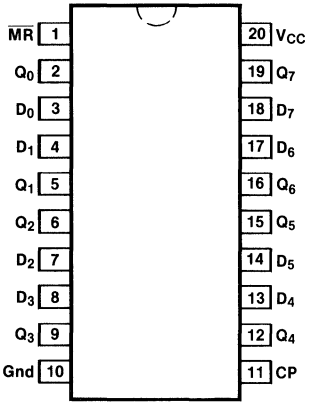
- **Ideal Buffer for MOS Microprocessor or Memory**
- **Eight Edge-Triggered D Flip-Flops**
- **Buffered Common Clock**
- **Buffered, Asynchronous Master Reset**
- **See 'F377 for Clock Enable Version**
- **See 'F377 for Transparent Latch Version**
- **See 'F374 for 3-State Version**

Ordering Code: See Section 5

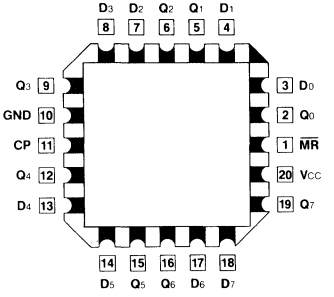
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

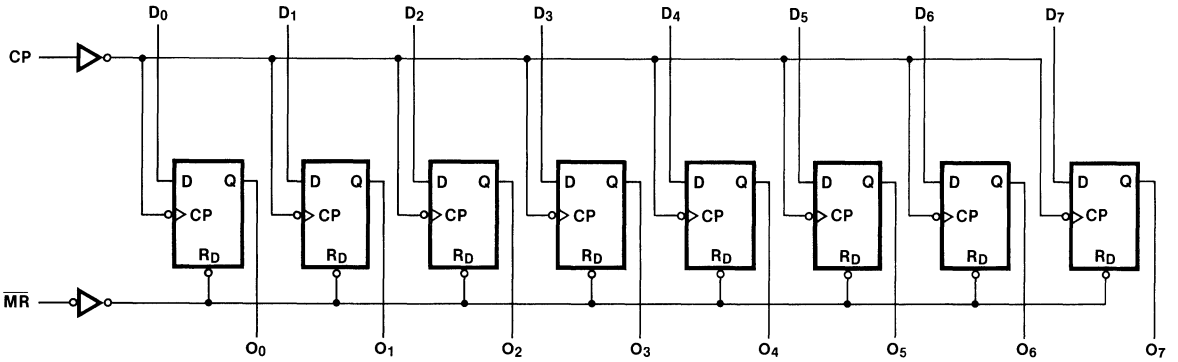
Pin Names	Description	54F/74F(U.L.) HIGH/LOW
D_0-D_7	Data Inputs	0.5/0.375
$\overline{MR}$	Master Reset (Active LOW)	0.5/0.375
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
Q_0-Q_7	Data Outputs	25/12.5

Mode Select-Function Table

Operating Mode	Inputs			Output
	$\overline{MR}$	CP	D_n	Q_n
Reset (Clear)	L	X	X	L
Load '1'	H	↑	h	H
Load '0'	H	↑	l	L

H = HIGH Voltage Level steady state
h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH clock transition
L = LOW Voltage Level steady state
l = LOW Voltage Level one setup time prior to the LOW-to-HIGH clock transition
X = Immaterial
↑ = LOW-to-HIGH clock transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		50	60	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$	T_A, V_{CC} = Mil $C_L = 50\ pF$	T_A, V_{CC} = Com $C_L = 50\ pF$		
		Min Typ Max	Min Max	Min Max		
f_{max}	Maximum Clock Frequency	100			MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay Clock to Output	10.0 11.0			ns	3-1 3-7
t_{PLH} t_{PHL}	Propagation Delay $\overline{MR}$ to Output	11.0 11.0			ns	3-1 3-11

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW Data to CP	3.0 3.0			ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW Data to CP	1.0 1.0				
$t_w(L)$	Clock Pulse Width, LOW	4.0			ns	3-7
$t_w(H)$ $t_w(L)$	$\overline{MR}$ Pulse Width HIGH or LOW	4.0 4.0			ns	3-11
t_{rec}	Recovery Time, $\overline{MR}$ to CP	3.0			ns	3-11

54F/74F280

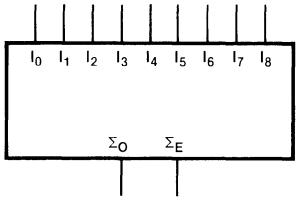
9-Bit Parity Generator/Checker

Description

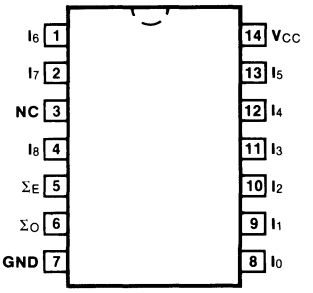
The 'F280 is a high-speed parity generator/checker that accepts nine bits of input data and detects whether an even or an odd number of these inputs is HIGH. If an even number of inputs is HIGH, the Sum Even output is HIGH. If an odd number is HIGH, the Sum Even output is LOW. The Sum Odd output is the complement of the Sum Even output.

Ordering Code: See Section 5

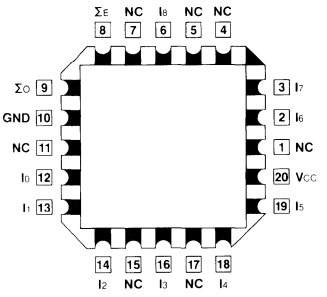
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

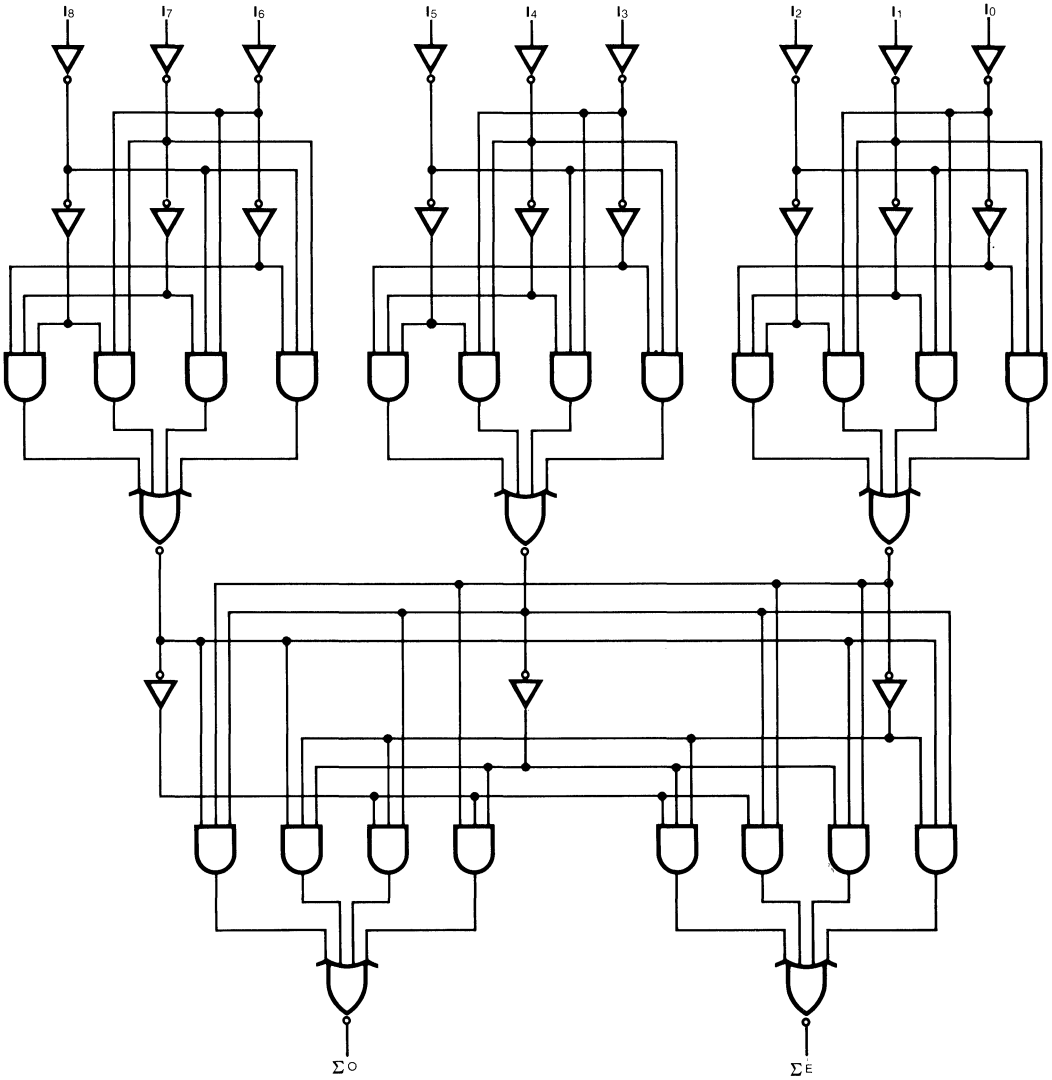
Pin Names	Description	54F/74F(U.L.) HIGH/LOW
I_0-I_8	Data Inputs	0.5/0.375
Σ_O	Odd Parity Output	25/12.5
Σ_E	Even Parity Output	25/12.5

Truth Table

Number of HIGH Inputs I_0-I_8	Outputs	
	Σ Even	Σ Odd
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

H = HIGH Voltage Level
L = LOW Voltage Level

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		25	38	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	6.5	10.0	15.0	6.5	20.0	6.5	16.0	ns	3-1
t_{PHL}	I_n to Σ_E	6.5	11.0	16.0	6.5	21.0	6.5	17.0		3-10
t_{PLH}	Propagation Delay	6.5	10.0	15.0	6.5	20.0	6.5	16.0	ns	3-1
t_{PHL}	I_n to Σ_O	6.5	11.0	16.0	6.5	21.0	6.5	17.0		3-10

54F/74F283

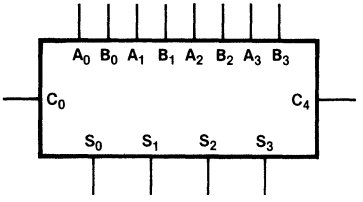
4-Bit Binary Full Adder With Fast Carry

Description

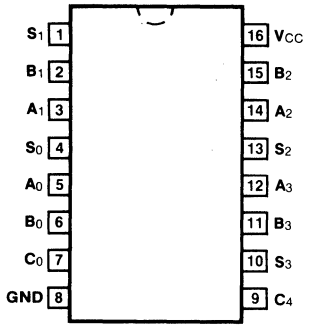
The 'F283 high-speed 4-bit binary full adder with internal carry lookahead accepts two 4-bit binary words (A_0-A_3, B_0-B_3) and a Carry input (C_0). It generates the binary Sum outputs (S_0-S_3) and the Carry output (C_4) from the most significant bit. The 'F283 will operate with either active HIGH or active LOW operands (positive or negative logic).

Ordering Code: See Section 5

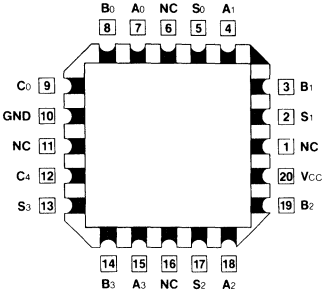
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
A_0-A_3	A Operand Inputs	0.5/0.75
B_0-B_3	B Operand Inputs	0.5/0.75
C_0	Carry Input	0.5/0.375
S_0-S_3	Sum Outputs	25/12.5
C_4	Carry Output	25/12.5

Functional Description

The 'F283 adds two 4-bit binary words (A plus B) plus the incoming Carry (C_0). The binary sum appears on the Sum (S_0-S_3) and outgoing carry (C_4) outputs. The binary weight of the various inputs and outputs is indicated by the subscript numbers, representing powers of two.

$$2^0(A_0 + B_0 + C_0) + 2^1(A_1 + B_1) + 2^2(A_2 + B_2) + 2^3(A_3 + B_3)$$

$$= S_0 + 2S_1 + 4S_2 + 8S_3 + 16C_4$$

Where (+) = plus

Interchanging inputs of equal weight does not affect the operation. Thus C_0, A_0, B_0 can be arbitrarily assigned to pins 5, 6 and 7 for DIPS, and 7, 8 and 9 for chip carrier packages. Due to the symmetry of the binary add function, the 'F283 can be used either with all inputs and outputs active HIGH (positive logic) or with all inputs and outputs active LOW (negative logic). See Figure a. Note that if C_0 is not used it must be tied LOW for active HIGH logic or tied HIGH for active LOW logic.

Due to pin limitations, the intermediate carries of the 'F283 are not brought out for use as inputs or outputs. However, other means can be used to effectively insert a carry into, or bring a carry out from, an intermediate stage. Figure b shows how to make a 3-bit adder. Tying the operand inputs of the fourth adder (A_3, B_3) LOW makes S_3 dependent only on, and equal to, the carry from the third adder. Using somewhat the same principle, Figure c shows a way of dividing the 'F283 into a 2-bit and a 1-bit adder. The third stage adder (A_2, B_2, S_2) is used merely as a means of getting a carry (C_{10}) signal into the fourth stage (via A_2 and B_2) and bringing out the carry from the second stage on S_2. Note that as long as A_2 and B_2 are the same, whether HIGH or LOW, they do not influence S_2. Similarly, when A_2 and B_2 are the same the carry into the third stage does not influence the carry out of the third stage. Figure D shows a method of implementing a 5-input encoder, where the inputs are equally weighted. The outputs S_0, S_1 and S_2 present a binary number equal to the number of inputs I_1-I_5 that are true. Figure e shows one method of implementing a 5-input majority gate. When three or more of the inputs I_1-I_5 are true, the output M_5 is true.

Fig. a Active HIGH versus Active LOW Interpretation

	C_0	A_0	A_1	A_2	A_3	B_0	B_1	B_2	B_3	S_0	S_1	S_2	S_3	C_4
Logic Levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0

Active HIGH: 0 + 10 + 9 = 3 + 16 Active LOW: 1 + 5 + 6 = 12 + 0

Fig. b 3-Bit Adder

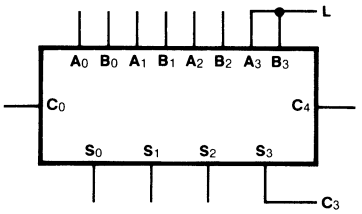


Fig. c 2-Bit and 1-Bit Adders

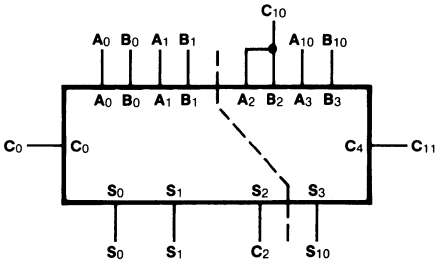


Fig. d 5-Input Encoder

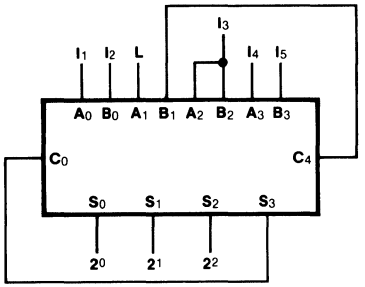
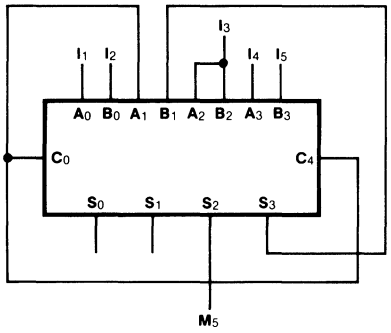
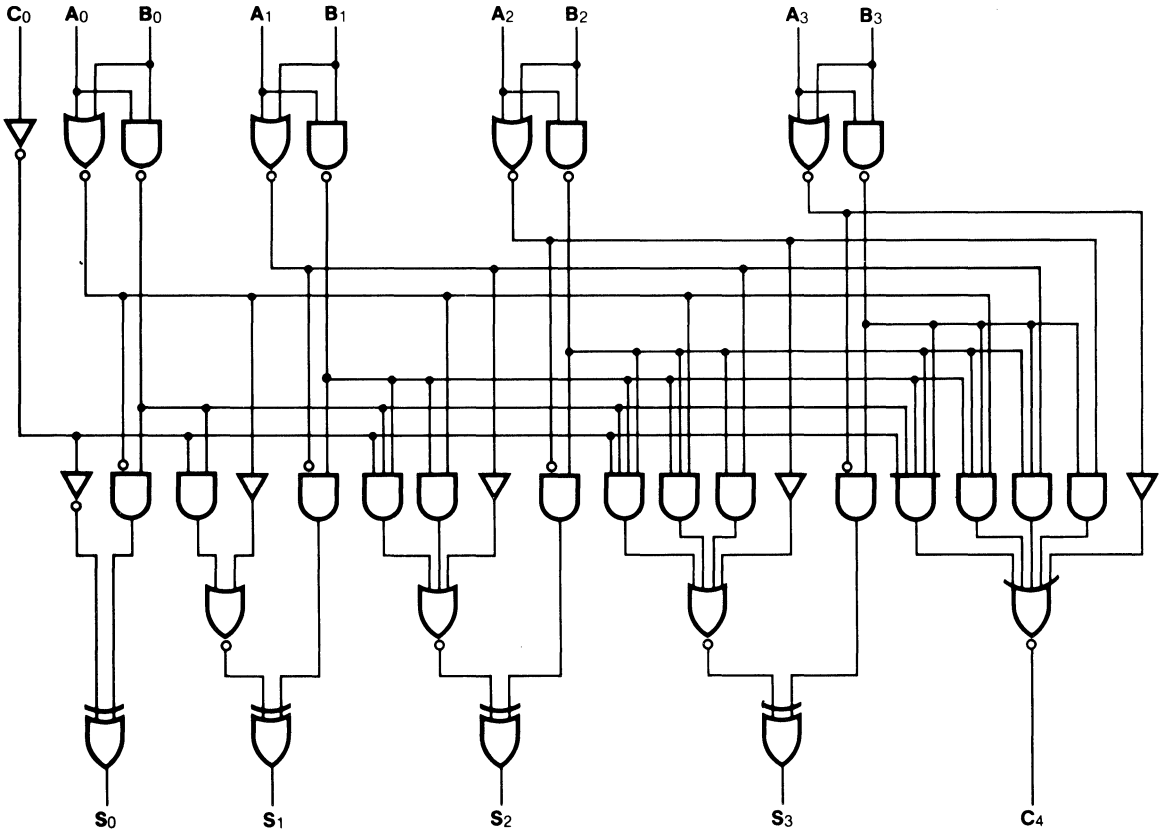


Fig. e 5-Input Majority Gate



Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		36	55	mA	V_{CC} = Max Inputs = HIGH

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			54F T_A, V_{CC} = Mil C_L = 50 pF		74F T_A, V_{CC} = Com C_L = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay C_0 to S_n	3.5 4.0	7.0 7.0	9.5 9.5	3.5 4.0	14.0 14.0	3.5 4.0	10.5 10.5	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay A_n or B_n to S_n	4.0 3.5	7.0 7.0	9.5 9.5	4.0 3.5	14.0 14.0	4.0 3.5	10.5 10.5	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay C_0 to C_4	3.5 3.0	5.7 5.4	7.5 7.0	3.5 3.0	10.5 10.0	3.5 3.0	8.5 8.0	ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay A_n or B_n to C_4	3.5 3.0	5.7 5.3	7.5 7.0	3.5 3.0	10.5 10.0	3.5 3.0	8.5 8.0	ns	3-1 3-4

54F/74F298

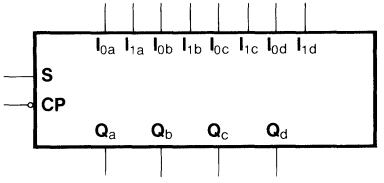
Quad 2-Input Multiplexer With Storage

Description

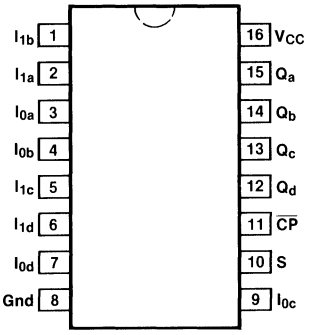
This device is a high-speed multiplexer with storage. It selects four bits of data from two sources (Ports) under the control of a common Select input (S). The selected data is transferred to the 4-bit output register synchronous with the HIGH-to-LOW transition of the Clock input ($\overline{CP}$). The 4-bit register is fully edge triggered. The Data inputs (I_0 and I_1) and Select input (S) must be stable only one setup time prior to the HIGH-to-LOW transition of the clock for predictable operation.

Ordering Code: See Section 5

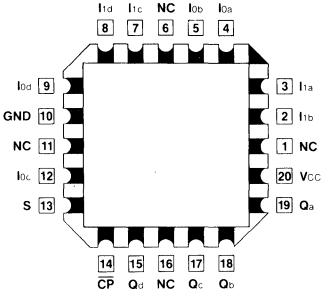
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC

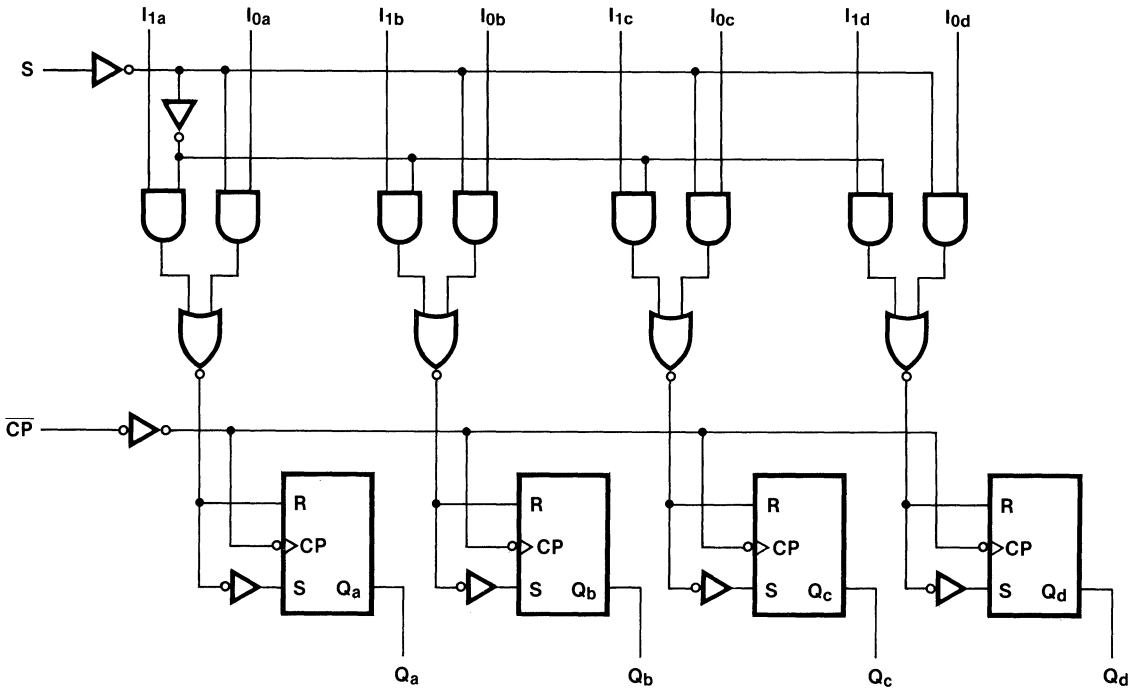


Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
I_{1a}-I_{1d}	Source 1 Data Inputs	0.5/0.375
I_{0a}-I_{0d}	Source 0 Data Inputs	0.5/0.375
S	Select Input	0.5/0.375
$\overline{CP}$	Clock Pulse Input (Active Falling Edge)	0.5/0.375
Q_a-Q_d	Outputs	25/12.5

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		31	46	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$	T_A, V_{CC} = Mil $C_L = 50\ pF$	T_A, V_{CC} = Com $C_L = 50\ pF$		
		Min Typ Max	Min Max	Min Max		
f_{max}	Maximum Clock Frequency	105			MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay CP to Q	7.0 7.0			ns	3-1 3-8

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW D to $\overline{CP}$	4.0 4.0			ns	3-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D to $\overline{CP}$	0 0				
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW S to $\overline{CP}$	8.0 8.0			ns	3-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW S to $\overline{CP}$	0 0				
$t_w(H)$ $t_w(L)$	$\overline{CP}$ Pulse Width HIGH or LOW	5.0 5.0			ns	3-8

54F/74F299

8-Input Universal Shift/Storage Register With Common Parallel I/O Pins

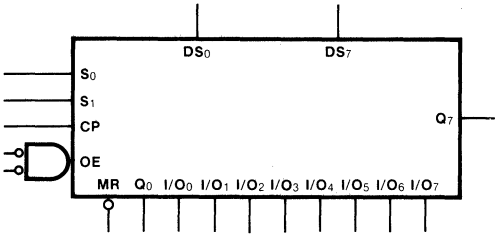
Description

The 'F299 is an 8-bit universal shift/storage register with 3-state outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Additional outputs are provided for flip-flops Q_0-Q_7 to allow easy serial cascading. A separate active LOW Master Reset is used to reset the register.

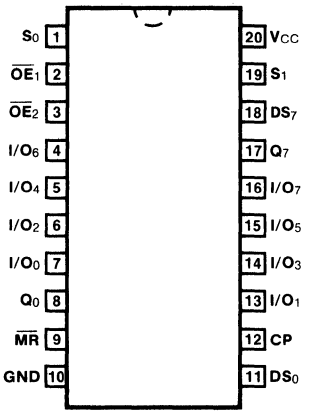
- **Common Parallel I/O for Reduced Pin Count**
- **Additional Serial Inputs and Outputs for Expansion**
- **Four Operating Modes: Shift Left, Shift Right, Load and Store**
- **3-State Outputs for Bus-Oriented Applications**

Ordering Code: See Section 5

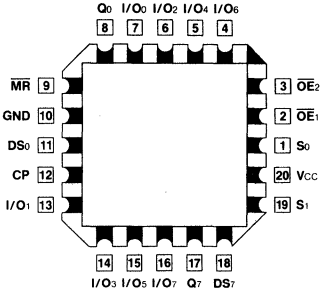
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC

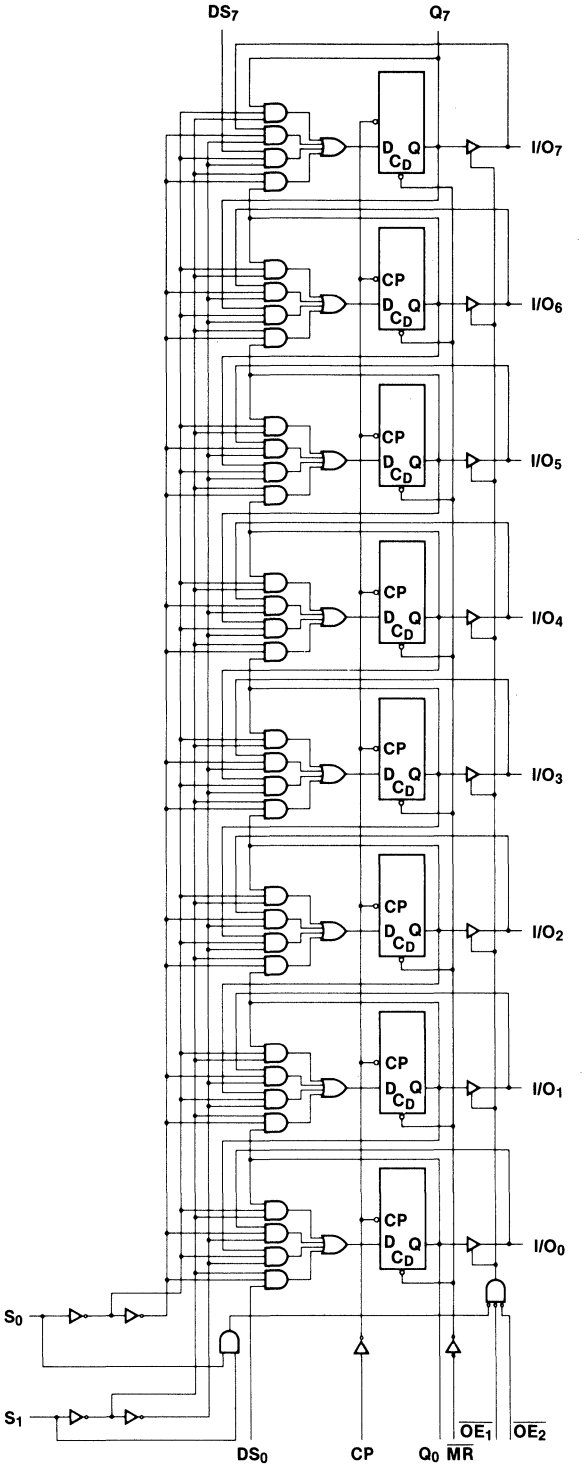


Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
DS_0	Serial Data Input for Right Shift	0.5/0.375
DS_7	Serial Data Input for Left Shift	0.5/0.375
S_0, S_1	Mode Select Inputs	0.5/0.75
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)	0.5/0.375
$\overline{OE}_1$, $\overline{OE}_2$	3-State Output Enable Inputs (Active LOW)	0.5/0.375
I/O_0-I/O_7	Parallel Data Inputs or	1.75/0.406
	3-State Parallel Outputs	75/15 (12.5)
Q_0, Q_7	Serial Outputs	25/12.5

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Functional Description

The 'F299 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous shift left, shift right, parallel load and hold operations. The type of operation is determined by S_0 and S_1, as shown in the Mode Select Table. All flip-flop outputs are brought out through 3-state buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q_0 and Q_7 are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on $\overline{MR}$ overrides the Select and CP inputs and resets the flip-flops. All other state changes are initiated by the rising edge of the clock. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP, are observed.

A HIGH signal on either $\overline{OE}_1$ or $\overline{OE}_2$ disables the 3-state buffers and puts the I/O pins in the high impedance state. In this condition the shift, hold, load and reset operations can still occur. The 3-state buffers are also disabled by HIGH signals on both S_0 and S_1 in preparation for a parallel load operation.

Mode Select Table

Inputs				Response
$\overline{MR}$	S_1	S_0	CP	
L	X	X	X	Asynchronous Reset; Q_0-Q_7 = LOW
H	H	H	⎍	Parallel Load; $I/O_n \rightarrow Q_n$
H	L	H	⎍	Shift Right; $DS_0 \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.
H	H	L	⎍	Shift Left; $DS_7 \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
H	L	L	X	Hold

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	70F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		68	95	mA	V_{CC} = Max, $\overline{OE}$ = HIGH CP = HIGH

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			54F T_A, V_{CC} = Mil C_L = 50 pF		74F T_A, V_{CC} = Com C_L = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Input Frequency	70	100				70		MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay CP to Q_0 or Q_7	4.0 3.5	7.0 6.5	9.0 8.5			4.0 3.5	10.0 9.5	ns	3-1, 3-7
t_{PLH} t_{PHL}	Propagation Delay CP to I/O_n	4.0 5.0	7.0 8.5	9.0 11.0			4.0 5.0	10.0 12.0		
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_0 or Q_7	4.5	7.5	9.5			4.5	10.5	ns	3-1, 3-11
t_{PHL}	Propagation Delay $\overline{MR}$ to I/O_n	6.5	11.0	14.0			6.5	15.0		
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to I/O_n	3.5 4.0	6.0 7.0	8.0 10.0			3.5 4.0	9.0 11.0	ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to I/O_n	2.5 2.0	4.5 4.0	6.0 5.5			2.5 2.0	7.0 6.5		

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW S_0 or S_1 to CP	8.5 8.5		8.5 8.5	ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW S_0 or S_1 to CP	0 0		0 0		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW I/O_n, DS_0 or DS_7 to CP	5.5 5.5		5.5 5.5	ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW I/O_n, DS_0 or DS_7 to CP	2.0 2.0		2.0 2.0		
$t_w(H)$ $t_w(L)$	CP Pulse Width HIGH or LOW	7.0 7.0		7.0 7.0	ns	3-7
$t_w(L)$	$\overline{MR}$ Pulse Width, LOW	7.0		7.0	ns	3-11
t_{rec}	Recovery Time, $\overline{MR}$ to CP	7.0		7.0	ns	3-11

54F/74F322

8-Bit Serial/Parallel Register With Sign Extend

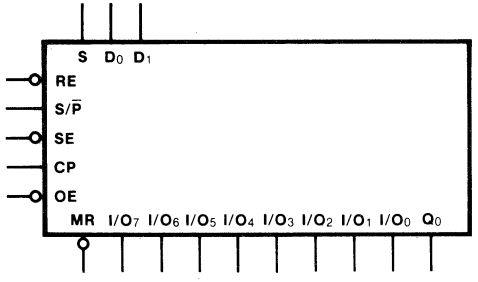
Description

The 'F322 is an 8-bit shift register with provision for either serial or parallel loading and with 3-state parallel outputs plus a bi-state serial output. Parallel data inputs and parallel outputs are multiplexed to minimize pin count. State changes are initiated by the rising edge of the clock. Four synchronous modes of operation are possible: hold (store), shift right with serial entry, shift right with sign extend and parallel load. An asynchronous Master Reset ($\overline{MR}$) input overrides clocked operation and clears the register.

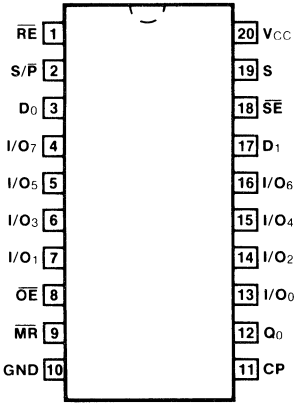
- **Multiplexed Parallel I/O Ports**
- **Separate Serial Input and Output**
- **Sign Extend Function**
- **3-State Outputs for Bus Applications**

Ordering Code: See Section 5

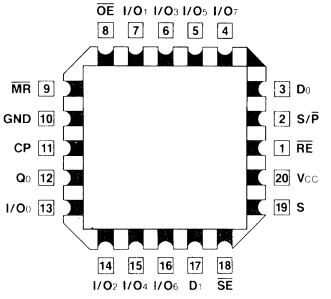
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
$\overline{RE}$	Register Enable Input (Active LOW)	0.5/0.375
$S/\overline{P}$	Serial (HIGH) or Parallel (LOW) Mode Control Input	0.5/0.375
$\overline{SE}$	Sign Extend Input (Active LOW)	0.5/1.125
S	Serial Data Select Input	0.5/0.75
D_0, D_1	Serial Data Inputs	0.5/0.375
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)	0.5/0.375
$\overline{OE}$	3-State Output Enable Input (Active LOW)	0.5/0.375
Q_0	Bi-state Serial Output	25/12.5
I/O_0-I/O_7	Multiplexed Parallel Data Inputs or 3-State Parallel Data Outputs	1.75/0.406 25/12.5

Functional Description

The 'F322 contains eight D-type edge triggered flip-flops and the interstage gating required to perform right shift and the intrastage gating necessary for hold and synchronous parallel load operations. A LOW signal on $\overline{RE}$ enables shifting or parallel loading, while a HIGH signal enables the hold mode. A HIGH signal on S/$\overline{P}$ enables shift right, while a LOW signal disables the 3-state output buffers and enables parallel loading. In the shift right mode a HIGH signal on $\overline{SE}$ enables serial entry from either D_0 or D_1, as determined by the S input. A LOW signal on $\overline{SE}$ enables shift right but Q_7 reloads its contents, thus performing the sign extend function required for the 'F384 Twos Complement Multiplier. A HIGH signal on $\overline{OE}$ disables the 3-state output buffers, regardless of the other control inputs. In this condition the shifting and loading operations can still be performed.

Mode Select Table

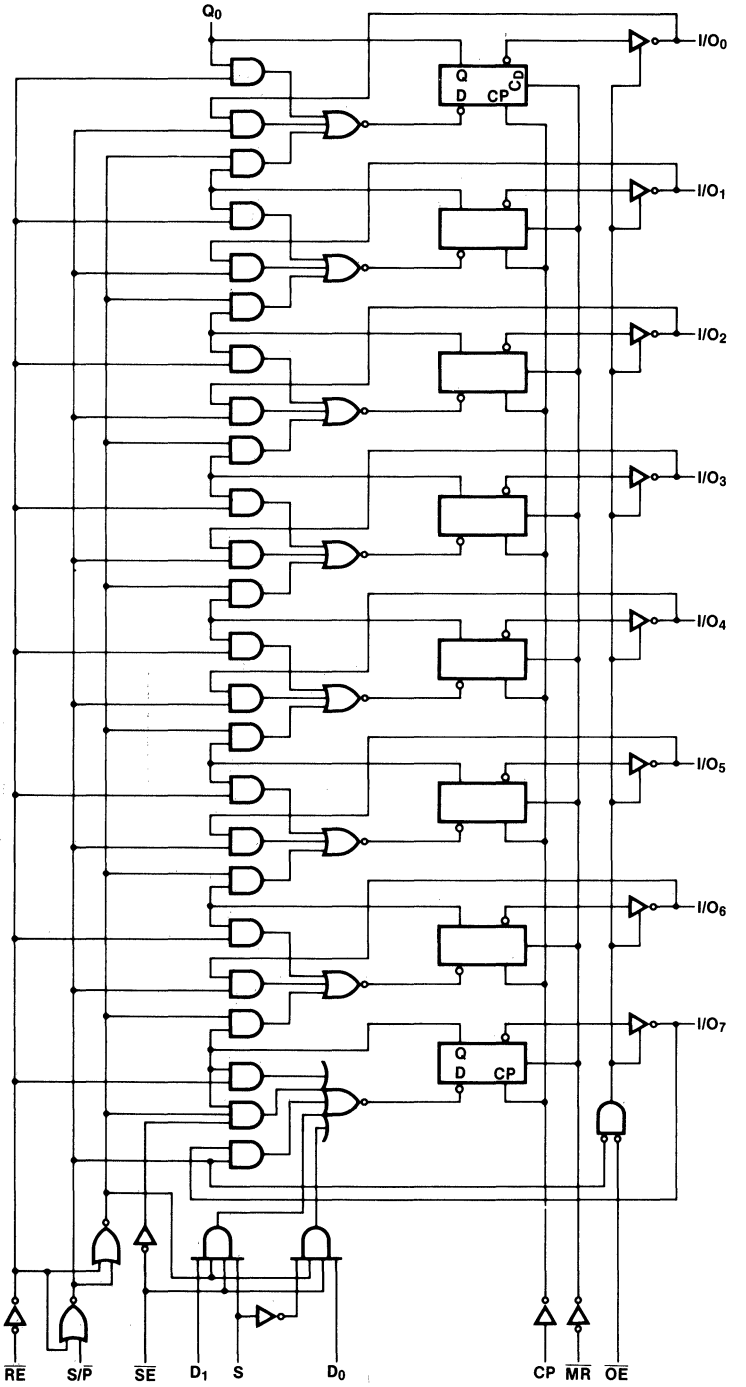
Mode	Inputs							Outputs								
	$\overline{MR}$	$\overline{RE}$	S/$\overline{P}$	$\overline{SE}$	S	$\overline{OE}$*	CP	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0	Q_0
Clear	L	X	X	X	X	L	X	L	L	L	L	L	L	L	L	L
	L	X	X	X	X	H	Z	Z	Z	Z	Z	Z	Z	Z	Z	L
Parallel Load	H	L	L	X	X	X	↑	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	I_0
Shift Right	H	L	H	H	L	L	↑	D_0	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_1
	H	L	H	H	H	L	↑	D_1	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_1
Sign Extend	H	L	H	L	X	L	↑	O_7	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_1
Hold	H	H	X	X	X	L	↑	NC	NC	NC	NC	NC	NC	NC	NC	NC

*When the $\overline{OE}$ input is HIGH all I/O_n terminals are at the high impedance state; sequential operation or clearing of the register is not affected.

1. I_7-I_0 = The level of the steady-state input at the respective I/O terminal is loaded into the flip-flop while the flip-flop outputs (except Q_0) are isolated from the I/O terminal.
2. D_0, D_1 = The level of the steady-state inputs to the serial multiplexer input.
3. O_7-O_0 = The level of the respective Q_n flip-flop prior to the last Clock LOW-to-HIGH transition.

H = HIGH Voltage Level
L = LOW Voltage Level
Z = High Impedance Output State
↑ = LOW-to-HIGH Transition
NC = No Change

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		60	90	mA	V_{CC} = Max, CP = HIGH Output Disabled

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			54F T_A, V_{CC} = Mil C_L = 50 pF		74F T_A, V_{CC} = Com C_L = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	70	90		50		70		MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay CP to I/O_n	3.5 4.0	5.5 6.0	7.5 8.0	3.0 3.5	9.5 10.0	3.5 3.5	8.5 9.0	ns	3-1, 3-7
t_{PLH} t_{PHL}	Propagation Delay CP to Q_0	3.5 3.5	7.0 6.0	9.0 8.0	3.5 3.5	11.0 10.0	3.5 3.5	10.0 9.0		
t_{PHL}	Propagation Delay $\overline{MR}$ to I/O_n	6.0	10.0	13.0	6.0	15.0	6.0	14.0	ns	3-1 3-11
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_0	5.5	9.5	12.0	5.5	14.0	5.5	13.0	ns	3-1 3-11
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to I/O_n	3.0 4.0	6.5 8.5	9.0 11.0	3.0 4.0	12.5 14.5	3.0 4.0	10.0 12.0	ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to I/O_n	2.0 2.0	4.5 5.0	6.0 7.0	2.0 2.0	8.0 10.0	2.0 2.0	7.0 8.0		
t_{PZH} t_{PZL}	Output Enable Time S/$\overline{P}$ to I/O_n	4.5 5.5	8.0 10.0	10.5 14.0	4.5 5.5	13.5 17.0	4.5 5.5	11.5 15.0	ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time S/$\overline{P}$ to I/O_n	5.0 6.0	9.0 12.0	11.5 15.5	5.0 6.0	16.5 19.5	5.0 6.0	12.5 16.5		

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F		54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\,V$		T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ	Max	Min Max	Min Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{RE}$ to CP	6.0 14.0		8.0 18.0	7.0 16.0	ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{RE}$ to CP	0 0		0 0	0 0	ns	3-5
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW D_0, D_1 or I/O_n to CP	6.5 6.5		8.5 8.5	7.5 7.5	ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D_0, D_1 or I/O_n to CP	2.0 2.0		3.0 3.0	3.0 3.0	ns	3-5
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{SE}$ to CP	7.0 2.5		9.0 4.5	8.0 3.5	ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{SE}$ to CP	2.0 0		2.0 0	2.0 0	ns	3-5
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW S/$\overline{P}$ to CP	11.0 13.5		13.0 21.0	12.0 15.5	ns	3-5
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW S to CP	6.5 9.0		8.5 11.0	7.5 10.0	ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW S or S/$\overline{P}$ to CP	0 0		0 0	0 0	ns	3-5
$t_w(H)$	CP Pulse Width, HIGH	7.0		8.0	7.0	ns	3-7
$t_w(L)$	$\overline{MR}$ Pulse Width, LOW	5.5		7.5	6.5	ns	3-11
t_{rec}	Recovery Time $\overline{MR}$ to CP	8.0		9.5	8.0	ns	3-11

54F/74F323

8-Bit Universal Shift/Storage Register With Synchronous Reset and Common I/O Pins

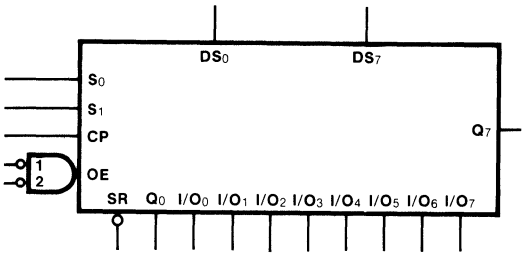
Description

The 'F323 is an 8-bit universal shift/storage register with 3-state outputs. Its function is similar to the 'F299 with the exception of Synchronous Reset. Parallel load inputs and flip-flop outputs are multiplexed to minimize pin count. Separate serial inputs and outputs are provided for Q_0 and Q_7 to allow easy cascading. Four operation modes are possible: hold (store), shift left, shift right and parallel load.

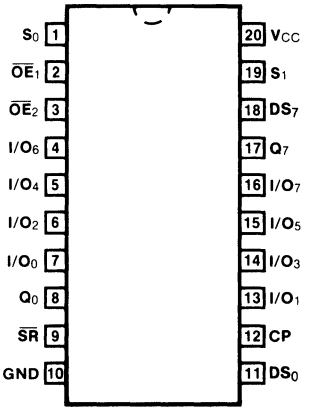
- **Common Parallel I/O for Reduced Pin Count**
- **Additional Serial Inputs and Outputs for Expansion**
- **Four Operating Modes: Shift Left, Shift Right, Load and Store**
- **3-State Outputs for Bus-Oriented Applications**

Ordering Code: See Section 5

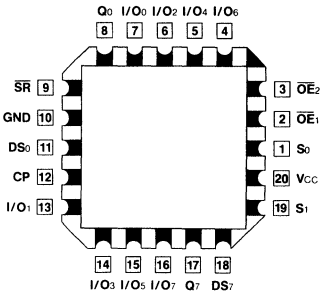
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC

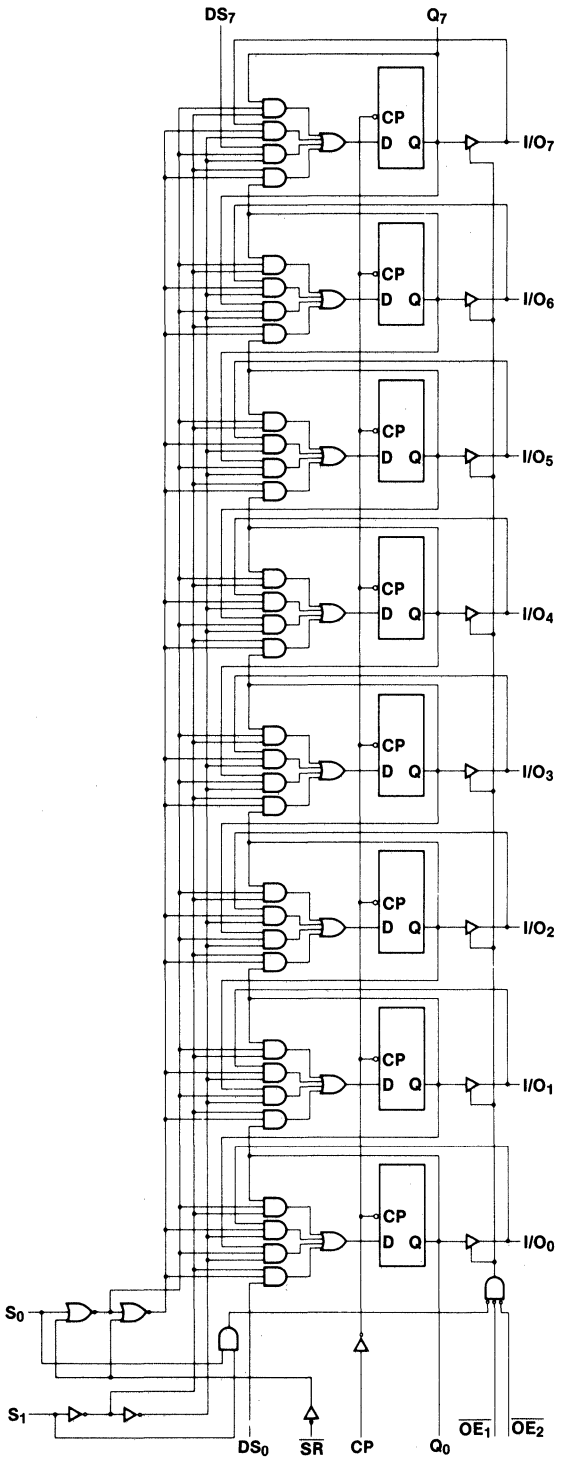


Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
DS_0	Serial Data Input for Right Shift	0.5/0.375
DS_7	Serial Data Input for Left Shift	0.5/0.375
S_0, S_1	Mode Select Inputs	0.5/0.75
$\overline{SR}$	Synchronous Reset Input (Active LOW)	0.5/0.375
$\overline{OE}_1$, $\overline{OE}_2$	3-State Output Enable Inputs (Active LOW)	0.5/0.375
I/O_0-I/O_7	Multiplexed Parallel Data Inputs	1.75/0.406
	3-State Parallel Data Outputs	75/15 (12.5)
Q_0, Q_7	Serial Outputs	25/12.5

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Functional Description

The 'F323 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous reset, shift left, shift right, parallel load and hold operations. The type of operation is determined by S_0 and S_1 as shown in the Mode Select Table. All flip-flop outputs are brought out through 3-state buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q_0 and Q_7 are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on $\overline{SR}$ overrides the Select inputs and allows the flip-flops to be reset by the next rising edge of CP. All other state changes are also initiated by the LOW-to-HIGH CP transition. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP, are observed.

A HIGH signal on either $\overline{OE}_1$ or $\overline{OE}_2$ disables the 3-state buffers and puts the I/O pins in the high impedance state. In this condition the shift, load, hold and reset operations can still occur. The 3-state buffers are also disabled by HIGH signals on both S_0 and S_1 in preparation for a parallel load operation.

4

Mode Select Table

Inputs				Response
$\overline{SR}$	S_1	S_0	CP	
L	X	X	↑	Synchronous Reset; Q_0-Q_7 = LOW
H	H	H	↑	Parallel Load; $I/O_n \rightarrow Q_n$
H	L	H	↑	Shift Right; $DS_0 \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.
H	H	L	↑	Shift Left; $DS_7 \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
H	L	L	X	Hold

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↑ = LOW-to-HIGH transition

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		68	95	mA	V_{CC} = Max, CP = HIGH Outputs Disabled

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$			T_A, V_{CC} = Mil $C_L = 50\ pF$		T_A, V_{CC} = Com $C_L = 50\ pF$			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Input Frequency	70	100				70		MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay CP to Q_0 or Q_7	4.0 3.5	7.0 6.5	9.0 8.5			4.0 3.5	10.0 9.5	ns	3-1, 3-7
t_{PLH} t_{PHL}	Propagation Delay CP to I/O_n	4.0 5.0	7.0 8.5	9.0 11.0			4.0 5.0	10.0 12.0		
t_{PZH} t_{PZL}	Output Enable Time	3.5 4.0	6.0 7.0	8.0 10.0			3.5 4.0	9.0 11.0	ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time	2.5 2.0	4.5 4.0	6.0 5.5			2.5 2.0	7.0 6.5		

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW S_0 or S_1 to CP	8.5 8.5					8.5 8.5		ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW S_0 or S_1 to CP	0 0					0 0			
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW I/O_n, DS_0, DS_7 to CP	5.0 5.0					5.0 5.0		ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW I/O_n, DS_0, DS_7 to CP	2.0 2.0					2.0 2.0			
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{SR}$ to CP	10.0 10.0					10.0 10.0		ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{SR}$ to CP	0 0					0 0			
$t_w(H)$ $t_w(L)$	CP Pulse Width HIGH or LOW	7.0 7.0					7.0 7.0		ns	3-7

54F/74F350

4-Bit Shifter
With 3-State Outputs

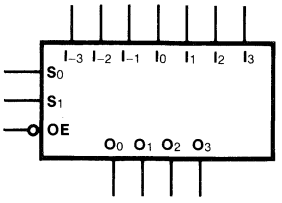
Description

The 'F350 is a specialized multiplexer that accepts a 4-bit word and shifts it 0, 1, 2 or 3 places, as determined by two Select (S_0, S_1) inputs. For expansion to longer words, three linking inputs are provided for lower-order bits; thus two packages can shift an 8-bit word, four packages a 16-bit word, etc. Shifting by more than three places is accomplished by paralleling the 3-state outputs of different packages and using the Output Enable ($\overline{OE}$) inputs as a third Select level. With appropriate interconnections, the 'F350 can perform zero-backfill, sign-extend or end-around (barrel) shift functions.

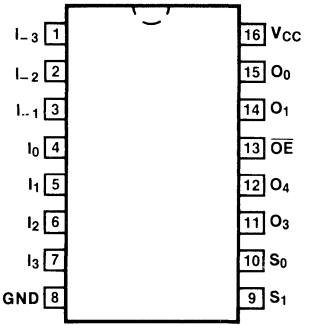
- **Linking Inputs for Word Expansion**
- **3-State Outputs for Extending Shift Range**

Ordering Code: See Section 5

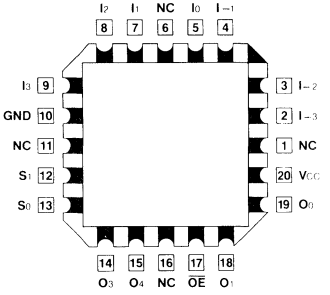
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
S_0, S_1	Select Inputs	0.5/0.75
I_{-3}-I_3	Data Inputs	0.5/0.75
$\overline{OE}$	Output Enable Input (Active LOW)	0.5/0.75
O_0-O_3	3-State Outputs	75/15 (12.5)

Functional Description

The 'F350 is operationally equivalent to a 4-input multiplexer with the inputs connected so that the select code causes successive one-bit shifts of the data word. This internal connection makes it possible to perform shifts of 0, 1, 2 or 3 places on words of any length.

A 7-bit data word is introduced at the I_n inputs and is shifted according to the code applied to the select inputs S_0, S_1. Outputs O_0-O_3 are 3-state, controlled by an active LOW output enable ($\overline{OE}$). When $\overline{OE}$ is LOW, data outputs will follow selected data inputs; when HIGH, the data outputs will be forced to the high impedance state. This feature allows shifters to be cascaded on the same output lines or to a common bus. The shift function can be logical, with zeros pulled in at either or both ends of the shifting field; arithmetic, where the sign bit is repeated during a shift down; or end around, where the data word forms a continous loop.

Logic Equations

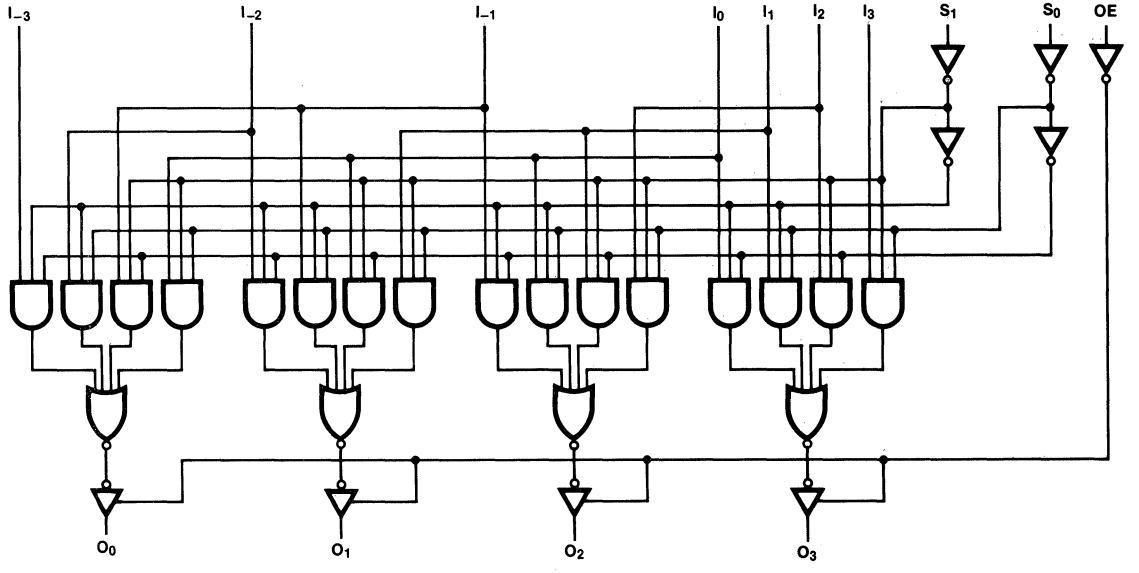
$$O_0 = \overline{S}_0\overline{S}_1I_0 + S_0\overline{S}_1I_{-1} + \overline{S}_0S_1I_{-2} + S_0S_1I_{-3}$$
$$O_1 = \overline{S}_0\overline{S}_1I_1 + S_0\overline{S}_1I_0 + \overline{S}_0S_1I_{-1} + S_0S_1I_{-2}$$
$$O_2 = \overline{S}_0\overline{S}_1I_2 + S_0\overline{S}_1I_1 + \overline{S}_0S_1I_0 + S_0S_1I_{-1}$$
$$O_3 = \overline{S}_0\overline{S}_1I_3 + S_0\overline{S}_1I_2 + \overline{S}_0S_1I_1 + S_0S_1I_0$$

Truth Table

Inputs			Outputs			
$\overline{OE}$	S_1	S_0	O_0	O_1	O_2	O_3
H	X	X	Z	Z	Z	Z
L	L	L	I_0	I_1	I_2	I_3
L	L	H	I_{-1}	I_0	I_1	I_2
L	H	L	I_{-2}	I_{-1}	I_0	I_1
L	H	H	I_{-3}	I_{-2}	I_{-1}	I_0

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

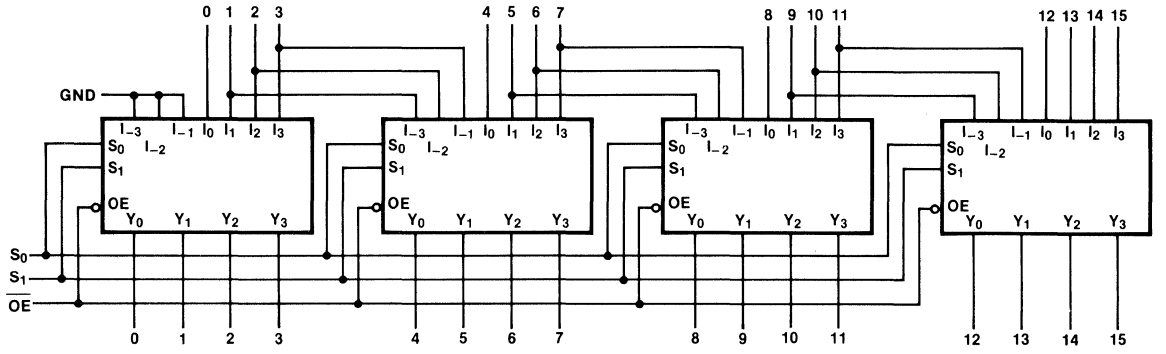
Symbol	Parameter	54F/74F			Units	Conditions	
		Min	Typ	Max			
I_{CCH}	Power Supply Current		22	35	mA	Outputs HIGH	V_{CC} = Max
I_{CCL}			27	41		Outputs LOW	
I_{CCZ}			26	42		Outputs OFF	

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay I_n to O_n	3.0 2.5	4.5 4.0	6.0 5.5			3.0 2.5	7.0 6.5	ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay S_n to O_n	4.0 3.0	7.8 6.5	10.0 8.5			4.0 3.0	11.0 9.5	ns	3-1 3-10
t_{PZH} t_{PZL}	Output Enable Time	2.5 4.0	5.0 7.0	7.0 9.0			2.5 4.0	8.0 10.0	ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time	2.0 2.0	3.9 4.0	5.5 5.5			2.0 2.0	6.5 6.5		

Applications

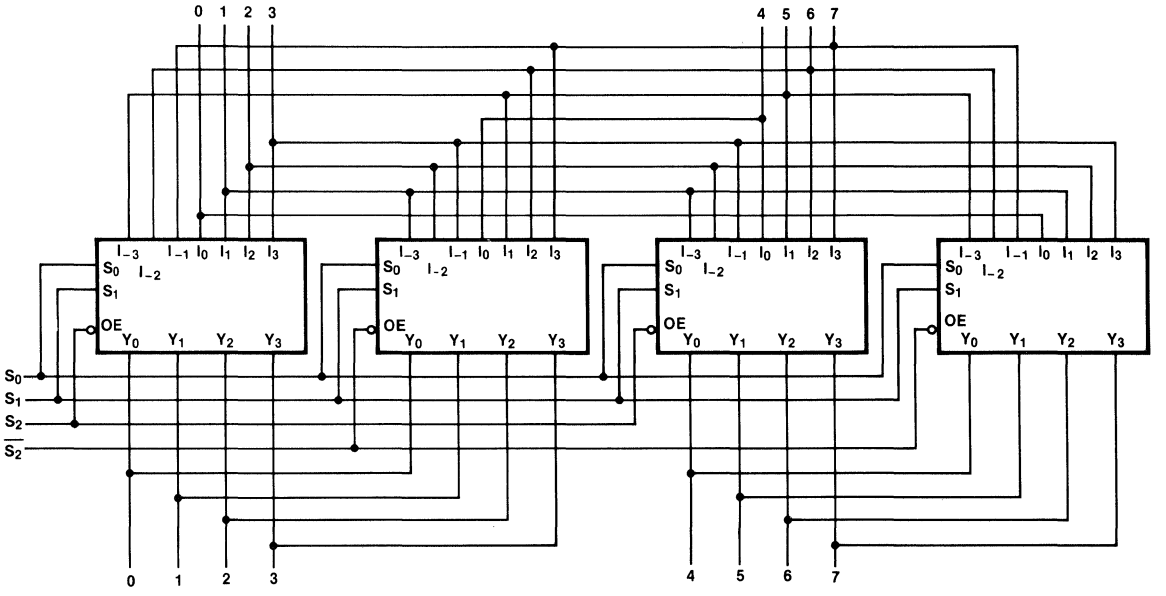
16-Bit Shift-Up 0 to 3 Places, Zero Backfill



Function Table

S_1	S_0	Shift Function
L	L	No Shift
L	H	Shift 1 Place
H	L	Shift 2 Places
H	H	Shift 3 Places

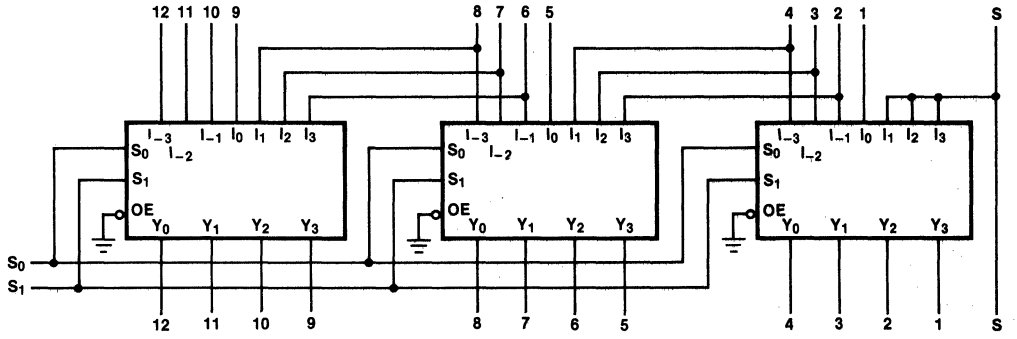
8-Bit End Around Shift 0 to 7 Places



Function Table

S_2	S_1	S_0	Shift Function
L	L	L	No Shift
L	L	H	Shift End Around 1
L	H	L	Shift End Around 2
L	H	H	Shift End Around 3
H	L	L	Shift End Around 4
H	L	H	Shift End Around 5
H	H	L	Shift End Around 6
H	H	H	Shift End Around 7

13-Bit Twos Complement Scaler



Function Table

S_1	S_0	Scale
L	L ÷ 8	1/8
L	H ÷ 4	1/4
H	L ÷ 2	1/2
H	H No Change	1

54F/74F352

Dual 4-Input Multiplexer

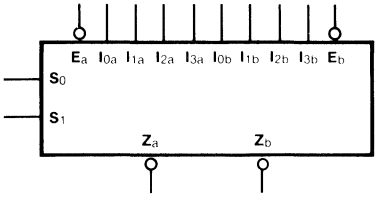
Description

The 'F352 is a very high-speed dual 4-input multiplexer with common Select inputs and individual Enable inputs for each section. It can select two bits of data from four sources. The two buffered outputs present data in the inverted (complementary) form. The 'F352 is the functional equivalent of the 'F153 except with inverted outputs.

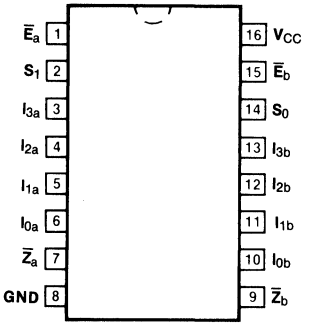
- **Inverted Version of the 'F153**
- **Separate Enables for Each Multiplexer**
- **Input Clamp Diode Limits High Speed Termination Effects**

Ordering Code: See Section 5

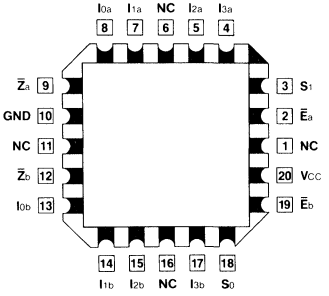
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
I_{0a}-I_{3a}	Side A Data Inputs	0.5/0.375
I_{0b}-I_{3b}	Side B Data Inputs	0.5/0.375
S_0, S_1	Common Select Inputs	0.5/0.375
$\overline{E}_a$	Side A Enable Input (Active LOW)	0.5/0.375
$\overline{E}_b$	Side B Enable Input (Active LOW)	0.5/0.375
$\overline{Z}_a$, $\overline{Z}_b$	Multiplexer Outputs (Inverted)	25/12.5

Functional Description

The 'F352 is a dual 4-input multiplexer. It selects two bits of data from up to four sources under the control of the common Select inputs(S_0, S_1). The two 4-input multiplexer circuits have individual active LOW Enables ($\overline{E}_a$, $\overline{E}_b$) which can be used to strobe the outputs independently. When the Enables ($\overline{E}_a$, $\overline{E}_b$) are HIGH, the corresponding outputs ($\overline{Z}_a$, $\overline{Z}_b$) are forced HIGH.

The logic equations for the outputs are shown below:

$$\overline{Z}_a = \overline{E}_a \bullet (I_{0a} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1a} \bullet \overline{S}_1 \bullet S_0 + I_{2a} \bullet S_1 \bullet \overline{S}_0 + I_{3a} \bullet S_1 \bullet S_0)$$

$$\overline{Z}_b = \overline{E}_b \bullet (I_{0b} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1b} \bullet \overline{S}_1 \bullet S_0 + I_{2b} \bullet S_1 \bullet \overline{S}_0 + I_{3b} \bullet S_1 \bullet S_0)$$

The 'F352 can be used to move data from a group of registers to a common output bus. The particular register from which the data came would be determined by the state of the Select inputs. A less obvious application is as a function generator. The 'F352 can generate two functions of three variables. This is useful for implementing highly irregular random logic.

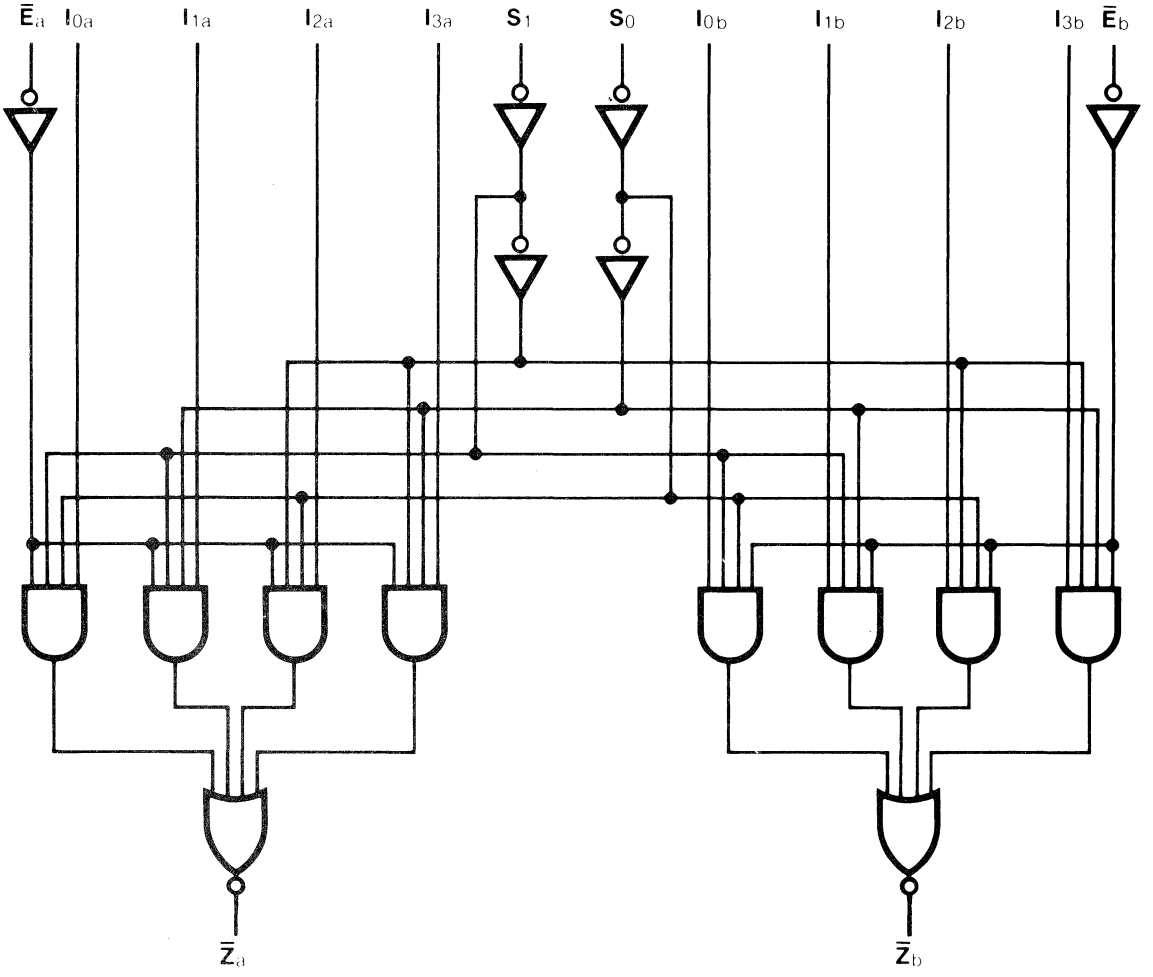
4

Truth Table

Select Inputs		Inputs (a or b)					Output
S_0	S_1	$\overline{E}$	I_0	I_1	I_2	I_3	$\overline{Z}$
X	X	H	X	X	X	X	H
L	L	L	L	X	X	X	H
L	L	L	H	X	X	X	L
H	L	L	X	L	X	X	H
H	L	L	X	H	X	X	L
L	H	L	X	X	L	X	H
L	H	L	X	X	H	X	L
H	H	L	X	X	X	L	H
H	H	L	X	X	X	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions	
		Min	Typ	Max			
I_{CCH}	Power Supply Current		9.3	14.0	mA	V_{IN} = Gnd	V_{CC} = Max
I_{CCL}			13.3	20.0		V_{IN} = HIGH	

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F $T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$			54F T_A, V_{CC} = Mil $C_L = 50\ pF$		74F T_A, V_{CC} = Com $C_L = 50\ pF$		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	3.5	8.0	11.0	3.0	14.0	3.0	12.5	ns	3-1
t_{PHL}	S_n to $\overline{Z}_n$	3.0	6.5	8.5	2.5	11.0	2.5	9.5		3-10
t_{PLH}	Propagation Delay	2.5	4.5	6.0	2.0	8.0	2.0	7.0	ns	3-1
t_{PHL}	$\overline{E}_n$ to $\overline{Z}_n$	3.0	5.0	7.0	2.5	9.0	2.5	8.0		3-4
t_{PLH}	Propagation Delay	2.5	5.2	7.0	2.0	9.0	2.0	8.0	ns	3-1
t_{PHL}	I_n to $\overline{Z}_n$	1.5	2.5	3.5	1.0	5.0	1.0	4.0		3-3

54F/74F353

Dual 4-Input Multiplexer With 3-State Outputs

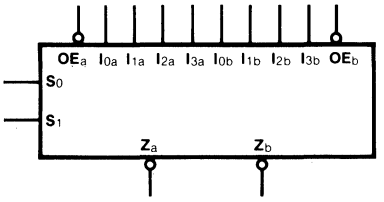
Description

The 'F353 is a dual 4-input multiplexer with 3-state outputs. It can select two bits of data from four sources using common Select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output Enable ($\overline{OE}$) inputs, allowing the outputs to interface directly with bus-oriented systems.

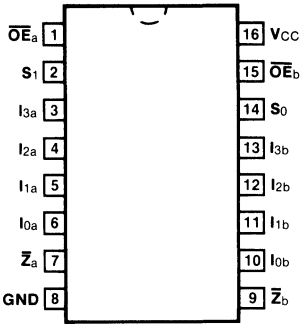
- **Inverted Version of 'F253**
- **Multifunction Capability**
- **Separate Enables for Each Multiplexer**

Ordering Code: See Section 5

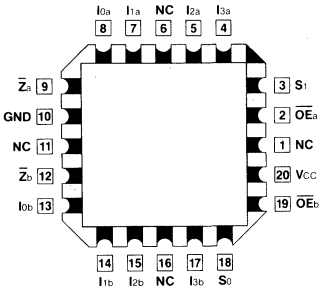
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
I_{0a}-I_{3a}	Side A Data Inputs	0.5/0.375
I_{0b}-I_{3b}	Side B Data Inputs	0.5/0.375
S_0, S_1	Common Select Inputs	0.5/0.375
$\overline{OE}_a$	Side A Output Enable Input (Active LOW)	0.5/0.375
$\overline{OE}_b$	Side B Output Enable Input (Active LOW)	0.5/0.375
$\overline{Z}_a$, $\overline{Z}_b$	3-State Outputs (Inverted)	25/12.5

Functional Description

The 'F353 contains two identical 4-input multiplexers with 3-state outputs. They select two bits from four sources selected by common Select inputs (S_0, S_1). The 4-input multiplexers have individual Output Enable ($\overline{OE}_a$, $\overline{OE}_b$) inputs which, when HIGH, force the outputs to a high impedance (High Z) state. The logic equations for the outputs are shown below:

$$\overline{Z}_a = \overline{OE}_a \bullet (I_{0a} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1a} \bullet \overline{S}_1 \bullet S_0 + I_{2a} \bullet S_1 \bullet \overline{S}_0 + I_{3a} \bullet S_1 \bullet S_0)$$

$$\overline{Z}_b = \overline{OE}_b \bullet (I_{0b} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1b} \bullet \overline{S}_1 \bullet S_0 + I_{2b} \bullet S_1 \bullet \overline{S}_0 + I_{3b} \bullet S_1 \bullet S_0)$$

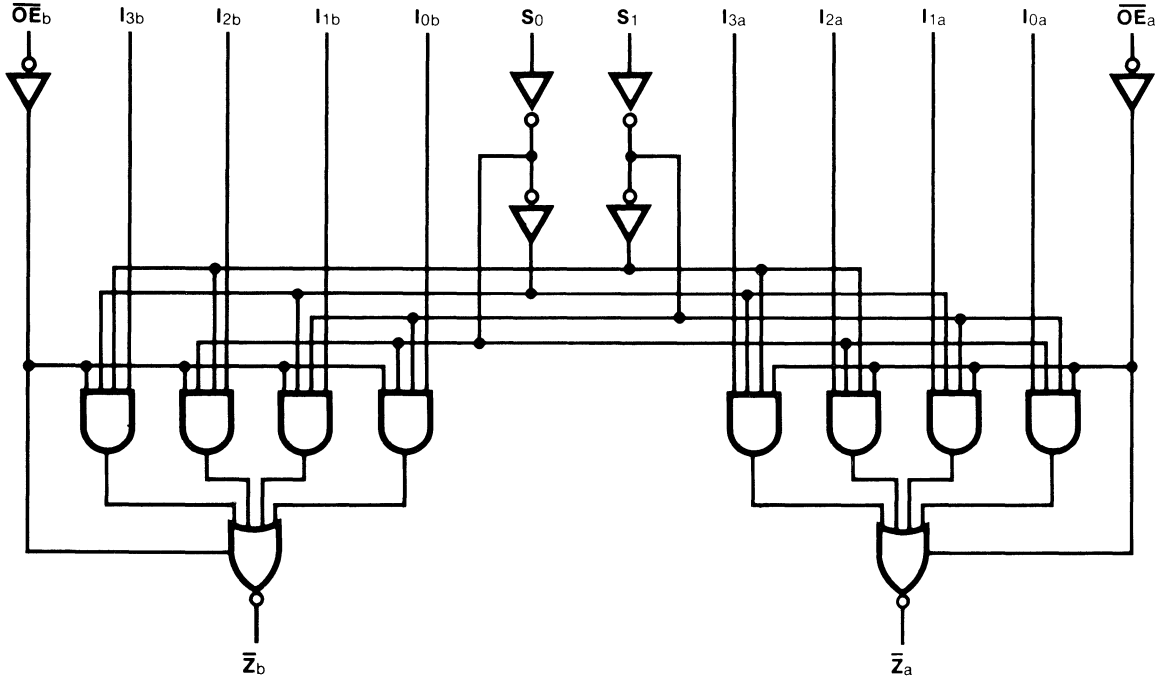
If the outputs of 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so that there is no overlap.

Truth Table

Select Inputs		Data Inputs				Output Enable	Output
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{OE}$	$\overline{Z}$
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	L	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

Address inputs S_0 and S_1 are common to both sections.
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions	
		Min	Typ	Max			
I_{CCH}	Power Supply Current		9.3	14.0	mA	I_n, S_n, $\overline{OE}_n$ = Gnd	V_{CC} = Max
I_{CCL}			13.3	20.0		I_n, S_n = Gnd	
I_{CCZ}			15.0	23.0		$\overline{OE}_n$ = HIGH	

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{Z}_n$	3.5 3.0	8.0 6.5	11.0 8.5	3.0 2.5	14.0 11.0	3.0 2.5	12.5 9.5	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay I_n to $\overline{Z}_n$	2.5 1.0	5.2 2.5	7.0 3.5	2.0 1.0	9.0 5.0	2.0 1.0	8.0 4.0	ns	3-1 3-3
t_{PZH} t_{PZL}	Output Enable Time	3.0 3.5	5.5 6.0	8.0 8.0	3.0 3.0	10.5 10.5	3.0 3.0	9.0 9.0	ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time	2.0 2.0	3.7 4.4	5.0 6.0	2.0 1.5	7.0 8.0	1.5 1.5	6.0 7.0		

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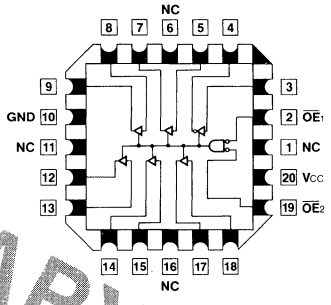
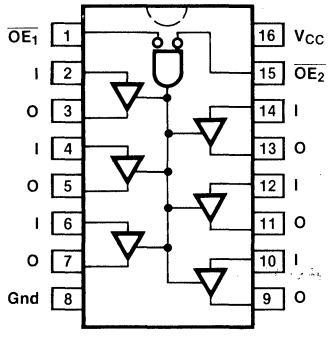
Hex Buffer/Driver With 3-State Outputs

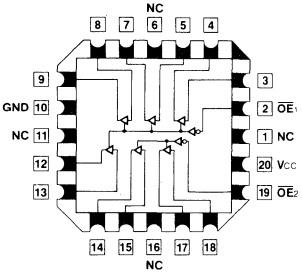
- 3-State Buffer Outputs Sink 64mA
- High Speed
- Bus Oriented

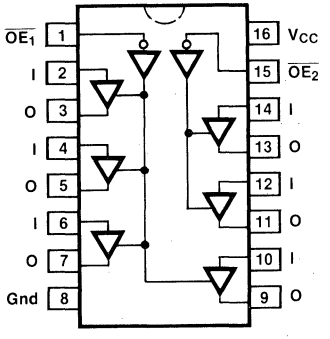
Connection Diagrams





'F365





'F367

Pin Assignment for LCC and PCC

Pin Assignment for DIP and SOIC

Ordering Code: See Section 5

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
$\overline{OE_1}$, $\overline{OE_2}$	3-State Output: Enable Input (Active LOW)	0.5/0.375
I	Inputs	0.5/0.375
O, $\overline{O}$	Outputs	75/40 (30)

Function Table, 'F365

Inputs			Outputs	
$\overline{OE}_1$	$\overline{OE}_2$	I	O	$\overline{O}$
L	L	L	L	H
L	L	H	H	L
X	H	X	Z	Z
H	X	X	Z	Z

Function Table, 'F367

Inputs		Outputs	
$\overline{OE}$	I	$\overline{O}$	$\overline{O}$
L	L	L	H
L	H	H	L
H	X	Z	Z

L = LOW Voltage Level
H = HIGH Voltage Level
X = Immaterial
Z = High Impedance

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CCH} I_{CCL} I_{CCZ}	Power Supply Current		35 60 60	50 90 90	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay		7.0 7.0						ns	3-1 3-4
t_{PZH} t_{PZL}	Enable Time		14.0 11.0						ns	3-1, 3-13 3-12
t_{PHZ} t_{PLZ}	Disable Time		9.0 17.0						ns	3-1, 3-13 3-12

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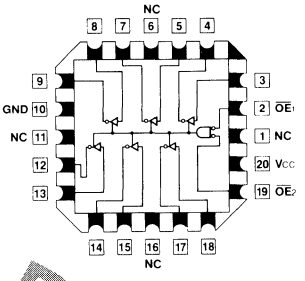
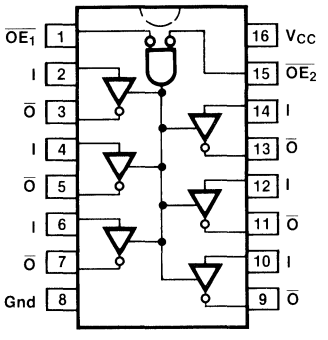
Hex Inverter Buffer With 3-State Outputs

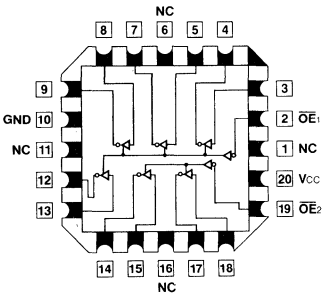
- 3-State Buffer Outputs Sink 64 mA
- High-Speed
- Bus-Oriented

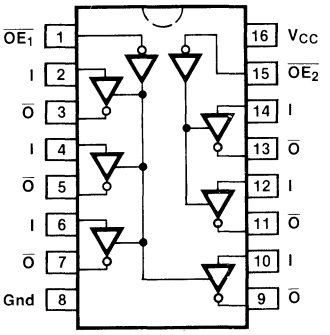
Connection Diagrams





'F366





'F368

Pin Assignment for LCC and PCC

Pin Assignment for DIP and SOIC

Ordering Code: See Section 5

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
$\overline{OE_1}$, $\overline{OE_2}$	3-State Output: Enable Input (Active LOW)	0.5/0.375
I	Inputs	0.5/0.375
O, $\overline{O}$	Outputs	75/40 (30)

Function Table, 'F366

Inputs			Outputs	
$\overline{OE}_1$	$\overline{OE}_2$	I	O	$\overline{O}$
L	L	L	L	H
L	L	H	H	L
X	H	X	Z	Z
H	X	X	Z	Z

Function Table, 'F368

Inputs		Outputs	
$\overline{OE}$	I	O	$\overline{O}$
L	L	L	H
L	H	H	L
H	X	Z	Z

L = LOW Voltage Level
H = HIGH Voltage Level
X = Immaterial
Z = High Impedance

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CCH}	Power Supply Current		35	50	mA	V_{CC} = Max
I_{CCL}			60	90		
I_{CCZ}			60	90		

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay		7.0						ns	3-1
t_{PHL}			7.0							3-3
t_{PZH}	Enable Time		14.0						ns	3-1, 3-13
t_{PZL}			11.0							3-12
t_{PHZ}	Disable Time		9.0						ns	3-1, 3-13
t_{PLZ}			17.0							3-12

54F/74F373

Octal Transparent Latch With 3-State Outputs

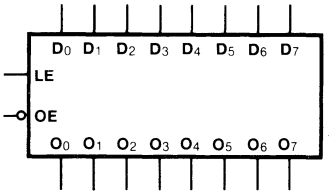
Description

The 'F373 consists of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH the bus output is in the high impedance state.

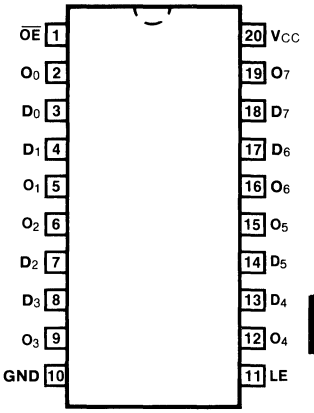
- **Eight Latches in a Single Package**
- **3-State Outputs for Bus Interfacing**

Ordering Code: See Section 5

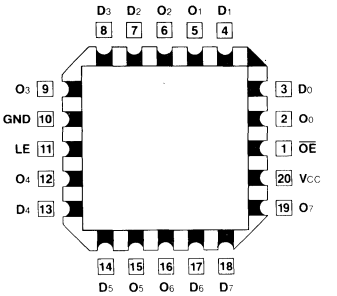
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

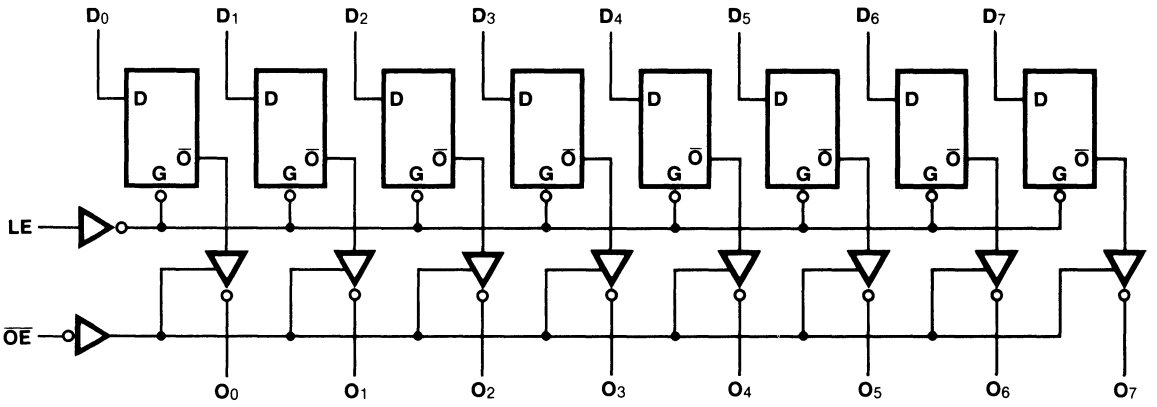
Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
D_0-D_7	Data Inputs	0.5/0.375
$\overline{LE}$	Latch Enable Input (Active HIGH)	0.5/0.375
$\overline{OE}$	Output Enable Input (Active LOW)	0.5/0.375
O_0-O_7	3-State Latch Outputs	75/15 (12.5)

Functional Description

The 'F373 contains eight D-type latches with 3-state output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-state buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are in the bi-state mode. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CCZ}	Power Supply Current (All Outputs OFF)		38	55	mA	V_{CC} = Max, $\overline{OE}$ = HIGH D_n, LE = Gnd

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$			T_A, V_{CC} = Mil $C_L = 50\ pF$		T_A, V_{CC} = Com $C_L = 50\ pF$			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	3.0	5.3	7.0	3.0	8.5	3.0	8.0	ns	3-1
t_{PHL}	D_n to O_n	2.0	3.7	5.0	2.0	7.0	2.0	6.0		3-4
t_{PLH}	Propagation Delay	5.0	9.0	11.5	5.0	15.0	5.0	13.0	ns	3-1
t_{PHL}	LE to O_n	3.0	5.2	7.0	3.0	8.5	3.0	8.0		3-7
t_{PZH}	Output Enable Time	2.0	5.0	11.0	2.0	13.5	2.0	12.0	ns	3-1, 3-12
t_{PZL}		2.0	5.6	7.5	2.0	10.0	2.0	8.5		3-13
t_{PHZ}	Output Disable Time	2.0	4.5	6.5	2.0	10.0	2.0	7.5	ns	3-1, 3-12
t_{PLZ}		2.0	3.8	6.0	2.0	7.0	2.0	6.0		3-13

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
$t_s(H)$	Setup Time, HIGH or LOW	2.0			2.0		2.0		ns	3-15
$t_s(L)$	D_n to LE	2.0			2.0		2.0			
$t_h(H)$	Hold Time, HIGH or LOW	3.0			3.0		3.0			
$t_h(L)$	D_n to LE	3.0			3.0		3.0			
$t_w(H)$	LE Pulse Width, HIGH	6.0			6.0		6.0		ns	3-7

54F/74F374

Octal D-Type Flip-Flop With 3-State Outputs

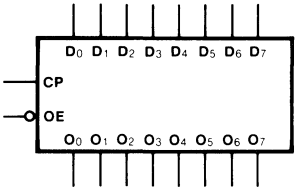
Description

The 'F374 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops.

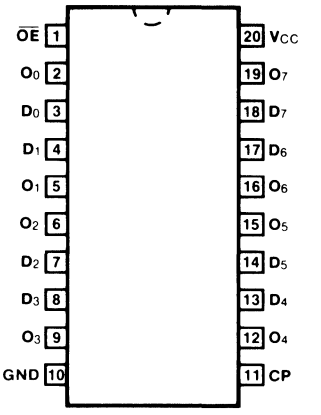
- **Edge-triggered D-Type Inputs**
- **Buffered Positive Edge-Triggered Clock**
- **3-State Outputs for Bus-Oriented Applications**

Ordering Code: See Section 5

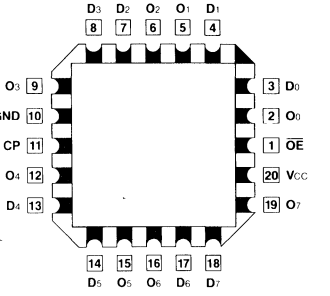
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
D_0-D_7	Data Inputs	0.5/0.375
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
$\overline{OE}$	3-State Output Enable Input (Active LOW)	0.5/0.375
O_0-O_7	3-State Outputs	75/15 (12.5)

Functional Description

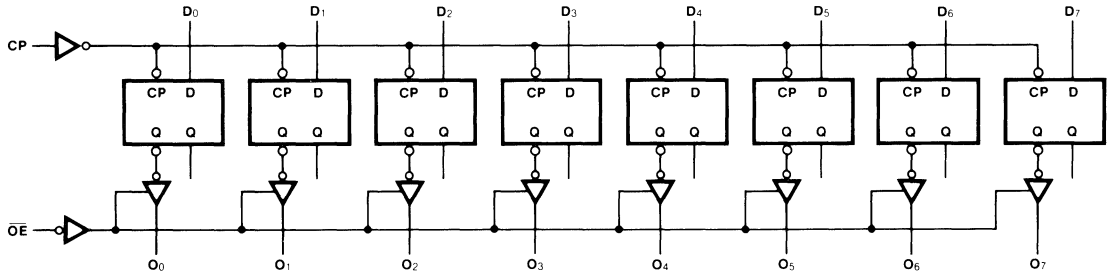
The 'F374 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-state true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Truth Table

Inputs		Outputs	
D_n	CP	$\overline{OE}$	O_n
H	⌜⌟	L	H
L	⌜⌟	L	L
X	X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CCZ}	Power Supply Current (All Outputs OFF)		55	86	mA	V_{CC} = Max, D_n = Gnd $\overline{OE}$ = HIGH

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$			T_A, V_{CC} = Mil $C_L = 50\ pF$		T_A, V_{CC} = Com $C_L = 50\ pF$			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	100	140		60		70		MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay CP to O_n	4.0 4.0	6.5 6.5	8.5 8.5	4.0 4.0	10.5 11.0	4.0 4.0	10.0 10.0	ns	3-1 3-7
t_{PZL} t_{PZL}	Output Enable Time	2.0 2.0	9.0 5.8	11.5 7.5	2.0 2.0	14.0 10.0	2.0 2.0	12.5 8.5	ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time	2.0 2.0	5.3 4.3	7.0 5.5	2.0 2.0	8.0 7.5	2.0 2.0	8.0 6.5		

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW D_n to CP	2.0 2.0			2.5 2.0		2.0 2.0		ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D_n to CP	2.0 2.0			2.0 2.5		2.0 2.0			
$t_w(H)$ $t_w(L)$	CP Pulse Width HIGH or LOW	7.0 6.0			7.0 6.0		7.0 6.0		ns	3-7

54F/74F377

Octal D Flip-Flop With Clock Enable

Description

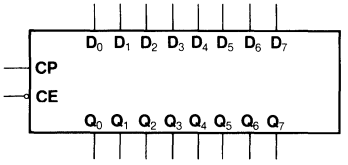
The 'F377 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously, when the Clock Enable ($\overline{CE}$) is LOW.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The $\overline{CE}$ input must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

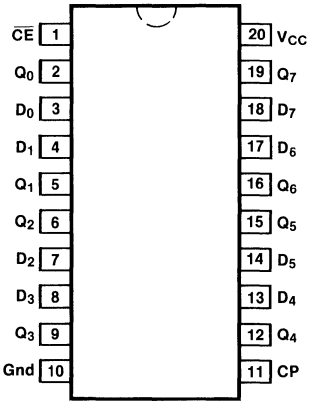
- **Ideal for Addressable Register Applications**
- **Clock Enable for Address and Data Synchronization Applications**
- **Eight Edge-Triggered D Flip-Flops**
- **Buffered Common Clock**
- **See 'F273 for Master Reset Version**
- **See 'F373 for Transparent Latch Version**
- **See 'F374 for 3-State Version**

Ordering Code: See Section 5

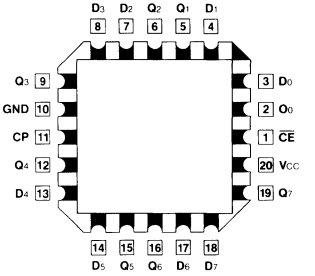
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

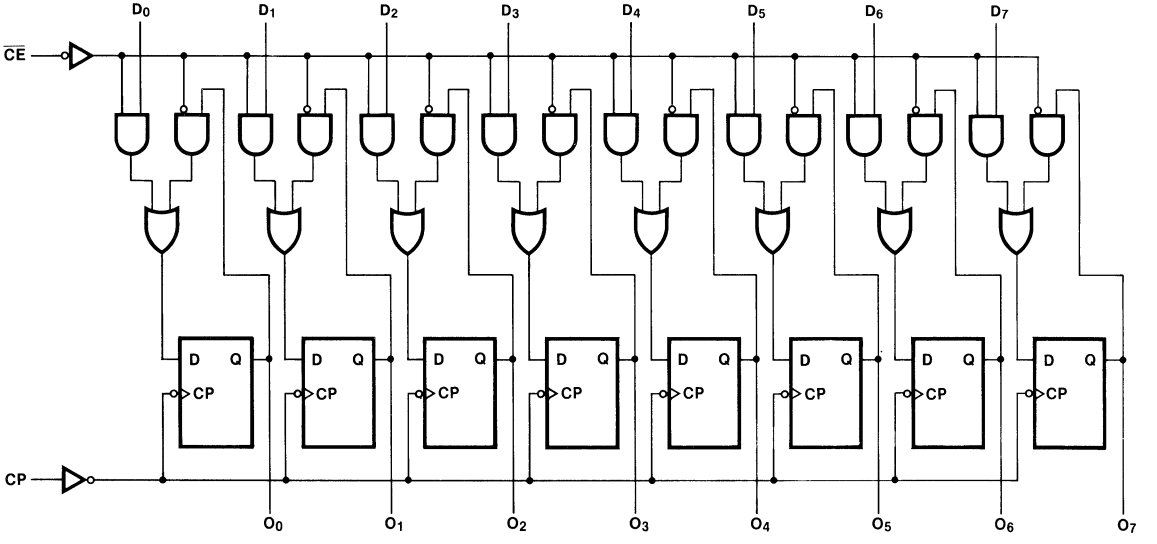
Pin Names	Description	54F/74F(U.L.) HIGH/LOW
D_0-D_7	Data Inputs	0.5/0.375
$\overline{CE}$	Clock Enable (Active LOW)	0.5/0.375
Q_0-Q_7	Data Outputs	25/12.5
CP	Clock Pulse Input	0.5/0.375

Mode Select-Function Table

Operating Mode	Inputs			Outputs
	CP	$\overline{CE}$	D_n	Q_n
Load "1"	↑	l	h	H
Load "0"	↑	l	l	L
Hold (Do Nothing)	↑	h	X	No Change
	X	H	X	No Change

H = HIGH Voltage Level
h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
L = LOW Voltage Level
l = LOW Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
X = Immaterial
↑ = LOW-to-HIGH Clock Transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions	
		Min	Typ	Max			
I_{CCH}	Power Supply Current		35	50	mA	Outputs HIGH	V_{CC} = Max
I_{CCL}			40	60		Outputs LOW	

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	100							MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n		**11.0** **12.0**						ns	3-1 3-7

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
t_s(H) t_s(L)	Setup Time, HIGH or LOW D_n to CP	3.0 3.0							ns	3-5
t_h(H) t_h(L)	Hold Time, HIGH or LOW D_n to CP	1.0 1.0							ns	3-5
t_s(H) t_s(L)	Setup Time, HIGH or LOW $\overline{CE}$ to CP	3.0 3.0							ns	3-5
t_h(H) t_h(L)	Hold Time, HIGH or LOW $\overline{CE}$ to CP	1.0 1.0							ns	3-5
t_w(L)	Clock Pulse Width, LOW	4.0							ns	3-7

54F/74F378

Parallel D Register With Enable

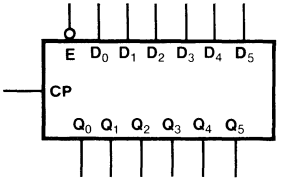
Description

The 'F378 is a 6-bit register with a buffered common Enable. This device is similar to the 'F174, but with common Enable rather than common Master Reset.

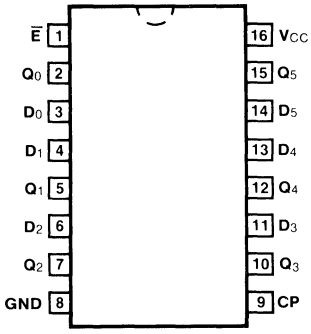
- **6-Bit High-Speed Parallel Register**
- **Positive Edge-Triggered D-Type Inputs**
- **Fully Buffered Common Clock and Enable Inputs**
- **Input Clamp Diodes Limit High-Speed Termination Effects**
- **Full TTL and CMOS Compatible**

Ordering Code: See Section 5

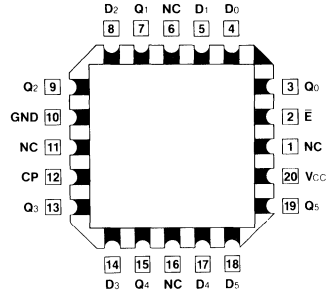
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
$\overline{E}$	Enable Input (Active LOW)	0.5/0.375
D_0-D_5	Data Inputs	0.5/0.375
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
Q_0-Q_5	Outputs	25/12.5

Functional Description

The 'F378 consists of six edge-triggered D-type flip-flops with individual D inputs and Q inputs. The Clock (CP) and Enable ($\overline{E}$) inputs are common to all flip-flops.

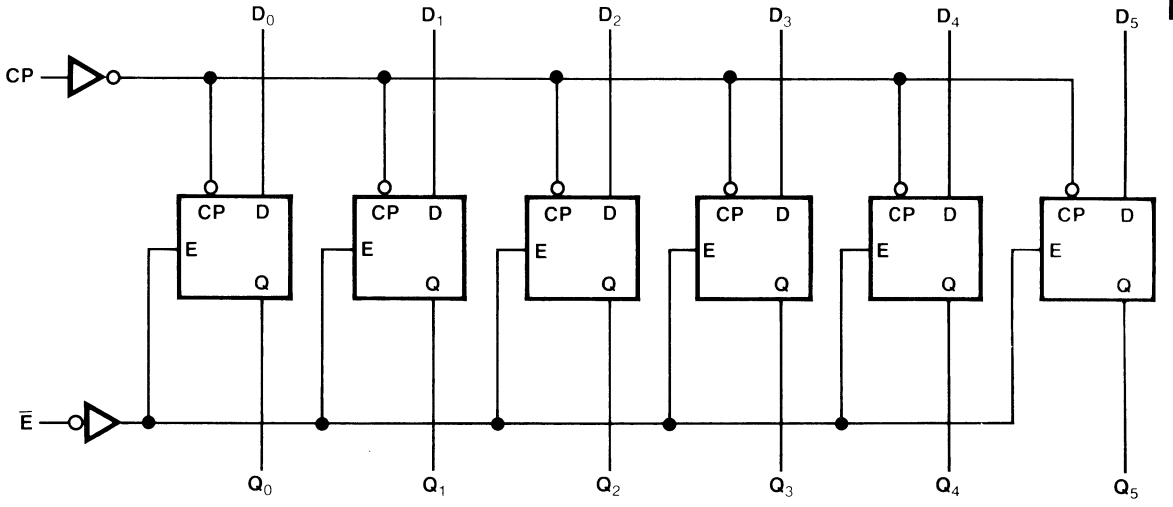
When the $\overline{E}$ input is LOW, new data is entered into the register on the LOW-to-HIGH transition of the CP input. When the $\overline{E}$ input is HIGH the register will retain the present data independent of the CP input.

Truth Table

Inputs			Output
$\overline{E}$	CP	D_n	Q_n
H	⎍	X	No Change
L	⎍	H	H
L	⎍	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		30	45	mA	V_{CC} = Max, V_{CP} = 0

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$			T_A, V_{CC} = Mil $C_L = 50\ pF$		T_A, V_{CC} = Com $C_L = 50\ pF$			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Input Frequency	80	100		70		80		MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n	3.0 3.5	5.5 6.0	7.5 8.5	3.0 3.5	10.0 10.5	3.0 3.5	8.5 9.5	ns	3-1 3-7

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW D_n to CP	4.0 4.0			5.0 5.0		4.0 4.0		ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D_n to CP	0 0			2.0 2.0		0 0		ns	3-5
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{E}$ to CP	4.0 10.0			4.5 13.0		4.0 10.0		ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{E}$ to CP	0 0			0 0		0 0		ns	3-5
$t_w(H)$ $t_w(L)$	CP Pulse Width HIGH or LOW	4.0 6.0			5.0 7.5		4.0 6.0		ns	3-7

54F/74F379

Quad Parallel Register With Enable

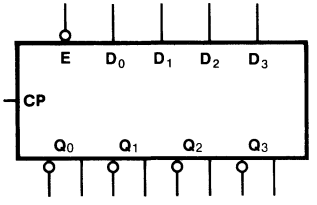
Description

The 'F379 is a 4-bit register with buffered common Enable. This device is similar to the 'F175 but features the common Enable rather than common Master Reset.

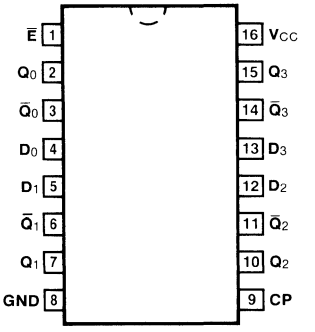
- **Edge-Triggered D-Type Inputs**
- **Buffered Positive Edge-Triggered Clock**
- **Buffered Common Enable Input**
- **True and Complement Outputs**

Ordering Code: See Section 5

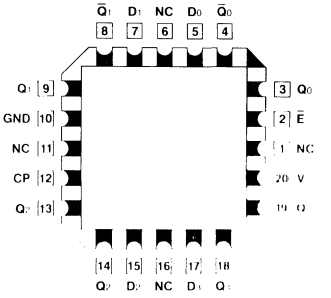
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
$\overline{E}$	Enable Input (Active LOW)	0.5/0.375
D_0-D_3	Data Inputs	0.5/0.375
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
Q_0-Q_3	Flip-Flop Outputs	25/12.5
$\overline{Q}_0$-$\overline{Q}_3$	Complement Outputs	25/12.5

Functional Description

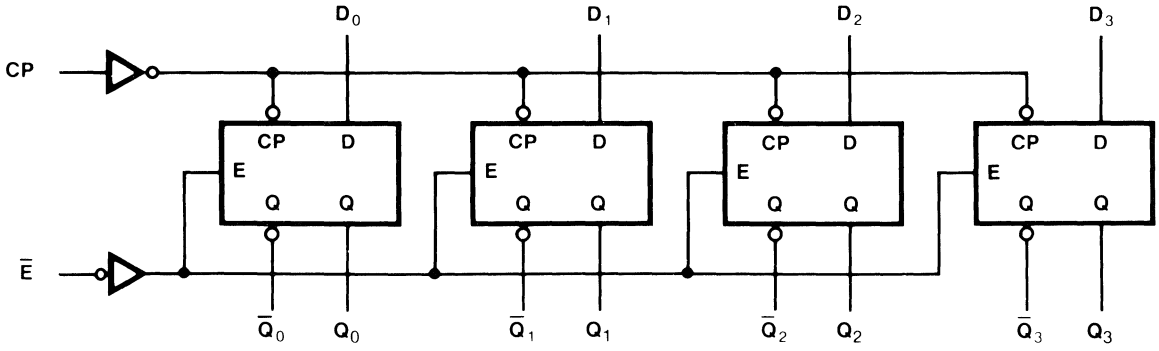
The 'F379 consists of four edge-triggered D-type flip-flops with individual D inputs and Q and $\overline{Q}$ outputs. The Clock (CP) and Enable ($\overline{E}$) inputs are common to all flip-flops. When the $\overline{E}$ input is HIGH, the register will retain the present data independent of the CP input. The D_n and $\overline{E}$ inputs can change when the clock is in either state, provided that the recommended setup and hold times are observed.

Truth Table

Inputs			Outputs	
$\overline{E}$	CP	D_n	Q_n	$\overline{Q}_n$
H	↑	X	NC	NC
L	↑	H	H	L
L	↑	L	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↑ = LOW-to-HIGH Transition
NC = No Change

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		28	40	mA	V_{CC} = Max; D, $\overline{E}$ = Gnd, CP = ⌐

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$			T_A, V_{CC} = Mil $C_L = 50\ pF$		T_A, V_{CC} = Com $C_L = 50\ pF$			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	100	140				100		MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n, $\overline{Q}_n$	4.0 5.0	5.0 6.5	6.5 8.5			4.0 5.0	7.5 9.5	ns	3-1 3-7

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW D_n to CP	3.0 3.0					3.0 3.0		ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D_n to CP	1.0 1.0					1.0 1.0			
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{E}$ to CP	6.0 6.0					6.0 6.0		ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{E}$ to CP	0 0					0 0			
$t_w(H)$ $t_w(L)$	CP Pulse Width HIGH or LOW	4.0 5.0					4.0 5.0		ns	3-7

54F/74F381

4-Bit Arithmetic Logic Unit

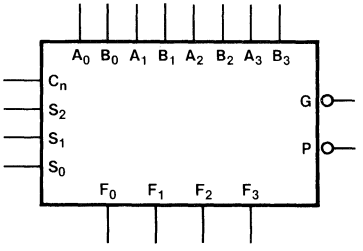
Description

The 'F381 performs three arithmetic and three logic operations on two 4-bit words, A and B. Two additional select input codes force the function outputs LOW or HIGH. Carry propagate and generate outputs are provided for use with the 'F182 carry lookahead generator for high-speed expansion to longer word lengths. For ripple expansion, refer to the 'F382 ALU data sheet.

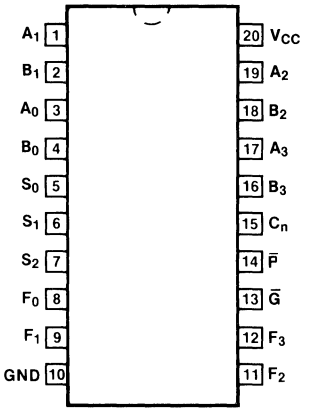
- **Low Input Loading Minimizes Drive Requirements**
- **Performs Six Arithmetic and Logic Functions**
- **Selectable LOW (Clear) and HIGH (Preset) Functions**
- **Carry Generate and Propagate Outputs for use with Carry Lookahead Generator**

Ordering Code: See Section 5

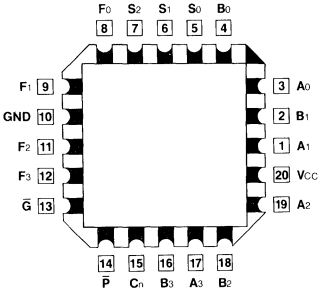
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
A_0-A_3	A Operand Inputs	0.5/1.50
B_0-B_3	B Operand Inputs	0.5/1.50
S_0-S_2	Function Select Inputs	0.5/0.375
C_n	Carry Input	0.5/1.50
$\overline{G}$	Carry Generate Output (Active LOW)	25/12.5
$\overline{P}$	Carry Propagate Output (Active LOW)	25/12.5
F_0-F_3	Function Outputs	25/12.5

Functional Description

Signals applied to the Select inputs S_0-S_2 determine the mode of operation, as indicated in the Function Select Table. An extensive listing of input and output levels is shown in the Truth Table. The circuit performs the arithmetic functions for either active HIGH or active LOW operands, with output levels in the same convention. In the Subtract operating modes, it is necessary to force a carry (HIGH for active HIGH operands, LOW for active LOW operands) into the C_n input of the least significant package.

The Carry Generate ($\overline{G}$) and Carry Propagate ($\overline{P}$) outputs supply input signals to the 'F182 carry lookahead generator for expansion to longer word length, as shown in Figure a. Note that an 'F382 ALU is used for the most significant package. Typical delays for Figure a are given in Figure b.

Function Select Table

Select			Operation
S_0	S_1	S_2	
L	L	L	Clear
H	L	L	B Minus A
L	H	L	A Minus B
H	H	L	A Plus B
L	L	H	A⊕B
H	L	H	A + B
L	H	H	AB
H	H	H	Preset

H = HIGH Voltage Level
L = LOW Voltage Level

4

Fig. a 16-Bit Lookahead Carry ALU Expansion

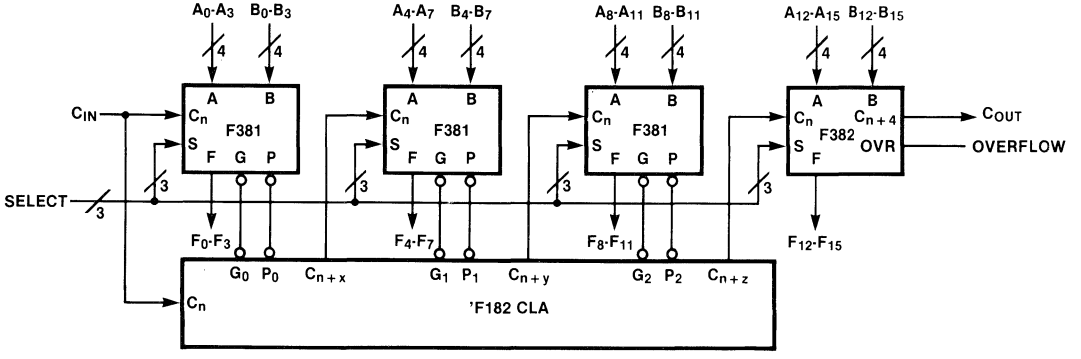
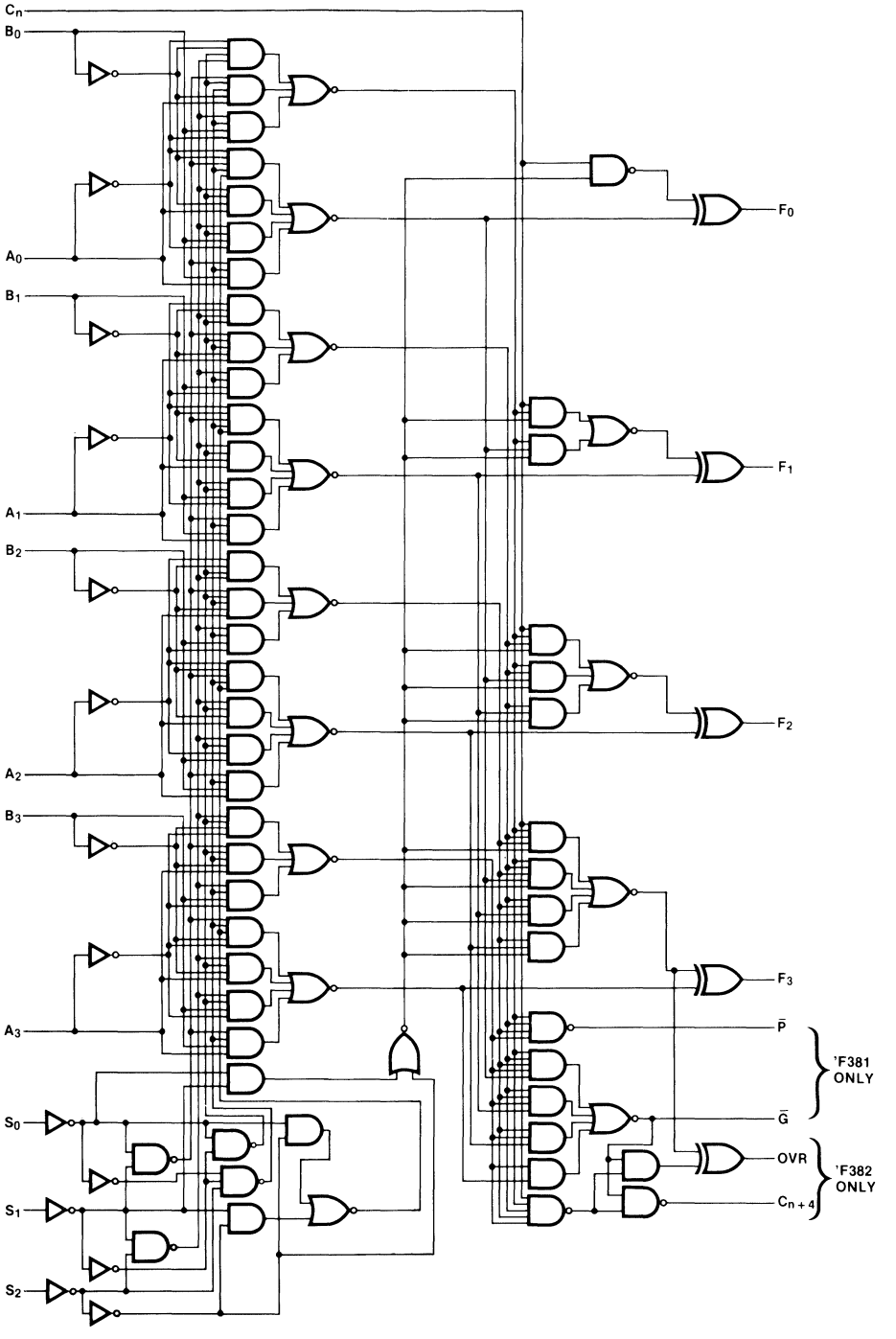


Fig. b 16-Bit Delay Tabulation

PATH SEGMENT	TOWARD F	OUTPUT C_{n+4}, OVR
A_i or B_i to $\overline{P}$	7.2 ns	7.2 ns
$\overline{P}_i$ to C_{n+j} ('F182)	6.2 ns	6.2 ns
C_n to F	8.1 ns	—
C_n to C_{n+4}, OVR	—	8.0 ns
Total Delay	21.5 ns	21.4 ns

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Truth Table

	Inputs						Outputs					
Function	S_0	S_1	S_2	C_n	A_n	B_n	F_0	F_1	F_2	F_3	$\overline{G}$	$\overline{P}$
CLEAR	0	0	0	X	X	X	0	0	0	0	0	0
B MINUS A	1	0	0	0	0	0	1	1	1	1	1	0
				0	0	1	0	1	1	1	0	0
				0	1	0	0	0	0	0	1	1
				0	1	1	1	1	1	1	1	0
				1	0	0	0	0	0	0	1	0
				1	0	1	1	1	1	1	0	0
				1	1	0	1	0	0	0	1	1
				1	1	1	0	0	0	0	1	0
A MINUS B	0	1	0	0	0	0	1	1	1	1	1	0
				0	0	1	0	0	0	0	1	1
				0	1	0	0	1	1	1	0	0
				0	1	1	1	1	1	1	1	0
				1	0	0	0	0	0	0	1	0
				1	0	1	1	0	0	0	1	1
				1	1	0	1	1	1	1	0	0
				1	1	1	0	0	0	0	1	0
A PLUS B	1	1	0	0	0	0	0	0	0	0	1	1
				0	0	1	1	1	1	1	1	0
				0	1	0	1	1	1	1	1	0
				0	1	1	0	1	1	1	0	0
				1	0	0	1	0	0	0	1	1
				1	0	1	0	0	0	0	1	0
				1	1	0	0	0	0	0	1	0
				1	1	1	1	1	1	1	0	0
A ⊕ B	0	0	1	X	0	0	0	0	0	0	1	1
				X	0	1	1	1	1	1	1	1
				X	1	0	1	1	1	1	1	0
				X	1	1	0	0	0	0	0	0
A + B	1	0	1	X	0	0	0	0	0	0	1	1
				X	0	1	1	1	1	1	1	1
				X	1	0	1	1	1	1	1	1
				X	1	1	1	1	1	1	1	0
AB	0	1	1	X	0	0	0	0	0	0	0	0
				X	0	1	0	0	0	0	1	1
				X	1	0	0	0	0	0	0	0
				X	1	1	1	1	1	1	1	0
PRESET	1	1	1	X	0	0	1	1	1	1	1	1
				X	0	1	1	1	1	1	1	1
				X	1	0	1	1	1	1	1	1
				X	1	1	1	1	1	1	1	0

1 = HIGH Voltage Level
0 = LOW Voltage Level
X = Immaterial

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		59	89	mA	V_{CC} = Max, S_0-S_3 = Gnd; Other Inputs HIGH

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay C_n to F_i	2.5 2.5	8.1 5.7	12.0 8.0			2.5 2.5	13.0 9.0	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay Any A or B to Any F	4.0 3.5	10.4 8.2	15.0 11.0			4.0 3.5	16.0 12.0	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay S_i to F_i	4.5 4.0	8.3 8.2	20.0 11.0			4.5 4.0	21.5 12.0	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay A_i or B_i to $\overline{G}$	3.5 4.0	6.4 6.8	9.0 10.0			3.5 4.0	10.0 11.0	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay A_i or B_i to $\overline{P}$	4.0 3.5	7.2 6.5	10.5 9.5			4.0 3.5	11.5 10.5	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay S_i to $\overline{G}$ or $\overline{P}$	4.0 4.5	7.8 10.2	12.0 13.5			4.0 4.5	13.0 14.5	ns	3-1 3-10

54F/74F382

4-Bit Arithmetic Logic Unit

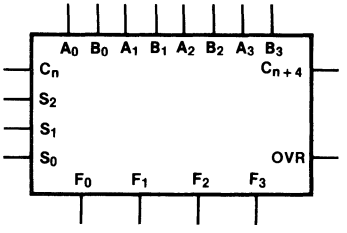
Description

The 'F382 performs three arithmetic and three logic operations on two 4-bit words, A and B. Two additional Select input codes force the Function outputs LOW or HIGH. An Overflow output is provided for convenience in twos complement arithmetic. A Carry output is provided for ripple expansion. For high-speed expansion using a Carry Lookahead Generator, refer to the 'F381 data sheet.

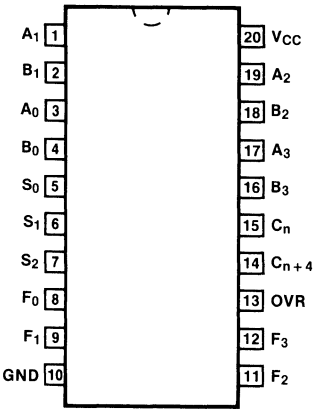
- **Performs Six Arithmetic and Logic Functions**
- **Selectable LOW (Clear) and HIGH (Preset) Functions**
- **LOW Input Loading Minimizes Drive Requirements**
- **Carry Output for Ripple Expansion**
- **Overflow Output for Twos Complement Arithmetic**

Ordering Code: See Section 5

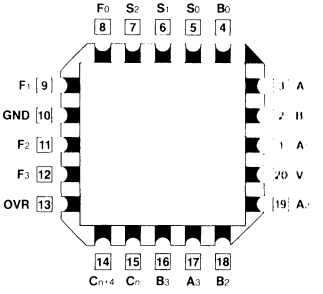
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC

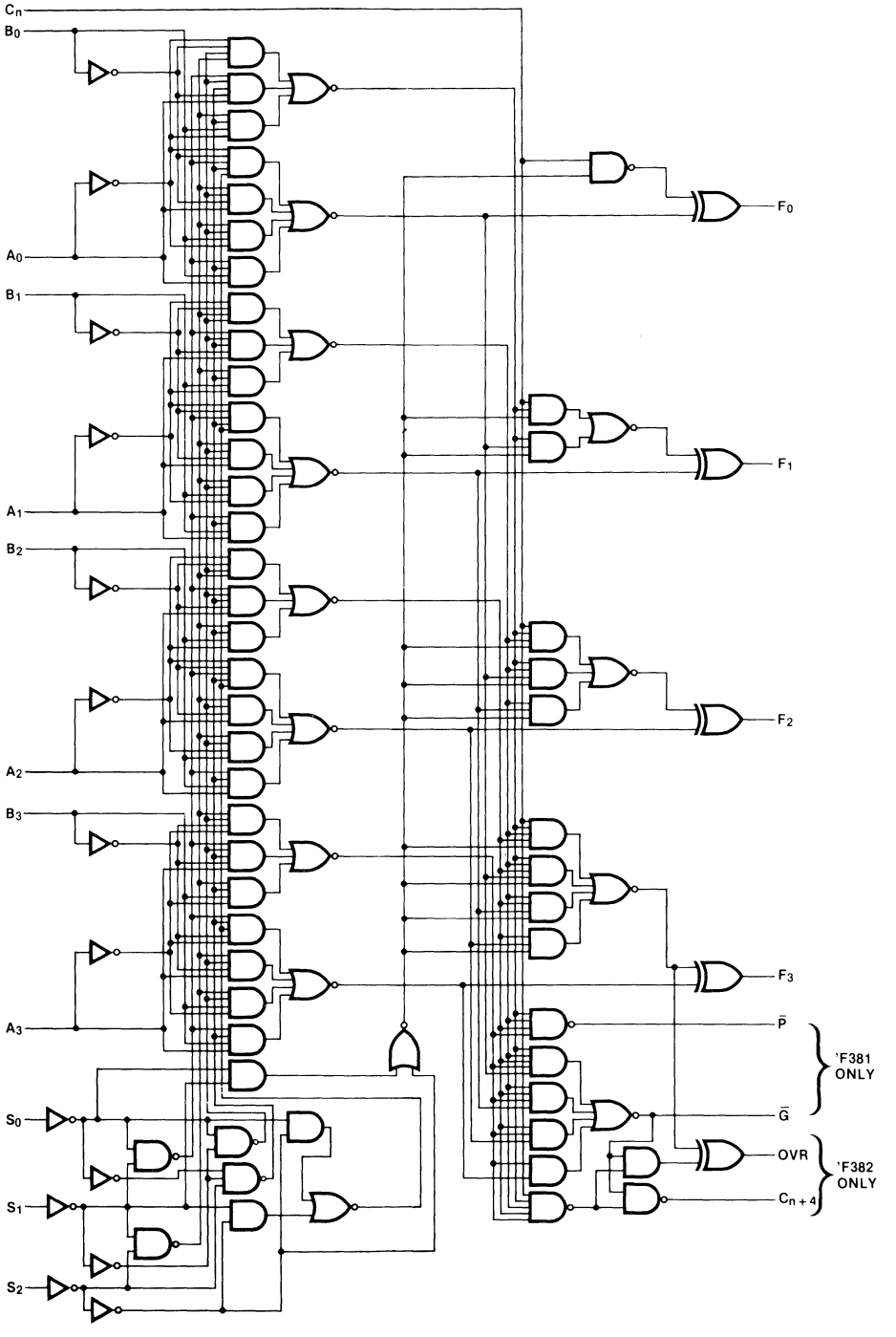


Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
A_0-A_3	A Operand Inputs	0.5/1.50
B_0-B_3	B Operand Inputs	0.5/1.50
S_0-S_2	Function Select Inputs	0.5/0.375
C_n	Carry Input	0.5/1.875
C_{n+4}	Carry Output	25/12.5
OVR	Overflow Output	25/12.5
F_0-F_3	Function Outputs	25/12.5

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Functional Description

Signals applied to the Select inputs S_0-S_2 determine the mode of operation, as indicated in the Function Select Table. An extensive listing of input and output levels is shown in the Truth Table. The circuit performs the arithmetic functions for either active HIGH or active LOW operands, with output levels in the same convention. In the Subtract operating modes, it is necessary to force a carry (HIGH for active HIGH operands, LOW for active LOW operands) into the C_n input of the least significant package. Ripple expansion is illustrated in Figure a. The overflow output OVR is the Exclusive-OR of C_{n+3} and C_{n+4}; a HIGH signal on OVR indicates overflow in twos complement operation. Typical delays for Figure a are given in Figure b.

Function Select Table

Select			Operation
S_0	S_1	S_2	
L	L	L	Clear
H	L	L	B Minus A
L	H	L	A Minus B
H	H	L	A Plus B
L	L	H	A⊕B
H	L	H	A+B
L	H	H	AB
H	H	H	Preset

H = HIGH Voltage Level
L = LOW Voltage Level

Fig. a 16-Bit Ripple Carry ALU Expansion

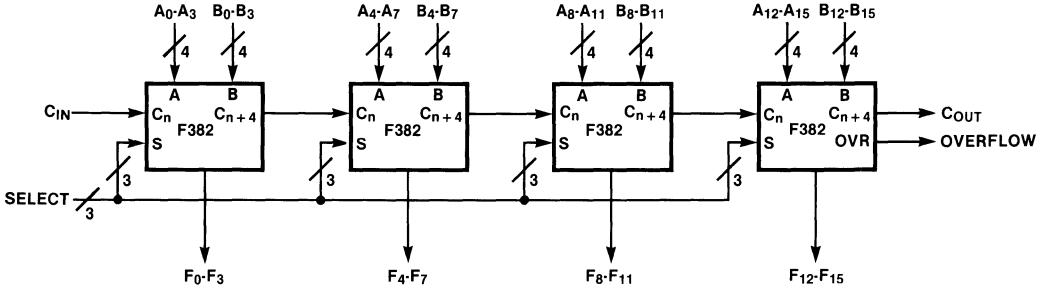


Fig. b 16-Bit Delay Tabulation

PATH SEGMENT	TOWARD F	OUTPUT C_{n+4}, OVR
A_i or B_i to C_{n+4}	6.5 ns	6.5 ns
C_n to C_{n+4}	6.3 ns	6.3 ns
C_n to C_{n+4}	6.3 ns	6.3 ns
C_n to F	8.1 ns	—
C_n to C_{n+4}, OVR	—	8.0 ns
Total Delay	27.2 ns	27.1 ns

Truth Table

	Inputs						Outputs					
Function	S_0	S_1	S_2	C_n	A_n	B_n	F_0	F_1	F_2	F_3	OVR	C_{n+4}
CLEAR	0	0	0	0	X	X	0	0	0	0	1	1
				1	X	X	0	0	0	0	1	1
B MINUS A	1	0	0	0	0	0	1	1	1	1	0	0
				0	0	1	0	0	0	0	0	1
				0	1	0	0	0	0	0	0	0
				0	1	1	1	1	1	1	0	0
				1	0	0	0	0	0	0	0	1
				1	0	1	1	1	1	1	0	1
				1	1	0	1	0	0	0	0	0
				1	1	1	0	0	0	0	0	1
A MINUS B	0	1	0	0	0	0	1	1	1	1	0	0
				0	0	1	0	0	0	0	0	0
				0	1	0	0	1	1	1	0	1
				0	1	1	1	1	1	1	0	0
				1	0	0	0	0	0	0	0	1
				1	0	1	1	0	0	0	0	0
				1	1	0	1	1	1	1	0	1
				1	1	1	0	0	0	0	0	1
A PLUS B	1	1	0	0	0	0	0	0	0	0	0	0
				0	0	1	1	1	1	1	0	0
				0	1	0	1	1	1	1	0	0
				0	1	1	0	1	1	1	0	1
				1	0	0	1	0	0	0	0	0
				1	0	1	0	0	0	0	0	1
				1	1	0	0	0	0	0	0	1
				1	1	1	1	1	1	1	0	1
A ⊕ B	0	0	1	X	0	0	0	0	0	0	0	0
				X	0	1	1	1	1	1	0	0
				0	1	0	1	1	1	1	0	0
				X	1	1	0	0	0	0	1	1
				1	1	0	1	1	1	1	1	1
A + B	1	0	1	X	0	0	0	0	0	0	0	0
				X	0	1	1	1	1	1	0	0
				X	1	0	1	1	1	1	0	0
				0	1	1	1	1	1	1	0	0
				1	1	1	1	1	1	1	1	1
AB	0	1	1	X	0	0	0	0	0	0	1	1
				X	0	1	0	0	0	0	0	0
				X	1	0	0	0	0	0	1	1
				0	1	1	1	1	1	1	0	0
				1	1	1	1	1	1	1	1	1
PRESET	1	1	1	X	0	0	1	1	1	1	0	0
				X	0	1	1	1	1	1	0	0
				X	1	0	1	1	1	1	0	0
				0	1	1	1	1	1	1	0	0
				1	1	1	1	1	1	1	1	1

1 = HIGH Voltage Level 0 = LOW Voltage Level X = Immaterial

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		54	81	mA	V_{CC} = Max; S_0, C_n = HIGH Other Inputs Gnd

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			54F T_A, V_{CC} = Mil C_L = 50 pF		74F T_A, V_{CC} = Com C_L = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay C_n to F_i	3.0 2.5	8.1 5.7	12.0 8.0			3.0 2.5	13.0 9.0	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay Any A or B to Any F	4.0 3.5	10.4 8.2	15.0 11.0			4.0 3.5	16.0 12.0	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay S_i to F_i	6.5 4.0	11.0 8.2	15.0 20.5			6.5 4.0	16.0 21.5	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay A_i or B_i to C_{n+4}	3.5 3.5	6.0 6.5	8.5 9.0			3.5 3.5	9.5 10.5	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay S_i to OVR or C_{n+4}	7.0 5.0	12.5 9.0	16.5 12.0			7.0 5.0	17.5 13.0	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay C_n to C_{n+4}	3.5 3.5	5.6 6.3	8.0 9.0			3.5 3.5	9.0 10.0	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay C_n to OVR	3.5 4.5	8.0 7.1	11.0 10.0			3.5 4.5	12.0 11.0	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay A_i or B_i to OVR	7.0 5.5	11.5 8.0	15.5 10.5			7.0 5.5	16.5 11.5	ns	3-1 3-10

54F/74F384

8-Bit Serial/Parallel Twos Complement Multiplier

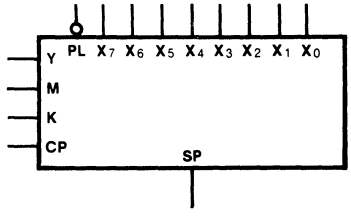
Description

The 'F384 is an 8-bit by 1-bit sequential logic element that multiplies two numbers represented in twos complement notation. The device implements Booth's algorithm internally to produce a twos complement product that needs no subsequent correction. Parallel inputs accept and store an 8-bit multiplicand (X_0-X_7). The multiplier word is applied to the Y input in a serial bit stream, least significant bit first. The product is clocked out at the SP output, least significant bit first.

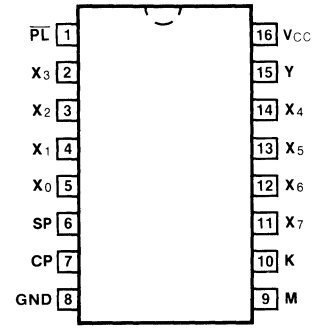
The K input is used for expansion to longer X words, using two or more 'F384 devices. The Mode Control (M) input is used to establish the most significant device. An asynchronous Parallel Load ($\overline{PL}$) input clears the internal flip-flops to the start condition and enables the X latches to accept new multiplicand data.

Ordering Code: See Section 5

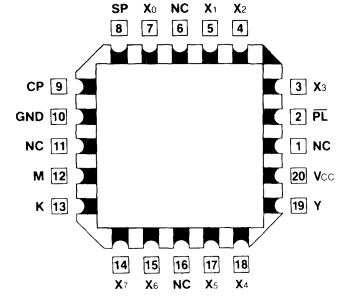
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
K	Serial Expansion Input	0.5/0.375
M	Mode Control Input	0.5/0.375
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)	0.5/0.75
X_0-X_7	Multiplicand Data Inputs	0.5/0.375
Y	Serial Multiplier Input	0.5/0.375
SP	Serial X•Y Product Output	25/12.5

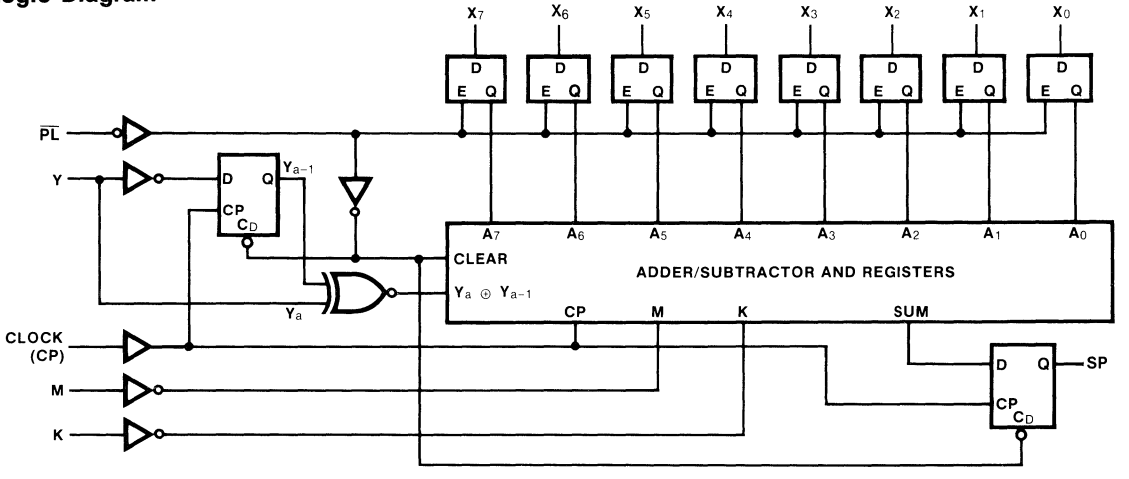
Functional Description

Referring to the Logic Diagram, the multiplicand (X_0-X_7) latches are enabled to receive new data when $\overline{PL}$ is LOW. Data that meet the setup time requirements are latched and stored when $\overline{PL}$ goes HIGH. The LOW signal on $\overline{PL}$ also clears the Y_{a-1} flip-flop as well as the carry-save flip-flops and the partial product register in the arithmetic section. Figure a is a conceptual logic diagram of a typical cell in the arithmetic section, except for the first (X_7) cell, in which K is the B_i input and M is incorporated into the carry logic. The cells use the carry-save technique to avoid the complexity and delays inherent in lookahead carry schemes for longer words.

Figure b is a timing diagram for an 8x8 multiplication process. New multiplicand data enters the X latches during bit time T_0. It is assumed that $\overline{PL}$ goes LOW shortly after the CP rising edge that marks the beginning of T_0 and goes HIGH again shortly after the beginning of T_1. The LSB (Y_0) of the multiplier is applied to the Y input during T_1 and combines with X_0 in the least significant cell to form the appropriate D input (X_0 Y_0) to the sum flip-flop. This is clocked into the sum flip-flop by the CP rising edge at the beginning of T_2 and this LSB (S_0) of the product is available shortly thereafter at the SP output of the package. The next-least bit (Y_1) of the multiplier is also applied during T_2. The detailed logic design of the cell is such that during T_2 the D input to the sum flip-flop of the least significant cell contains not only X_0Y_1 but also, the X_1Y_0 product. Thus the term ($X_1Y_0 + X_0Y_1$) is formed at the D input of the least significant sum flip-flop during T_2 and this next-least term S_1 of the product is available at the SP output shortly after the CP rising edge at the beginning of T_3. Due to storage in the two preceding cells and in its own carry flip-flop, the D input to the least significant sum flip-flop during T_3 will contain the products X_2Y_0 and X_1Y_1 as well as X_0Y_2. During each succeeding bit time the SP output contains information formed one stage further upstream. For example, the SP output during T_9 contains X_7Y_0, which was actually formed during T_1.

The MSB Y_7 (the sign bit Y_S) of the multiplier is first applied to the Y input during T_8 and must also be applied during bit times T_9 through T_{16}. This extension of the sign bit is a necessary adjunct to the implementation of Booth's algorithm and is a built-in feature of the 'F322 Shift Register. Figure c shows the method of using two 'F384s to perform a 12xn bit multiplication. Notice that the sign of X is effectively extended by connecting X_{11} to X_4-X_7 of the most significant package. Whereas the 8x8 multiplication required 18 clock periods (m + n to form the product terms plus T_0 to clear the multiplier plus T_{17} to recognize and store S_{15}), the arrangement of Figure c requires 12 + n bits to form the product terms plus the bit times to clear the multiplier and to recognize and store SP_{n+11}.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Function Table

Inputs						Internal	Output	Function
$\overline{PL}$	CP	K	M	X_i	Y	Y_{a-1}	SP	
X	X	L	L	X	X	X	X	Most Significant Multiplier Device
X	X	CS	H	X	X	X	X	Devices Cascaded in Multiplier String
L	X	X	X	OP	X	L	L	Load New Multiplicand and Clear Internal Sum and Carry Registers
H	X	X	X	X	X	X	X	Device Enabled
H	↑	X	X	X	L	L	AR	Shift Sum Register
H	↑	X	X	X	L	H	AR	Add Multiplicand to Sum Register and Shift
H	↑	X	X	X	H	L	AR	Subtract Multiplicand from Sum Register and Shift
H	↑	X	X	X	H	H	AR	Shift Sum Register

H = HIGH Voltage Level
L = LOW Voltage Level
↑ = LOW-to-HIGH Transition
CS = Connected to SP output of high order device
OP = X_i latches open for new data (i = 0-7)
AR = Output as required per Booth's algorithm
X = Immaterial

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		60	90	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	80	100					70	MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay CP to SP	3.5 3.5	6.5 6.5	9.0 9.0			3.5 3.5	10.0 10.0	ns	3-1 3-7
t_{PHL}	Propagation Delay $\overline{PL}$ to SP	6.0	10.0	13.0			6.0	14.0	ns	3-1 3-11

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW K to CP	13.5 13.5		15.0 15.0	ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW K to CP	2.0 2.0		2.0 2.0		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW Y to CP	15.0 15.0		15.0 15.0	ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW Y to CP	2.0 2.0		2.0 2.0		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW X_n to $\overline{PL}$	5.5 5.5		6.5 6.5	ns	3-14
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW X_n to $\overline{PL}$	2.0 2.0		2.0 2.0		
$t_w(H)$ $t_w(L)$	CP Pulse Width HIGH or LOW	7.0 5.5		7.5 6.0	ns	3-7
$t_w(L)$	$\overline{PL}$ Pulse Width, LOW	6.5		7.0	ns	3-11
t_{rec}	Recovery Time $\overline{PL}$ to CP	5.5		6.0	ns	3-11

Fig. a Conceptual Carry Save Adder Cell

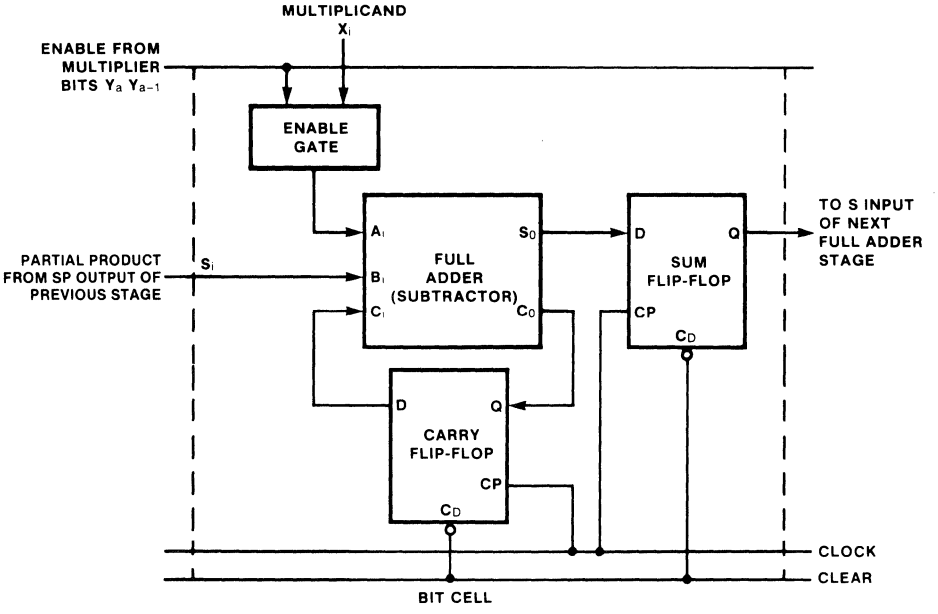


Fig. b Timing Diagram Showing 18 Clock Cycle Operation of 8x8 Multiplication

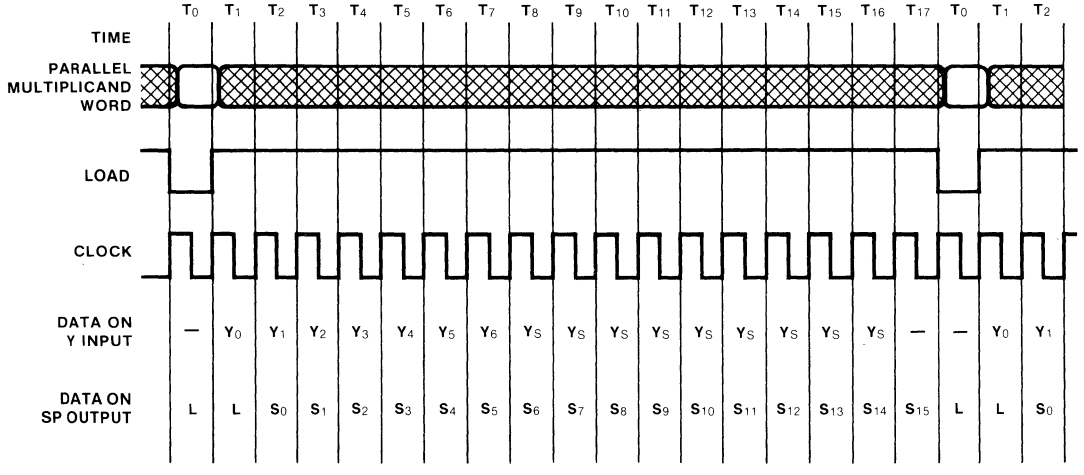
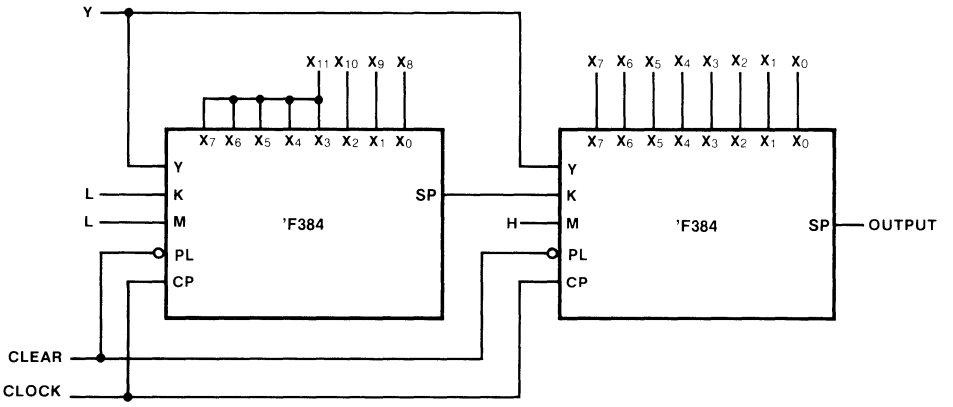


Fig. c 12-Bit by n-Bit Twos Complement Multiplier



54F/74F385

Quad Serial Adder/Subtractor

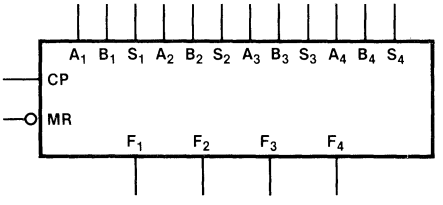
Description

The 'F385 contains four serial adder/subtractors with common clock and clear inputs, but independent operand and mode select inputs. Each adder/subtractor contains a sum flip-flop and a carry-save flip-flop for synchronous operations. Each circuit performs either A plus B or A minus B in twos complement notation, but can also be used for magnitude-only or ones complement operation. The 'F385 is designed for use with the 'F384 and 'F784 serial multipliers in implementing digital filters or butterfly networks in fast Fourier transforms.

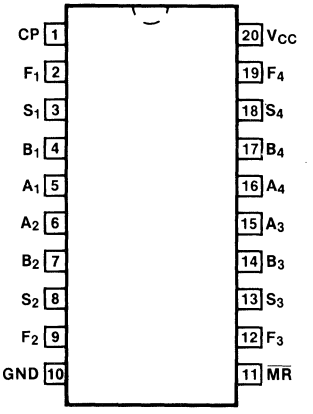
- **Four Independent Adder/Subtractors**
- **Twos Complement Arithmetic**
- **Synchronous Operation**
- **Common Clear and Clock**
- **Ones Complement or Magnitude-Only Capability**

Ordering Code: See Section 5

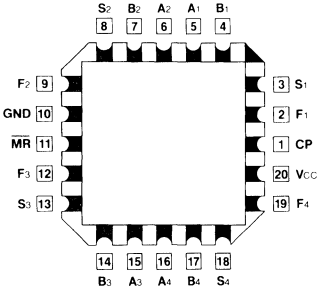
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
A_1-A_4	A Operand Inputs	0.5/0.375
B_1-B_4	B Operand Inputs	0.5/0.375
S_1-S_4	Function Select Inputs	0.5/0.375
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)	0.5/0.375
F_1-F_4	Sum or Difference Outputs	25/12.5

Functional Description

Each adder contains two edge-triggered flip-flops to store the sum and carry, as shown in the Logic Diagram. Flip-flop state changes occur on the rising edge of the Clock Pulse (CP) input signal. The Select (S) input should be LOW for the Add (A plus B) mode and HIGH for the Subtract (A minus B) mode. A LOW signal on the asynchronous Master Reset ($\overline{MR}$) input clears the sum flip-flop and resets the carry flip-flop to zero in the Add mode or presets it to one in the Subtract mode.

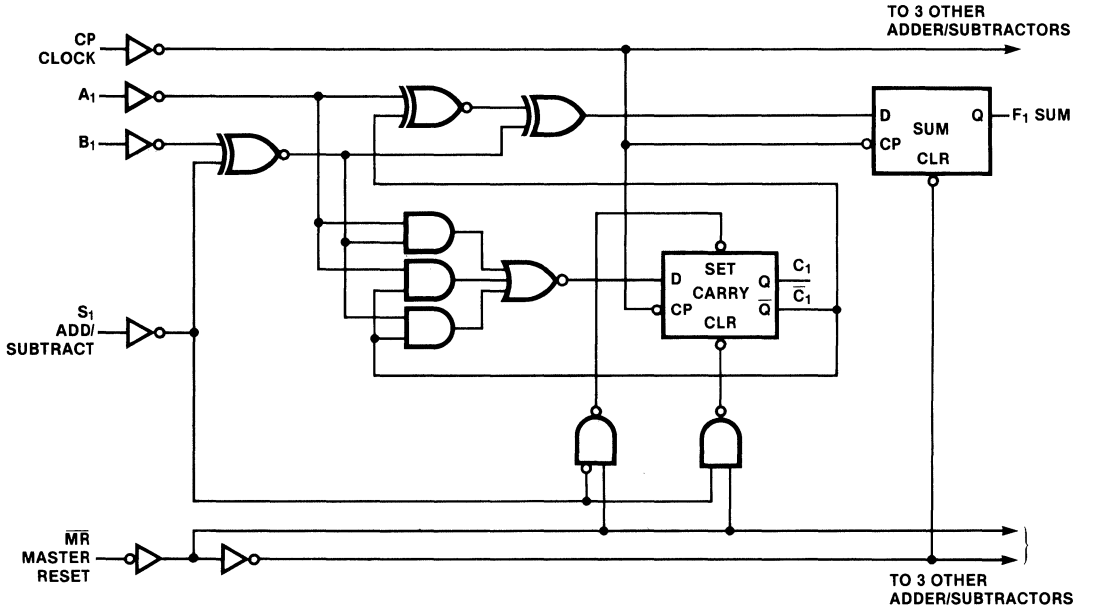
In the Subtract mode, the B operand is internally complemented. Presetting the carry flip-flop to one completes the twos complement transformation by adding one to 'A plus $\overline{B}$' during the first (LSB) operation after $\overline{MR}$ is released. For ones complement subtraction, the carry flip-flop can be set to zero by making S LOW during the reset, then making S HIGH after the reset but before the next clock.

Truth Table

Inputs*				Internal Carry		Output*	Function
$\overline{MR}$	S	A	B	C	C_1	F	
L	L	X	X	L	L	L	Clear
L	H	X	X	H	H	L	
H	L	L	L	L	L	L	Add
H	L	L	L	H	L	H	
H	L	L	H	L	L	H	
H	L	L	H	H	H	L	
H	L	H	L	L	L	H	
H	L	H	L	H	H	L	
H	L	H	H	L	H	L	
H	L	H	H	H	H	H	
H	H	L	L	L	L	H	Subtract
H	H	L	L	H	H	L	
H	H	L	H	L	L	L	
H	H	L	H	H	L	H	
H	H	H	L	L	H	L	
H	H	H	L	H	H	H	
H	H	H	H	L	L	H	
H	H	H	H	H	H	L	

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
* = Inputs before CP transition, output after C
C_1 = Carry flip-flop state before (C) and after (C_1) clock transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		68	95	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$			T_A, V_{CC} = Mil $C_L = 50\ pF$		T_A, V_{CC} = Com $C_L = 50\ pF$			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	70	100		65		70		MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay CP to F_n	3.5 4.0	6.0 7.0	8.0 9.0	3.0 3.5	10.0 11.0	3.5 4.0	9.0 10.0	ns	3-1 3-7
t_{PHL}	Propagation Delay $\overline{MR}$ to F_n	5.5	9.0	12.0	5.0	14.0	5.5	13.0	ns	3-1 3-11

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW A_n to CP	15.0 15.0			17.5 17.5		15.0 15.0		ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW A_n to CP	0 0			0 0		0 0			
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW B_n or S_n to CP	15.0 15.0			17.5 17.5		15.0 15.0		ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW B_n or S_n to CP	0 0			0 0		0 0			
$t_w(H)$ $t_w(L)$	CP Pulse Width HIGH or LOW	6.0 6.0			7.0 7.0		6.0 6.0		ns	3-7
$t_w(L)$	$\overline{MR}$ Width, LOW	6.0			6.5		6.0		ns	3-11
t_{rec}	Recovery Time, $\overline{MR}$ to CP	8.5			10.0		9.5		ns	3-11

54F/74F395

4-Bit Cascadable Shift Register With 3-State Outputs

Description

The 'F395 is a 4-bit Shift Register with serial and parallel synchronous operating modes and four 3-state buffer outputs. The shifting and loading operations are controlled by the state of the Parallel Enable (PE) input. When PE is HIGH, data is loaded from the Parallel Data inputs (D_0-D_3) into the register synchronous with the HIGH-to-LOW transition of the Clock input ($\overline{CP}$). When PE is LOW, the data at the Serial Data input (D_s) is loaded into the Q_0 flip-flop, and the data in the register is shifted one bit to the right in the direction (Q_0-Q_1-Q_2-Q_3) synchronous with the negative clock transition. The PE and Data inputs are fully edge-triggered and must be stable only one setup prior to the HIGH-to-LOW transition of the clock.

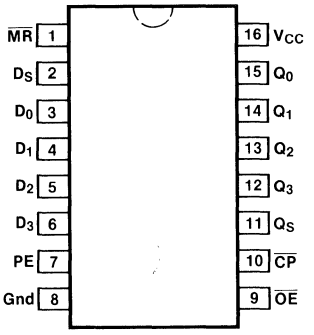
The Master Reset ($\overline{MR}$) is an asynchronous Active LOW input. When LOW, the $\overline{MR}$ overrides the clock and all other inputs and clears the register.

The 3-state output buffers are designed to drive heavily loaded 3-state buses, or large capacitive loads. The Active LOW Output Enable ($\overline{OE}$) controls all four 3-state buffers independent of the register operation. The data in the register appears at the outputs when $\overline{OE}$ is LOW. The outputs are in the high impedance (OFF) state, which means they will neither drive nor load the bus when $\overline{OE}$ is HIGH. The output from the last stage is brought out separately. This output (Q_s) is tied to the Serial Data input (D_s) of the next register for serial expansion applications. The Q_s output is not affected by the 3-state buffer operation.

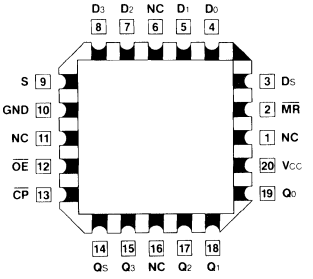
- **4-Bit Parallel Load Shift Register**
- **Independent 3-State Buffer Outputs**
- **Separate Q_s Output for Serial Expansion**
- **Asynchronous Master Reset**

Ordering Code: See Section 5

Connection Diagrams

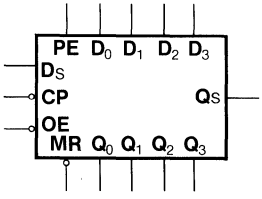


Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Logic Symbol



Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
D_0, D_1, D_2, D_3	Data Inputs	0.5/0.375
D_s	Serial Data Input	0.5/0.375
PE	Enable Input	0.5/0.375
$\overline{MR}$	Master Reset (Active LOW)	0.5/0.375
$\overline{OE}$	Output Enable (Active LOW)	0.5/0.375
$\overline{CP}$	Clock Pulse Input (Active Falling Edge)	0.5/0.375
Q_s	Serial Expansion Output	25/12.5
Q_0, Q_1, Q_2, Q_3	Data Outputs	75/15 (12.5)

Mode Select-Function Tables

Register Operating Modes	Inputs					Outputs			
	$\overline{MR}$	$\overline{CP}$	PE	D_s	D_n	Q_0	Q_1	Q_2	Q_3
Reset (clear)	L	X	X	X	X	L	L	L	L
Shift Right	H	↓	l	l	X	L	q_0	q_1	q_2
	H	↓	l	h	X	H	q_0	q_1	q_2
Parallel Load	H	↓	h	X	l	L	L	L	L
	H	↓	h	X	h	H	H	H	H

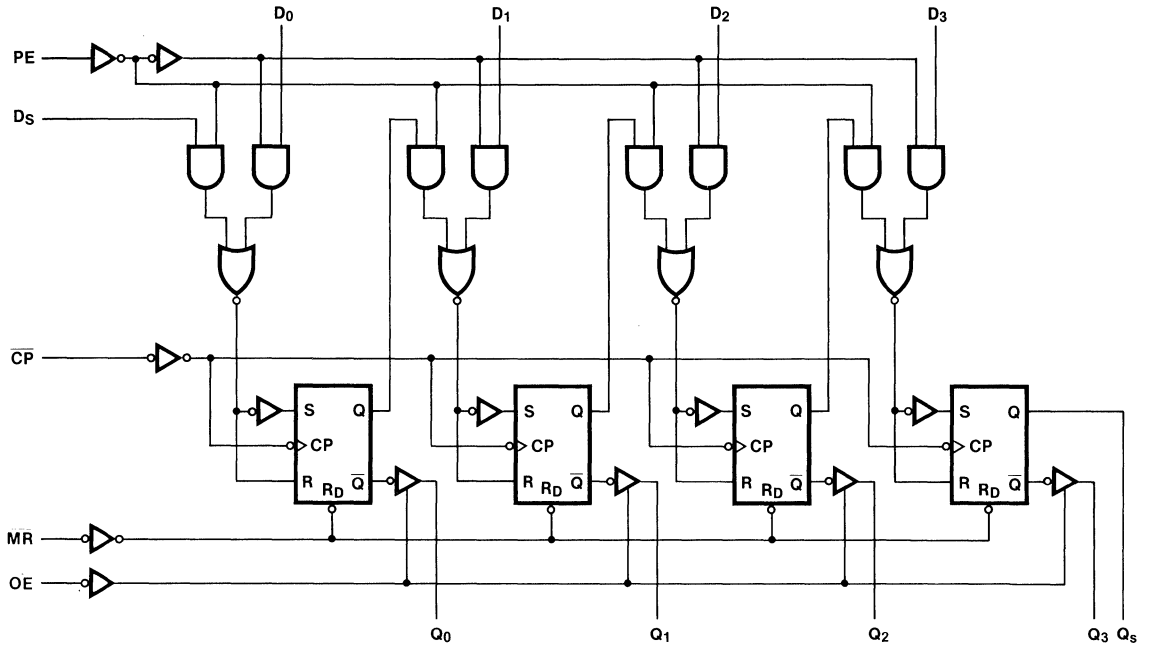
3-State Buffer Operating Modes	Inputs		Outputs	
	$\overline{OE}$	Q_n(Register)	Q_0, Q_1, Q_2, Q_3	Q_s
Read	L	L	L	L
	L	H	H	H
Disable Buffers	H	L	Z	L
	H	H	Z	H

H = HIGH Voltage Level
L = LOW Voltage Level
q_n = Lower case letters indicate the state of the referenced output one setup time prior to the HIGH-to-LOW Clock Transition
X = Immaterial
Z = High Impedance
↓ = HIGH-to-LOW transition

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current				mA	V_{CC} = Max

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$	T_A, V_{CC} = Mil $C_L = 50\ pF$	T_A, V_{CC} = Com $C_L = 50\ pF$		
		Min Typ Max	Min Max	Min Max		
f_{max}	Maximum Clock Frequency	105			MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay Clock to Buffer Outputs	7.0 7.0			ns	3-1 3-8
t_{PLH} t_{PHL}	Propagation Delay Clock to Q_s Output	7.0 7.0			ns	3-1 3-8
t_{PHL}	Propagation Delay $\overline{MR}$ to Output	12.0			ns	3-1 3-9
t_{PZH} t_{PZL}	Enable Time	11.5 7.5			ns	3-1, 3-12 3-13
t_{PHZ} t_{PLZ}	Disable Time	7.0 5.5			ns	3-1, 3-12 3-13

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW Data to Clock	4.0 4.0			ns	3-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW Data to Clock	0 0				
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW PE to Clock	8.0 8.0			ns	3-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW PE to Clock	0 0				
$t_w(H)$ $t_w(L)$	$\overline{CP}$ Pulse Width HIGH or LOW	5.0 5.0			ns	3-8
$t_w(H)$ $t_w(L)$	$\overline{MR}$ Pulse Width HIGH or LOW	5.0 5.0			ns	3-9
t_{rec}	Recovery Time, $\overline{MR}$ to Clock	7.0			ns	3-11

54F/74F398 • 54F/74F399

Quad 2-Port Register

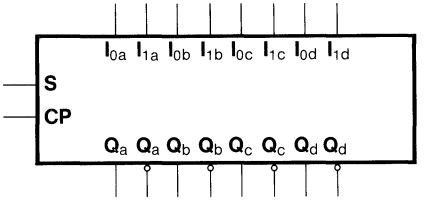
Description

The 'F398 and 'F399 are the logical equivalent of a quad 2-input multiplexer feeding into four edge-triggered flip-flops. A common Select input determines which of the two 4-bit words is accepted. The selected data enters the flip-flops on the rising edge of the clock. The 'F399 is the 16-pin version of the 'F398, with only the Q outputs of the flip-flops available.

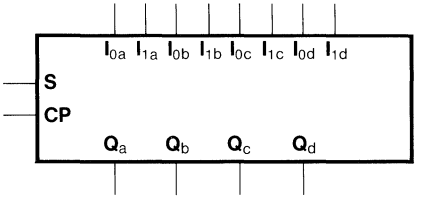
- **Select Inputs from Two Data Sources**
- **Fully Positive Edge-Triggered Operation**
- **Both True and Complement Outputs—'F398**

Ordering Code: See Section 5

Logic Symbols

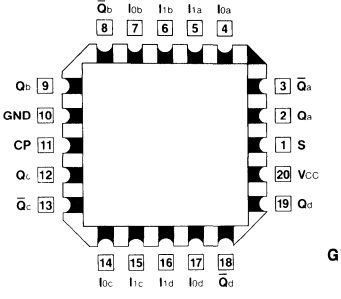


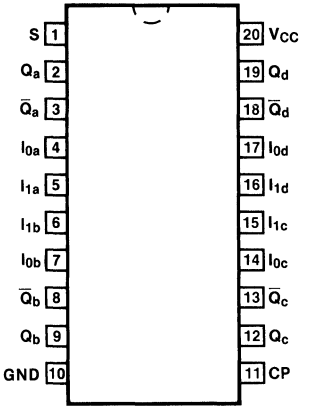
'F398



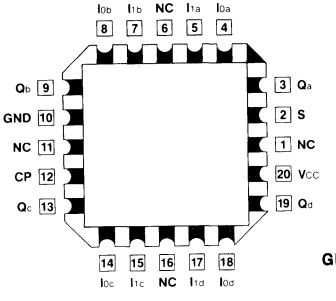
'F399

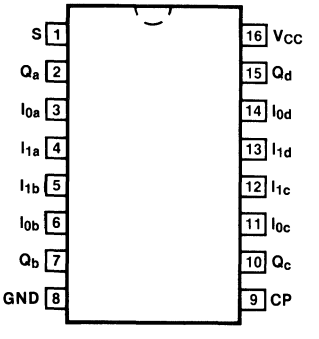
Connection Diagrams





'F398





'F399

Pin Assignment for LCC and PCC

Pin Assignment for DIP and SOIC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
S	Common Select Input	0.5/0.375
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
I_{0a}-I_{0d}	Data Inputs from Source 0	0.5/0.375
I_{1a}-I_{1d}	Data Inputs from Source 1	0.5/0.375
Q_a-Q_d	Register True Outputs	25/12.5
$\overline{Q}_a$-$\overline{Q}_d$	Register Complementary Outputs ('F398)	25/12.5

Functional Description

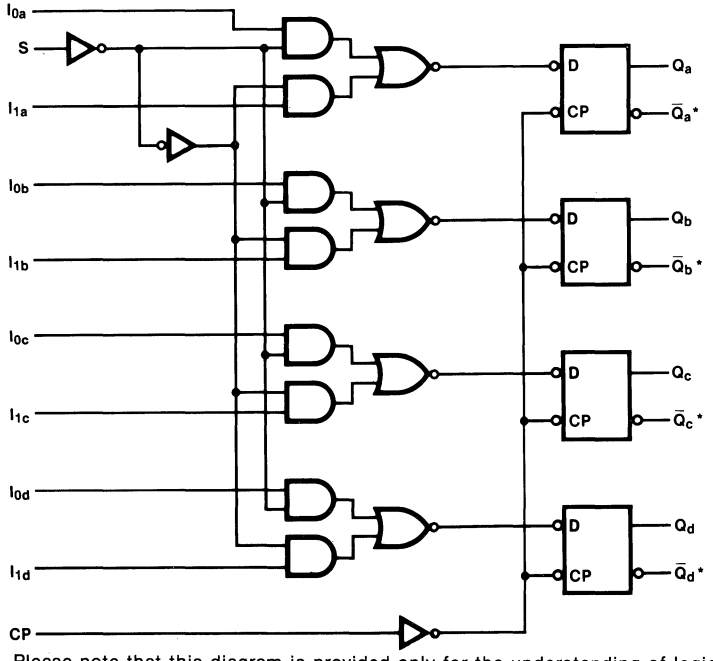
The 'F398 and 'F399 are high-speed quad 2-port registers. They select four bits of data from either of two sources (Ports) under control of a common Select input (S). The selected data is transferred to a 4-bit output register synchronous with the LOW-to-HIGH transition of the Clock input (CP). The 4-bit D-type output register is fully edge-triggered. The Data inputs (I_{0x}, I_{1x}) and Select input (S) must be stable only a setup time prior to and hold time after the LOW-to-HIGH transition of the Clock input for predictable operation. The 'F398 has both Q and $\overline{Q}$ outputs.

Function Table

Inputs			Outputs	
S	I_0	I_1	Q	$\overline{Q}$*
l	l	X	L	H
l	h	X	H	L
h	X	l	L	H
h	X	h	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH clock transition
l = LOW Voltage Level one setup time prior to the LOW-to-HIGH clock transition
X = Immaterial

Logic Diagram



* 'F398 only

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter		54F/74F Min	54F/74F Typ	54F/74F Max	Units	Conditions
I_{CC}	Power Supply Current	'F398		25	38		V_{CC} = Max, V_{IN} = Gnd
		'F399		22	34		CP = ⊓

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF Min	Typ	Max	54F T_A, V_{CC} = Mil, C_L = 50 pF Min	Max	74F T_A, V_{CC} = Com, C_L = 50 pF Min	Max	Units	Fig. No.
f_{max}	Input Clock Frequency	100	140		80		100		MHz	3-1
t_{PLH}	Propagation Delay	3.0	5.7	7.5	3.0	9.5	3.0	8.5	ns	3-1
t_{PHL}	CP to Q or $\overline{Q}$	3.0	6.8	9.5	3.0	11.5	3.0	10.0		3-7

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F T_A = +25°C, V_{CC} = +5.0 V Min	Typ	Max	54F T_A, V_{CC} = Mil Min	Max	74F T_A, V_{CC} = Com Min	Max	Units	Fig. No.
t_s(H)	Setup Time, HIGH or LOW	3.0			4.5		3.0		ns	3-1, 3-5
t_s(L)	I_n to CP	3.0			4.5		3.0			
t_h(H)	Hold Time, HIGH or LOW	1.0			1.5		1.0			
t_h(L)	I_n to CP	1.0			1.5		1.0			
t_s(H)	Setup Time, HIGH or LOW	7.5			10.5		8.5		ns	3-5
t_s(L)	S to CP ('F398)	7.5			10.5		8.5			
t_s(H)	Setup Time, HIGH or LOW	7.5			9.5		8.5			
t_s(L)	S to CP ('F399)	7.5			9.5		8.5			
t_h(H)	Hold Time, HIGH or LOW	0			0		0			
t_h(L)	S to CP	0			0		0			
t_w(H)	CP Pulse Width	4.0			4.0		4.0		ns	3-7
t_w(L)	HIGH or LOW	5.0			7.0		5.0			

54F/74F401

CRC Generator/Checker

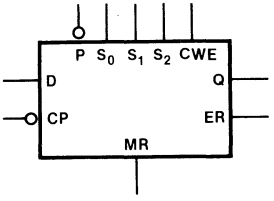
Description

The 'F401 Cycle Redundancy Check (CRC) Generator/Checker provides an advanced tool for implementing the most widely used error detection scheme in serial digital data handling systems. A 3-bit control input selects one-of-eight generator polynomials. The list of polynomials includes CRC-16 and CRC-CCITT as well as their reciprocals (reverse polynomials). Automatic right justification is incorporated for polynomials of degree less than 16. Separate clear and preset inputs are provided for floppy disk and other applications. The Error output indicates whether or not a transmission error has occurred. Another control input inhibits feedback during check word transmission. The 'F401 is fully compatible with all TTL families.

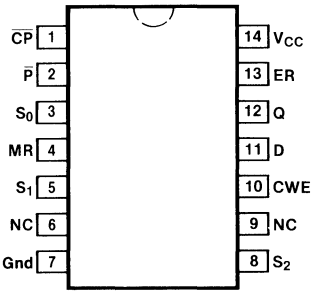
- **Eight Selectable Polynomials**
- **Error Indicator**
- **Separate Preset and Clear Controls**
- **Automatic Right Justification**
- **Fully Compatible with all TTL Logic Families**
- **14-Pin Package**
- **9401 Equivalent**
- **Typical Applications:**
  - **Floppy and Other Disk Storage Systems**
  - **Digital Cassette and Cartridge Systems**
  - **Data Communication Systems**

Ordering Code: See Section 5

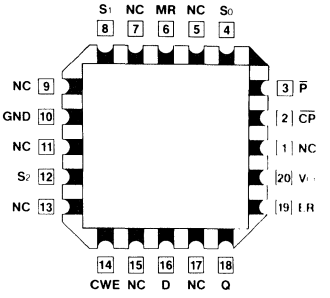
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC

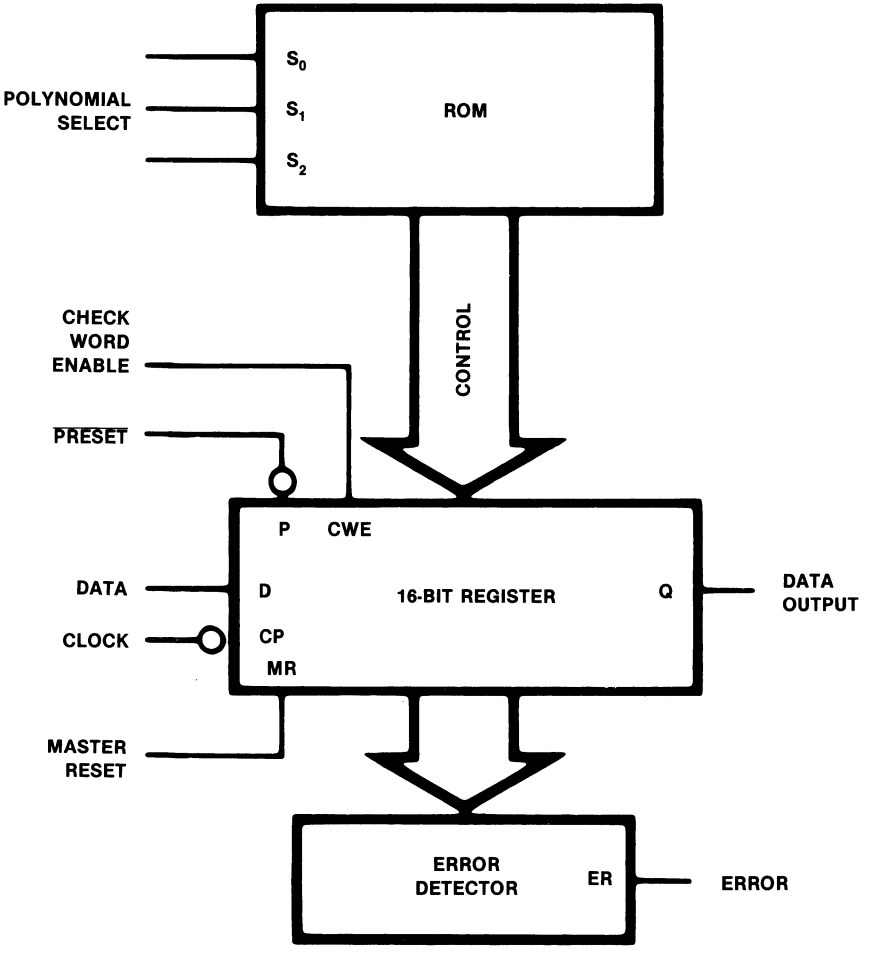


Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
S_0-S_2	Polynomial Select Inputs	0.5/0.375
D	Data Input	0.5/0.375
$\overline{CP}$	Clock Input (Operates on HIGH-to-LOW Transition)	0.5/0.375
CWE	Check Word Enable Input	0.5/0.375
$\overline{P}$	Preset (Active LOW) Input	0.5/0.375
MR	Master Reset (Active HIGH) Input	0.5/0.375
Q	Data Output	25/12.5
ER	Error Output	25/12.5

Block Diagram



Functional Description

The 'F401 is a 16-bit programmable device which operates on serial data streams and provides a means of detecting transmission errors. Cyclic encoding and decoding schemes for error detection are based on polynomial manipulation in modulo arithmetic. For encoding, the data stream (message polynomial) is divided by a selected polynomial. This division results in a remainder which is appended to the message as check bits. For error checking, the bit stream containing both data and check bits is divided by the same selected polynomial. If there are no detectable errors, this division results in a zero remainder. Although it is possible to choose many generating polynomials of a given degree, standards exist that specify a small number of useful polynomials. The 'F401 implements the polynomials listed in Table 1 by applying the appropriate logic levels to the select pins S_0, S_1 and S_2.

The 'F401 consists of a 16-bit register, a Read Only Memory (ROM) and associated control circuitry as shown in the block diagram. The polynomial control code presented at inputs S_0, S_1 and S_2 is decoded by the ROM, selecting the desired polynomial by establishing shift mode operation on the register with Exclusive OR gates at appropriate inputs. To generate the check bits, the data stream is entered via the Data inputs (D), using the HIGH-to-LOW transition of the Clock input ($\overline{CP}$). This data is gated with the most significant output (Q) of the register, and controls the Exclusive OR gates (Figure 1). The Check Word Enable (CWE) must be held HIGH while the data is being entered. After the last data bit is entered, the CWE is brought LOW and the check bits are shifted out of the register and appended to the data bits using external gating (Figure 2).

To check an incoming message for errors, both the data and check bits are entered through the D input with the CWE input held HIGH. The 'F401 is not in the data path, but only monitors the message. The Error Output becomes valid after the last check bit has been entered into the 'F401 by a HIGH-to-LOW transition of $\overline{CP}$. If no detectable errors have occurred during the data transmission, the resultant internal register bits are all LOW and the Error Output (ER) is LOW. If a detectable error has occurred, ER is HIGH.

A HIGH on the Master Reset input (MR) asynchronously clears the register. A LOW on the Preset input ($\overline{P}$) asynchronously sets the entire register if the control code inputs specify a 16-bit polynomial; in the case of 12 or 8-bit check polynomials only the most significant 12 or 8 register bits are set and the remaining bits are cleared.

Table 1

Select Code			Polynomial	Remarks
S_2	S_1	S_0		
L	L	L	$X^{16}+X^{15}+X^2+1$	CRC-16
L	L	H	$X^{16}+X^{14}+X+1$	CRC-16 REVERSE
L	H	L	$X^{16}+X^{15}+X^{13}+X^7+X^4+X^2+X^1+1$	
L	H	H	$X^{12}+X^{11}+X^3+X^2+X+1$	CRC-12
H	L	L	$X^8+X^7+X^5+X^4+X+1$	
H	L	H	X^8+1	LRC-8
H	H	L	$X^{16}+X^{12}+X^5+1$	CRC-CCITT
H	H	H	$X^{16}+X^{11}+X^4+1$	CRC-CCITT REVERSE

Fig. 1 Equivalent Circuit for $X^{16} + X^{15} + X^2 + 1$

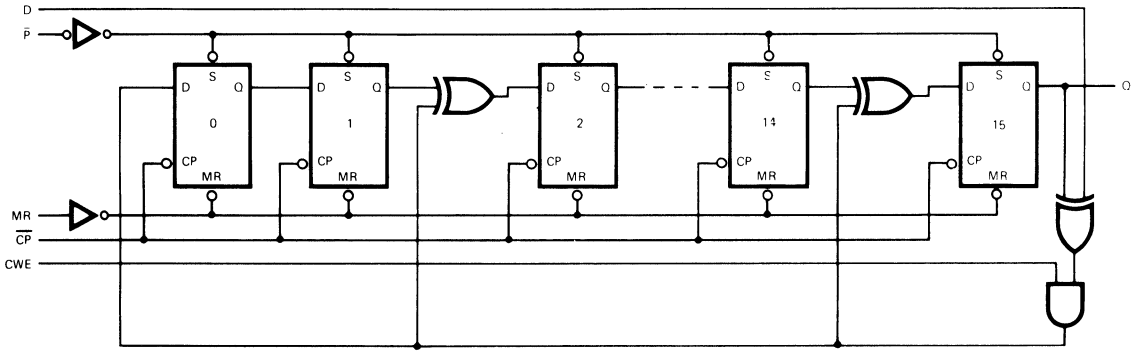
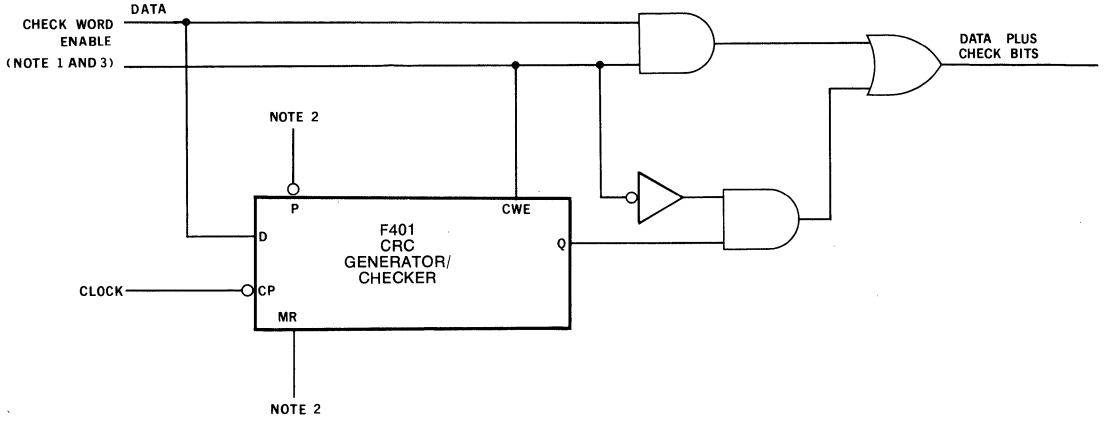


Fig. 2 Check Word Generation



NOTES:
1. Check word Enable is HIGH while data is being clocked, LOW while transmission of check bits.
2. 'F401 must be reset or preset before each computation.
3. CRC check bits are generated and appended to data bits.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		70	110	mA	V_{CC} = Max, Inputs Open

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF	T_A, V_{CC} = Mil, C_L = 50 pF	T_A, V_{CC} = Com, C_L = 50 pF		
		Min Typ Max	Min Max	Min Max		
f_{max}	Maximum Clock Frequency	70			MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to Q	15.0 15.0			ns	3-1 3-8
t_{PHL}	Propagation Delay MR to Q	11.0			ns	3-1 3-11
t_{PLH}	Propagation Delay $\overline{P}$ to ER	12.0			ns	3-1 3-11
t_{PLH}	Propagation Delay $\overline{P}$ to Q	12.0			ns	3-1 3-11
t_{PHL}	Propagation Delay MR to ER	15.0			ns	3-1 3-11
t_{PLH}	Propagation Delay $\overline{P}$ to ER	15.0			ns	3-1 3-11
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to ER	15.0 15.0			ns	3-1 3-8

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$ $t_s(L)$	Set-up Time, HIGH or LOW D to $\overline{CP}$	5.0 5.0			ns	3-6
$t_s(H)$ $t_s(L)$	Set-up Time, HIGH or LOW CWE to $\overline{CP}$	5.0 5.0				
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D and CWE to $\overline{CP}$	0 0				
$t_w(L)$	$\overline{P}$ Pulse Width, LOW	9.0			ns	3-9
$t_w(L)$	Clock Pulse Width, LOW	10.0			ns	3-8
$t_w(H)$	MR Pulse Width, HIGH	9.0			ns	3-11
t_{rec}	Recovery Time MR to $\overline{CP}$	10.0			ns	3-11
t_{rec}	Recovery Time $\overline{P}$ to $\overline{CP}$	10.0			ns	3-11

54F/74F402

Serial Data Polynomial Generator/Checker

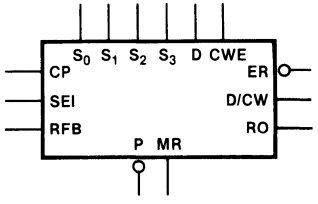
Description

The 'F402 expandable Serial Data Polynomial generator/checker is an expandable version of the 'F401. It provides an advanced tool for the implementation of the most widely used error detection scheme in serial digital handling systems. A 4-bit control input selects one-of-six generator polynomials. The list of polynomials includes CRC-16, CRC-CCITT and Ethernet, as well as three other standard polynomials (56th order, 48th order, 32nd order). Individual clear and preset inputs are provided for floppy disk and other applications. The Error output indicates whether or not a transmission error has occurred. The CWG Control input inhibits feedback during check word transmission. The 'F402 is compatible with Fairchild Advanced Schottky TTL (FAST) devices and is fully compatible with all TTL families.

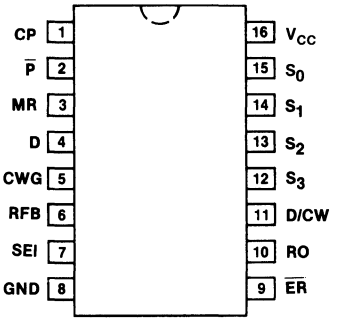
- **Guaranteed 30 MHz Data Rate**
- **Six Selectable Polynomials**
- **Other Polynomials Available**
- **Separate Preset and Clear Controls**
- **Expandable**
- **Automatic Right Justification**
- **Error Output Open Collector**
- **Typical Applications**
  - **Floppy and Other Disk Storage Systems**
  - **Digital Cassette and Cartridge Systems**
  - **Data Communication Systems**

Ordering Code: See Section 5

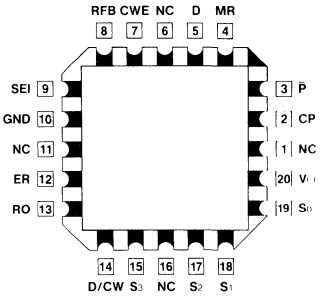
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

4

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
S_0-S_3	Polynomial Select Inputs	0.5/0.25
CWG	Check Word Generate Input	0.5/0.25
D/CW	Serial Data/Check Word	10/5(2.5)
D	Data Input	0.5/0.25
$\overline{ER}$	Error Output	*/10(5)
RO	Register Output	10/5(2.5)
CP	Clock Pulse	0.5/0.25
SEI	Serial Expansion Input	0.5/0.25
RFB	Register Feedback	0.5/0.25
MR	Master Reset	0.5/0.25
$\overline{P}$	Preset	0.5/0.25

*Open Collector

Functional Description

The 'F402 Serial Data Polynomial Generator/ Checker is an expandable 16-bit programmable device which operates on serial data streams and provides a means of detecting transmission errors. Cyclic encoding and decoding schemes for error detection are based on polynomial manipulation in modulo arithmetic. For encoding, the data stream (message polynomial) is divided by a selected polynomial. This division results in a remainder (or residue) which is appended to the message as check bits. For error checking, the bit stream containing both data and check bits is divided by the same selected polynomial. If there are no detectable errors, this division results in a zero remainder. Although it is possible to choose many generating polynomials of a given degree, standards exist that specify a small number of useful polynomials. The 'F402 implements the polynomials listed in Table 1 by applying the appropriate logic levels to the select pins S_0, S_1, S_2, and S_3.

The 'F402 consists of a 16-bit register, a Read Only Memory (ROM) and associated control circuitry as shown in the Block Diagram. The polynomial control code presented at inputs S_0, S_1, S_2, and S_3 is decoded by the ROM, selecting the desired polynomial or part of a polynomial by establishing shift mode operation on the register with Exclusive OR (XOR) gates at appropriate inputs. To generate the check bits, the data stream is entered via the Data Inputs (D), using the LOW-to-HIGH transition of the Clock Input (CP). This data is gated with the most significant Register Output (RO) via the Register Feedback Input (RFB), and controls the XOR gates. The Check Word Generate (CWG) must be held HIGH while the data is being entered. After the last data bit is entered, the CWG is brought LOW and the check bits are shifted out of the register(s) and appended to the data bits (no external gating is needed).

To check an incoming message for errors, both the data and check bits are entered through the D Input with the CWG Input held HIGH. The Error Output becomes valid after the last check bit has been entered into the 'F402 by a LOW-to-HIGH transition of CP, with the exception of the Ethernet polynomial (see Applications paragraph). If no detectable errors have occurred during the data transmission, the resultant internal register bits are all LOW and the Error Output ($\overline{ER}$) is HIGH. If a detectable error has occurred, $\overline{ER}$ is LOW. $\overline{ER}$ remains valid until the next LOW-to-HIGH transition of CP or until the device has been preset or reset.

A HIGH on the Master Reset Input (MR) asynchronously clears the entire register. A LOW on the Preset Input ($\overline{P}$) asynchronously sets the entire register with the exception of:

1) The Ethernet residue selection, in which the registers containing the non-zero residue are cleared;
2) The 56th order polynomial, in which the 8 least significant register bits of the least significant device are cleared; and,
3) Register S = 0, in which all bits are cleared.

Block Diagram

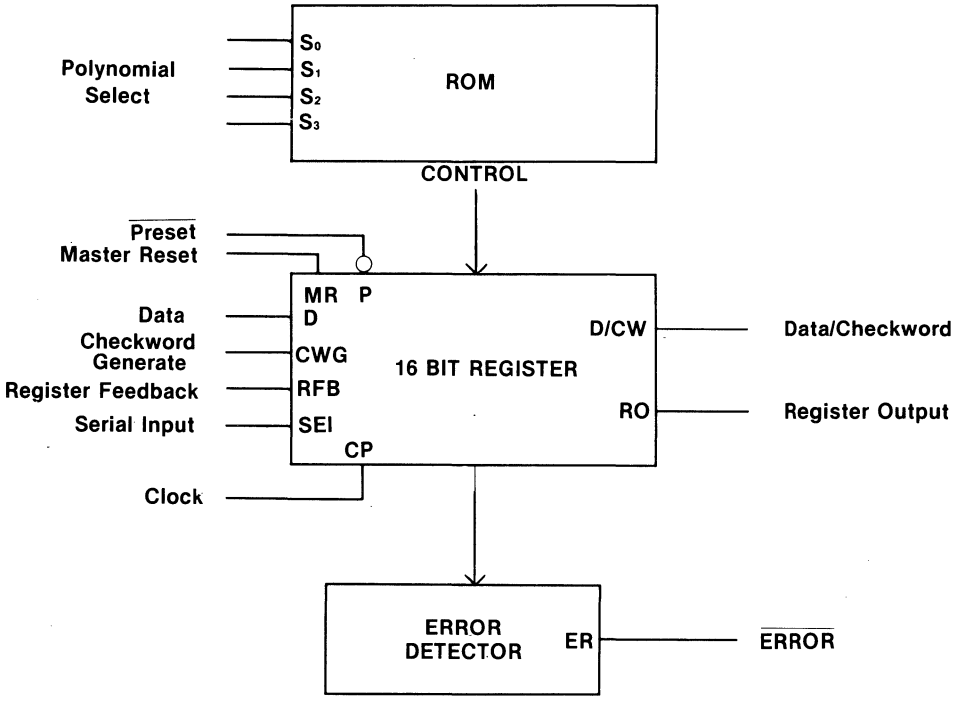


Table 1

Hex	Select Code S_3	S_2	S_1	S_0	Polynomial	Remarks
0	L	L	L	L	0	S = 0
C D	H H	H H	L L	L H	$X^{32}+X^{26}+X^{23}+X^{22}+X^{16}+$ $X^{12}+X^{11}+X^{10}+X^8+X^7+X^5+X^4+X^2+X+1$	Ethernet Polynomial
E F	H H	H H	H H	L H	$X^{32}+X^{31}+X^{27}+X^{26}+X^{25}+X^{19}+X^{16}+$ $X^{15}+X^{13}+X^{12}+X^{11}+X^9+X^7+X^6+X^5+X^4+X^2+X+1$	Ethernet Residue
7	L	H	H	H	$X^{16}+X^{15}+X^2+1$	CRC-16
B	H	L	H	H	$X^{16}+X^{12}+X^{12}+X^5+1$	CRC-CCITT
3 2 4 8	L L L H	L L H L	H H L L	H L L L	$X^{56}+X^{55}+X^{49}+X^{45}+X^{41}+$ $X^{39}+X^{38}+X^{37}+X^{36}+X^{31}+$ $X^{22}+X^{19}+X^{17}+X^{16}+X^{15}+X^{14}+X^{11}+X^9+$ X^5+X+1	56th Order
5 9 1	L H L	H L L	L L L	H H H	$X^{48}+X^{36}+X^{35}+$ $X^{23}+X^{21}+$ $X^{15}+X^{13}+X^8+X^2+1$	48th Order
6 A	L H	H L	H H	L L	$X^{32}+X^{23}+X^{21}+$ $X^{11}+X^2+1$	32nd Order

Table 2

Select Code	P_3	P_2	P_1	P_0	C_2	C_1	C_0	Polynomial
0	0	0	0	0	1	0	0	S = 0
C D	1 1	1 1	1 1	1 1	1 1	0 0	1 1	Ethernet Polynomial
E F	0 0	0 0	0 0	0 0	0 0	0 1	0 0	Ethernet Residue
7	1	1	1	1	1	0	0	CRC-16
B	1	1	1	1	1	0	0	CRC-CCITT
3 2 4 8	1 1 1 0	1 1 1 0	1 1 1 1	1 1 1 1	1 1 1 1	0 0 0 0	0 0 0 0	56th Order
5 9 1	1 1 1	1 1 1	1 1 1	1 1 1	1 1 1	0 0 0	0 0 0	48th Order
6 A	1 1	1 1	1 1	1 1	1 1	0 0	0 0	32nd Order

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		110	165	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			54F T_A, V_{CC} = Mil C_L = 50 pF		74F T_A, V_{CC} = Com C_L = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	30	45				30		MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay CP to D/CW	8.5 10.5	15.0 18.0	19.0 23.0			9.5 9.0	21.0 24.0	ns	3-1 3-7
t_{PLH} t_{PHL}	Propagation Delay CP to RO	8.0 8.0	13.5 14.0	17.0 18.0			7.0 7.0	19.0 20.0	ns	3-1 3-7
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{ER}$	15.5 8.5	26.0 14.5	33.0 18.5			13.5 7.5	35.0 20.5	ns	3-1 3-7
t_{PLH} t_{PHL}	Propagation Delay $\overline{P}$ to D/CW	11.0 11.5	18.5 19.5	23.5 24.5			9.5 10.0	25.5 26.5	ns	3-1 3-8
t_{PLH}	Propagation Delay $\overline{P}$ to RO	9.5	16.0	20.5			8.5	22.5	ns	3-1 3-8
t_{PLH}	Propagation Delay $\overline{P}$ to $\overline{ER}$	10.0	17.0	21.5			9.0	23.5	ns	3-1 3-8
t_{PLH} t_{PHL}	Propatation Delay MR to D/CW	10.5 11.0	18.0 19.0	23.0 24.0			9.5 10.0	25.0 26.0	ns	3-1 3-11
t_{PHL}	Propagation Delay MR to RO	9.0	15.5	19.5			8.0	21.5	ns	3-1 3-11
t_{PLH}	Propagation Delay MR to $\overline{ER}$	16.5	28.0	35.5			14.5	37.5	ns	3-1 3-11
t_{PLH} t_{PHL}	Propagation Delay D to D/CW	6.0 7.5	10.5 12.0	13.5 16.0			5.0 6.5	15.0 18.0	ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay CWG to D/CW	6.5 7.0	11.0 12.0	14.0 15.5			5.5 6.0	15.5 17.5	ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay S_n to D/CW	11.5 9.5	19.5 16.0	24.5 20.0			10.5 8.5	26.5 22.0	ns	3-1 3-4

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$ $t_s(L)$	Set up Time, HIGH or LOW SEI to CP	4.5 4.5		5.0 5.0	ns	3-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW SEI to CP	0 0		0 0		
$t_s(H)$ $t_s(L)$	Set up Time, HIGH or LOW RFB to CP	11.0 11.0		12.0 12.0	ns	3-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW RFB to CP	0 0		0 0		
$t_s(H)$ $t_s(L)$	Set up Time, HIGH or LOW S_1 to CP	13.5 13.0		15.0 14.5	ns	3-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW S_1 to CP	0 0		0 0		
$t_s(H)$ $t_s(L)$	Set up Time, HIGH or LOW D to CP	9.0 9.0		10.0 10.0	ns	3-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D to CP	0 0		0 0		
$t_s(H)$ $t_s(L)$	Set up Time, HIGH or LOW CWG to CP	7.0 5.5		8.0 6.5	ns	3-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW CWG to CP	0 0		0 0		
$t_w(H)$ $t_w(L)$	Clock Pulse Width HIGH or LOW	4.0 4.0		4.5 4.5	ns	3-7
$t_w(H)$	MR Pulse Width, HIGH	4.0		4.5	ns	3-11
$t_w(L)$	$\overline{P}$ Pulse Width, LOW	4.0		4.5	ns	3-11
t_{rec}	Recovery Time MR to CP	3.0		2.5	ns	3-6
t_{rec}	Recovery Time $\overline{P}$ to CP	5.0		6.0		

Applications

In addition to polynomial selection there are four other capabilities provided for in the 'F402 ROM. The first is set or clear selectability. The sixteen internal registers have the capability to be either set or cleared when $\overline{P}$ is brought LOW. This set or clear capability is done in four groups of 4 (see Table 2, P_0-P_3). The second ROM capability (C_0) is in determining the polarity of the check word. As is the case with the Ethernet polynomial the check word can be inverted when it is appended to the data stream or as is the case with the other polynomials, the residue is appended with no inversion. Thirdly, the ROM contains a bit (C_1) which is used to select the RFB input instead of the SEI input to be fed into the LSB. This is used when the polynomial selected is actually a residue (least significant) stored in the ROM which indicates whether the selected location is a polynomial or a residue. If the latter, then it inhibits the RFB input.

As mentioned previously, upon a successful data transmission, the CRC register has a zero residue. There is an exception to this, however, with respect to the Ethernet polynomial. This polynomial, upon a successful data transmission, has a non-zero residue in the CRC register (C7 04 DD $7B)_{16}$. In order to provide a no-error indication, two ROM locations have been preloaded with the residue so that by selecting these locations and clocking the device one additional time, after the last check bit has been entered, will result in zeroing the CRC register. In this manner a no-error indication is achieved.

With the present mix of polynomials, the largest is 56^{th} order requiring four devices while the smallest is 16^{th} order requiring just one device. In order to accommodate multiplexing between high order polynomials (X 16^{th} order) and lower order polynomials, a location of all zeros is provided. This allows the user to choose a lower order polynomial even if the system is configured for a higher order one.

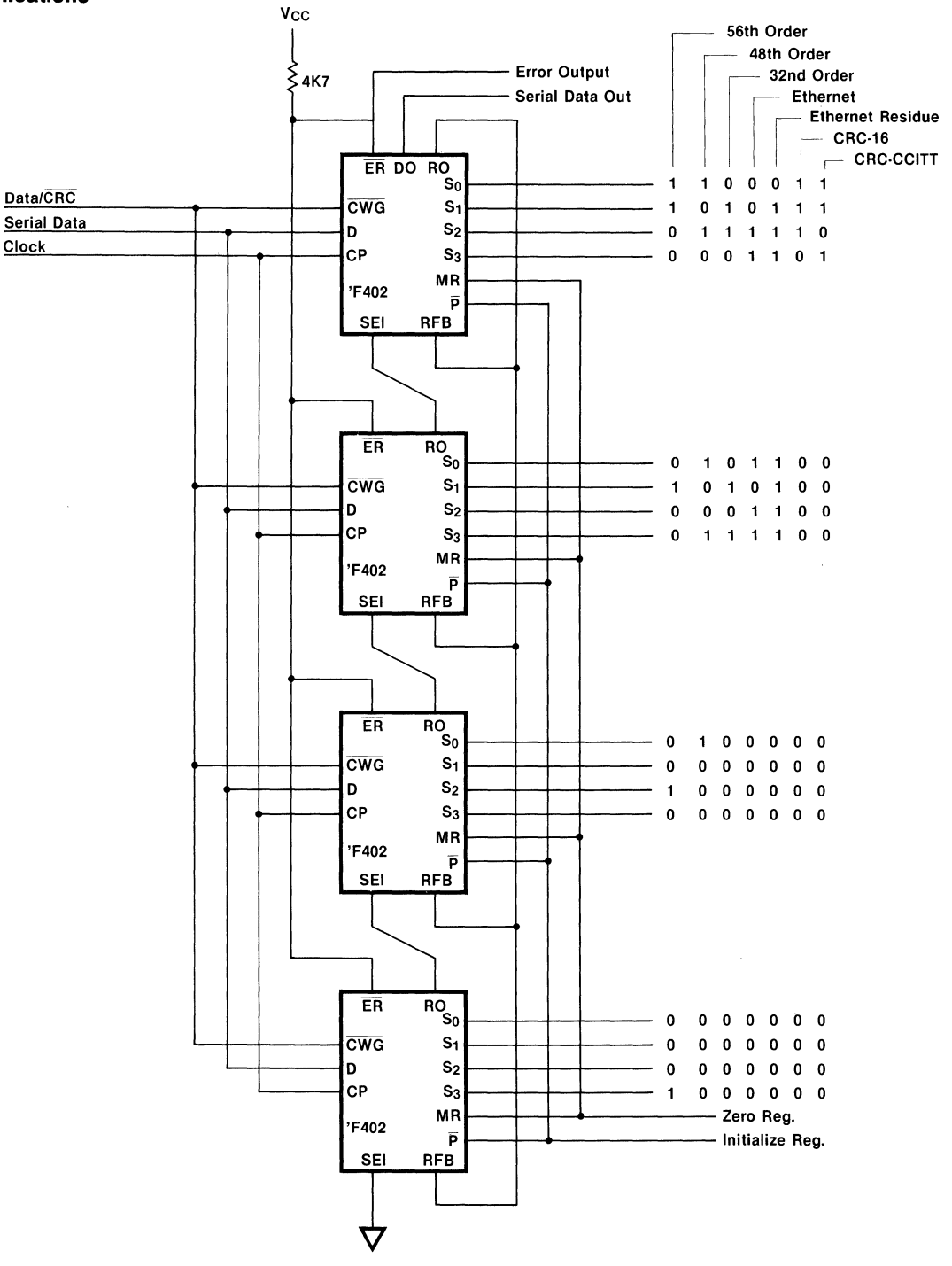
The 'F402 expandable CRC generator checker contains 6 popular CRC polynomials, 2-16^{th} Order, 2-32^{nd} Order, 1-48^{th} Order and 1-56^{th} Order. The application diagram shows the 'F402 connected for a 56^{th} Order polynomial. Also shown are the input patterns for other polynomials. When the 'F402 is used with a gated clock, disabling the clock in a HIGH state will ensure no erroneous clocking occurs when the clock is re-enabled. Preset and Master Reset are asynchronous inputs presetting the register to S or clearing to 0s respectively (note Ethernet residue and 56^{th} Order select code 8, LSB, are exceptions to this).

To generate a CRC, the pattern for the selected polynomial is applied to the S inputs, the register is preset or cleared as required, clock is enabled, CWG is set HIGH, data is applied to D input, output data is on D/CW. When the last data bit has been entered, CWG is set LOW and the register is clocked for n bits (where n is the order of the polynomial). The clock may now be stopped if desired (holding CWG LOW and clocking the register will output zeros from D/CW after the residue has been shifted out).

To check a CRC, the pattern for the selected polynomial is applied to the S inputs, the register is preset or cleared as required, clock is enabled, CWG is set HIGH, the data stream including the CRC is applied to D input. When the last bit of the CRC has been entered, the $\overline{ER}$ output is checked: HIGH = error free data, LOW = corrupt data. The clock may now be stopped if desired.

To implement polynomials of lower order than 56^{th}, select the number of packages required for the order of polynomial and apply the pattern for the selected polynomial to the S inputs (0000 on S inputs disables the package from the feedback chain).

Applications



54F/74F403

First-In First-Out (FIFO) Buffer Memory

Description

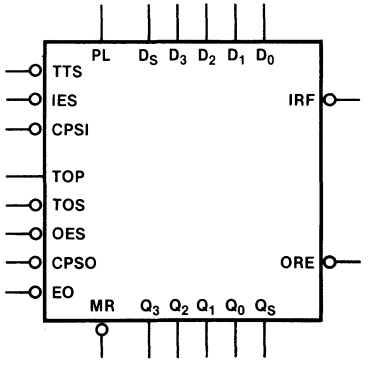
The 'F403 is an expandable fall-through type high-speed First-In First-Out (FIFO) Buffer Memory optimized for high-speed disk or tape controllers and communication buffer applications. It is organized as 16-words by 4-bits and may be expanded to any number of words or any number of bits in multiples of four. Data may be entered or extracted asynchronously in serial or parallel, allowing economical implementation of buffer memories.

The 'F403 has 3-state outputs which provide added versatility and is fully compatible with all TTL families.

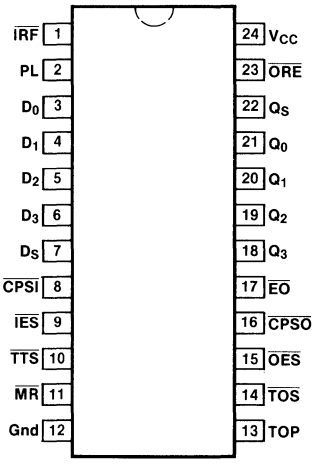
- **Serial or Parallel Input**
- **Serial or Parallel Output**
- **Expandable without External Logic**
- **3-State Outputs**
- **Fully Compatible with all TTL Families**
- **Slim 24-Pin Package**

Ordering Code: See Section 5

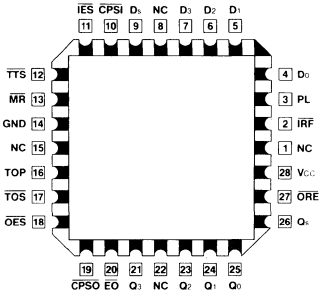
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
D_0-D_3	Parallel Data Inputs	1.0/0.23
D_S	Serial Data Input	1.0/0.23
PL	Parallel Load Input	1.0/0.23
$\overline{CPSI}$	Serial Input Clock	1.0/0.23
$\overline{IES}$	Serial Input Enable	1.0/0.23
$\overline{TTS}$	Transfer to Stack Input	1.0/0.23
$\overline{OES}$	Serial Output Enable	1.0/0.6
$\overline{TOS}$	Transfer Out Serial	1.0/0.23
TOP	Transfer Out Parallel	1.0/0.23
$\overline{MR}$	Master Reset	1.0/0.23
$\overline{OE}$	Output Enable	1.0/0.23
$\overline{CPSO}$	Serial Output Clock	1.0/0.23
Q_0-Q_3	Parallel Data Outputs	130/10
Q_S	Serial Data Output	10/10
$\overline{IRF}$	Input Register Full	10/5
$\overline{ORE}$	Output Register Empty	10/5

Functional Description

As shown in the block diagram the 'F403 consists of three sections:

1. An Input Register with parallel and serial data inputs as well as control inputs and outputs for input handshaking and expansion.
2. A 4-bit wide, 14-word deep fall-through stack with self-contained control logic.
3. An Output Register with parallel and serial data outputs as well as control inputs and outputs for output handshaking and expansion.

Since these three sections operate asynchronously and almost independently, they will be described separately below.

Input Register (Data Entry)

The Input Register can receive data in either bit-serial or in 4-bit parallel firm. It stores this data until it is sent to the fall-through stack and generates the necessary status and control signals.

Figure 1 is a conceptual logic diagram of the input section. As described later, this 5-bit register is initialized by setting the F_3 flip-flop and resetting the other flip-flops. The Q-output of the last flip-flop (FC) is brought out as the 'Input Register Full' output ($\overline{IRF}$). After initialization this output is HIGH.

Parallel Entry—A HIGH on the PL input loads the D_0-D_3 inputs into the F_0-F_3 flip-flops and sets the FC flip-flop. This forces the $\overline{IRF}$ output LOW indicating that the input register is full. During parallel entry, the $\overline{CPSI}$ input must be LOW. If parallel expansion is not being implemented, $\overline{IES}$ must be LOW to establish row mastership (see Expansion section).

Serial Entry—Data on the D_S input is serially entered into the F_3, F_2, F_1, F_0, FC shift register on each HIGH-to-LOW transition of the $\overline{CPSI}$ clock input, provided $\overline{IES}$ and PL are LOW.

After the fourth clock transition, the four data bits located in the four flip-flops, F_0-F_3. The FC flip-flop is set, forcing the $\overline{IRF}$ output LOW and internally inhibiting $\overline{CPSI}$ clock pulses from affecting the register, Figure 2 illustrates the final positions in a 'F403 resulting from a 64-bit serial bit train. B_0 is the first bit, B_{63} the last bit.

Transfer to the Stack—The outputs of Flip-Flops F_0-F_3 feed the stack. A LOW level on the $\overline{TTS}$ input initiates a 'fall-through' action. If the top location of the stack is empty, data is loaded into the stack and the input register is re-initialized. Note that this initialization is postponed until PL is LOW again. Thus, automatic FIFO action is achieved by connecting the $\overline{IRF}$ output to the $\overline{TTS}$ input.

An RS Flip-Flop (the Request Initialization Flip-Flop shown in Figure 10) in the control section records the fact that data has been transferred to the stack. This prevents multiple entry of the same word into the stack despite the fact the $\overline{IRF}$ and $\overline{TTS}$ may still be LOW. The Request Initialization Flip-Flop is not cleared until PL goes LOW. Once in the stack, data falls through the stack automatically, pausing only when it is necessary to wait for an empty next location. In the 'F403 as in most modern FIFO designs, the $\overline{MR}$ input only initializes the stack control section and does not clear the data.

Output Register (Data Extraction)

The Output Register receives 4-bit data words from the bottom stack location, stores it and outputs data on a 3-state 4-bit parallel data bus or on a 3-state serial data bus. The output section generates and receives the necessary status and control signals. Figure 3 is a conceptual logic diagram of the output section.

Parallel Data Extraction—When the FIFO is empty after a LOW pulse is applied to $\overline{MR}$, the Output Register Empty ($\overline{ORE}$) output is LOW. After data has been entered into the FIFO and has fallen through to the bottom stack location, it is transferred into the Output Register provided the 'Transfer Out Parallel' (TOP) input is HIGH. As a result of the data transfer $\overline{ORE}$ goes HIGH, indicating valid data on the data outputs (provided the 3-state buffer is enabled). TOP can now be used to clock out the next word. When TOP goes LOW, $\overline{ORE}$ will go LOW indicating that the output data has been extracted, but the data itself remains on the output bus until the next HIGH level at TOP permits the transfer of the next word (if available) into the Output Register. During parallel data extraction $\overline{CPSO}$ should be LOW. TOS should be grounded for single slice operation or connected to the appropriate $\overline{ORE}$ for expanded operation (see Expansion section).

TOP is not edge triggered. Therefore, if TOP goes HIGH before data is available from the stack, but data does become available before TOP goes LOW again, that data will be transferred into the Output Register. However, internal control circuitry prevents the same data from being transferred twice. If TOP goes HIGH and returns to LOW before data is available from the stack, $\overline{ORE}$ remains LOW indicating that there is no valid data at the outputs.

Serial Data Extraction—When the FIFO is empty after a LOW pulse is applied to $\overline{MR}$, the Output Register Empty ($\overline{ORE}$) output is LOW. After data has been entered into the FIFO and has fallen through to the bottom stack location, it is transferred into the Output Register provided $\overline{TOS}$ is LOW and TOP is HIGH. As a result of the data transfer $\overline{ORE}$ goes HIGH indicating valid data in the register. The 3-state Serial Data Output, Q_S, is automatically enabled and puts the first data bit on the output bus. Data is serially shifted out on the HIGH-to-LOW transition of $\overline{CPSO}$. To prevent false shifting, $\overline{CPSO}$ should be LOW when the new word is being loaded into the Output Register. The fourth transition empties the shift register, forces $\overline{ORE}$ output LOW and disables the serial output, Q_S (refer to Figure 3). For serial operation the $\overline{ORE}$ output may be tied to the $\overline{TOS}$ input, requesting a new word from the stack as soon as the previous one has been shifted out.

Expansion

Vertical Expansion—The 'F403 may be vertically expanded to store more words without external parts. The interconnections necessary to form a 46-word by 4-bit FIFO are shown in Figure 4. Using the same technique, and FIFO of (15n + 1)-words by 4-bits can be constructed, where n is the number of devices. Note that expansion does not sacrifice any of the 'F403's flexibility for serial/parallel input and output.

Horizontal and Vertical Expansion—The 'F403 can be expanded in both the horizontal and vertical directions without any external parts and without sacrificing any of its FIFO's flexibility for serial/parallel input and output. The interconnections necessary to form a 31-word by 16-bit FIFO are shown in Figure 6. Using the same technique, any FIFO of (15m + 1)-words by (4n)-bits can be constructed, where m is the number of devices in a column and n is the number of devices in a row. Figures 7 and 8 show the timing diagrams for serial data entry and extraction for the 31-word by 16-bit FIFO shown in Figure 6. The final position of data after serial insertion of 496 bits into the FIFO array of Figure 6 is shown in Figure 9.

Interlocking Circuitry—Most conventional FIFO designs provide status signals analogous to $\overline{IRF}$ and $\overline{ORE}$. However, when these devices are operated in arrays, variations in unit to unit operating speed require external gating to assure all devices have completed an operation. The 'F403 incorporates simple but effective 'master/slave' interlocking circuitry to eliminate the need for external gating.

In the 'F403 array of Figure 6 devices 1 and 5 are defined as 'row masters' and the other devices are slaves to the master in their row. No slave in a given row will initialize its Input Register until it has received LOW on its $\overline{IES}$ input from a row master or a slave of higher priority.

In a similar fashion, the $\overline{ORE}$ outputs of slaves will not go HIGH until their $\overline{OES}$ inputs have gone HIGH. This interlocking scheme ensures that new input data may be accepted by the array when the $\overline{IRF}$ output of the final slave in that row goes LOW and that output data for the array may be extracted when the $\overline{ORE}$ of the final slave in the output row goes HIGH.

The row master is established by connecting its $\overline{IES}$ input to ground while a slave receives its $\overline{IES}$ input from the $\overline{IRF}$ output of the next higher priority device. When an array of 'F403 FIFOs is initialized with a LOW on the $\overline{MR}$ inputs of all devices, the $\overline{IRF}$ outputs of all devices will be HIGH. Thus, only the row master receives a LOW on the $\overline{IES}$ input during initialization. Figure 10 is a conceptual logic diagram of the internal circuitry which determines master/slave operation. Whenever $\overline{MR}$ and $\overline{IES}$ are LOW, the Master Latch is set. Whenever $\overline{TTS}$ goes LOW the Request Initialization Flip-Flop will be set. If the Master Latch is HIGH, the Input Register will be immediately initialized and the Request Initialization Flip-Flop reset. If the Master Latch is reset, the Input Register is not initialized until $\overline{IES}$ goes LOW. In array operation, activating the $\overline{TTS}$ initiates a ripple input register initialization from the row master to the last slave.

A similar operation takes place for the output register. Either a $\overline{TOS}$ or TOP input initiates a load-from-stack operation and sets the $\overline{ORE}$ Request Flip-Flop. If the Master Latch is set, the last Output Register Flip-Flop is set and $\overline{ORE}$ goes HIGH. If the Master Latch is reset, the $\overline{ORE}$ output will be LOW until an $\overline{OES}$ input is received.

Block Diagram

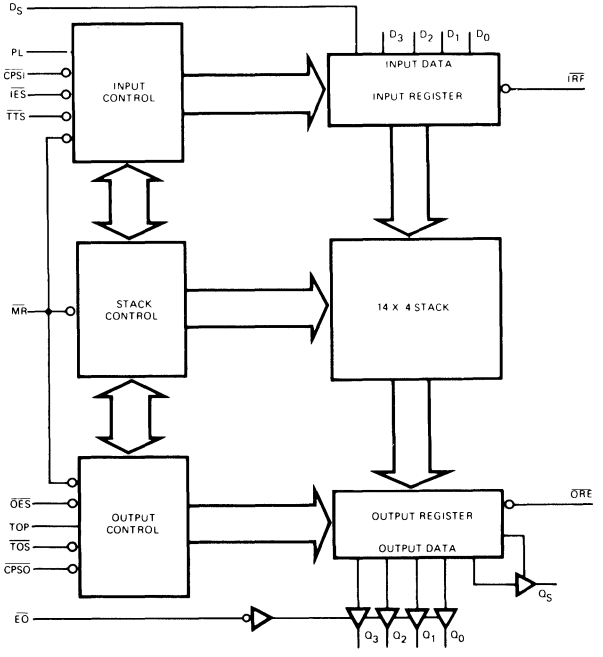


Fig. 1 Conceptual Input Section

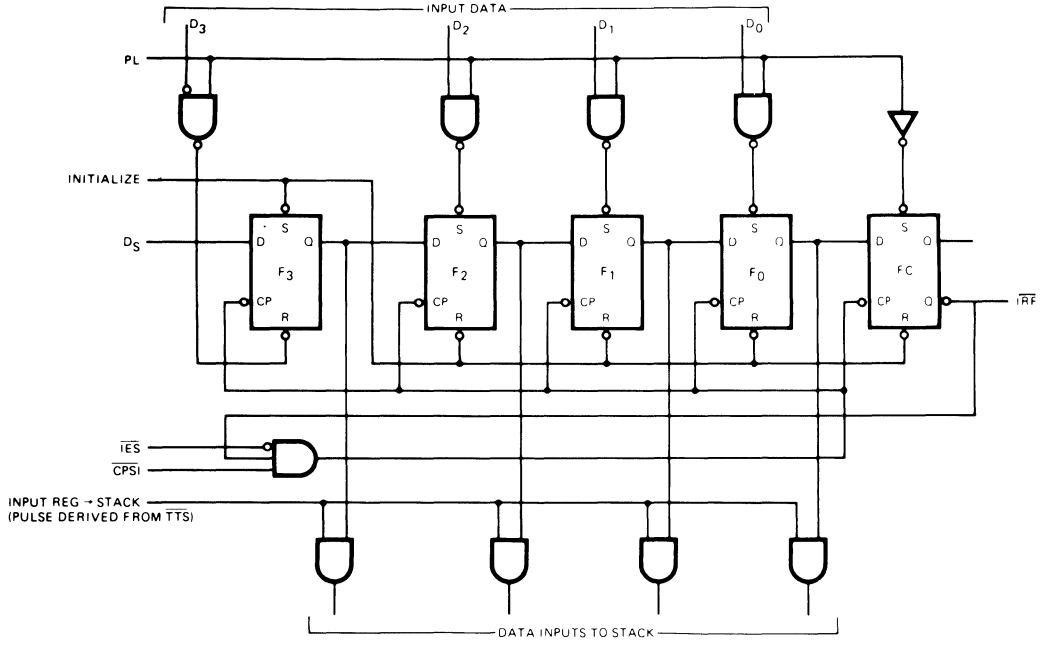


Fig. 2 Final Positions in a 'F403 Resulting from a 64-Bit Serial Train

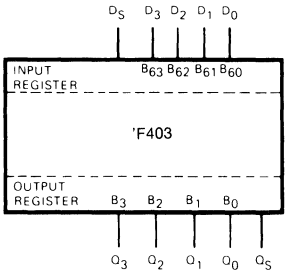


Fig. 3 Conceptual Output Section

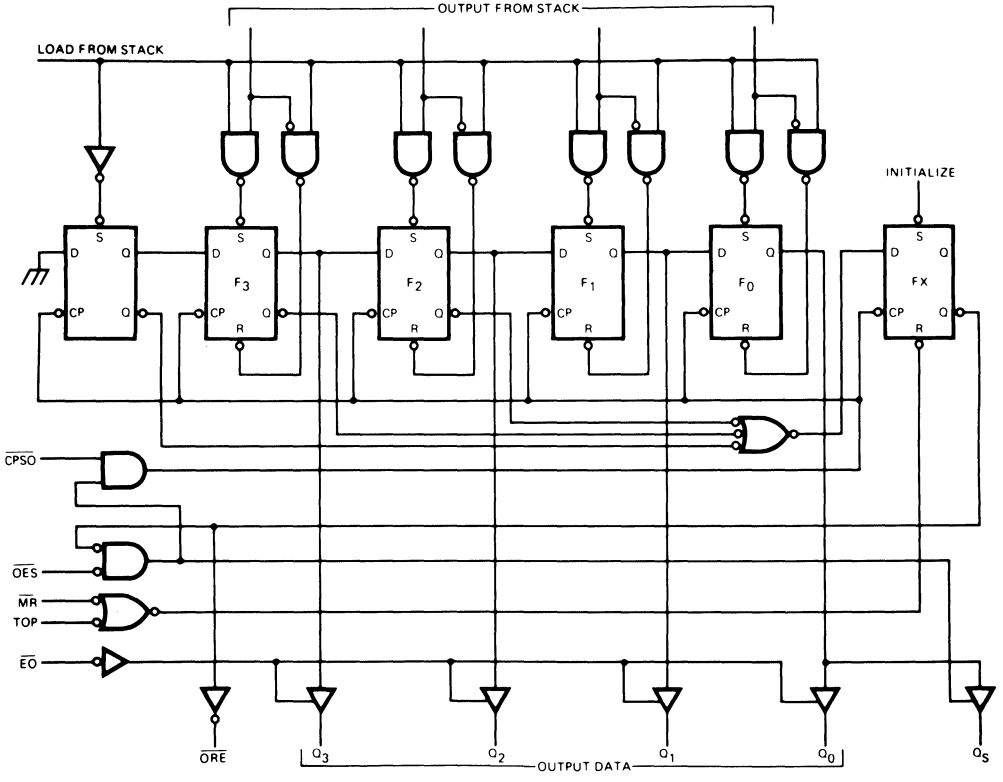


Fig. 4 A Vertical Expansion Scheme

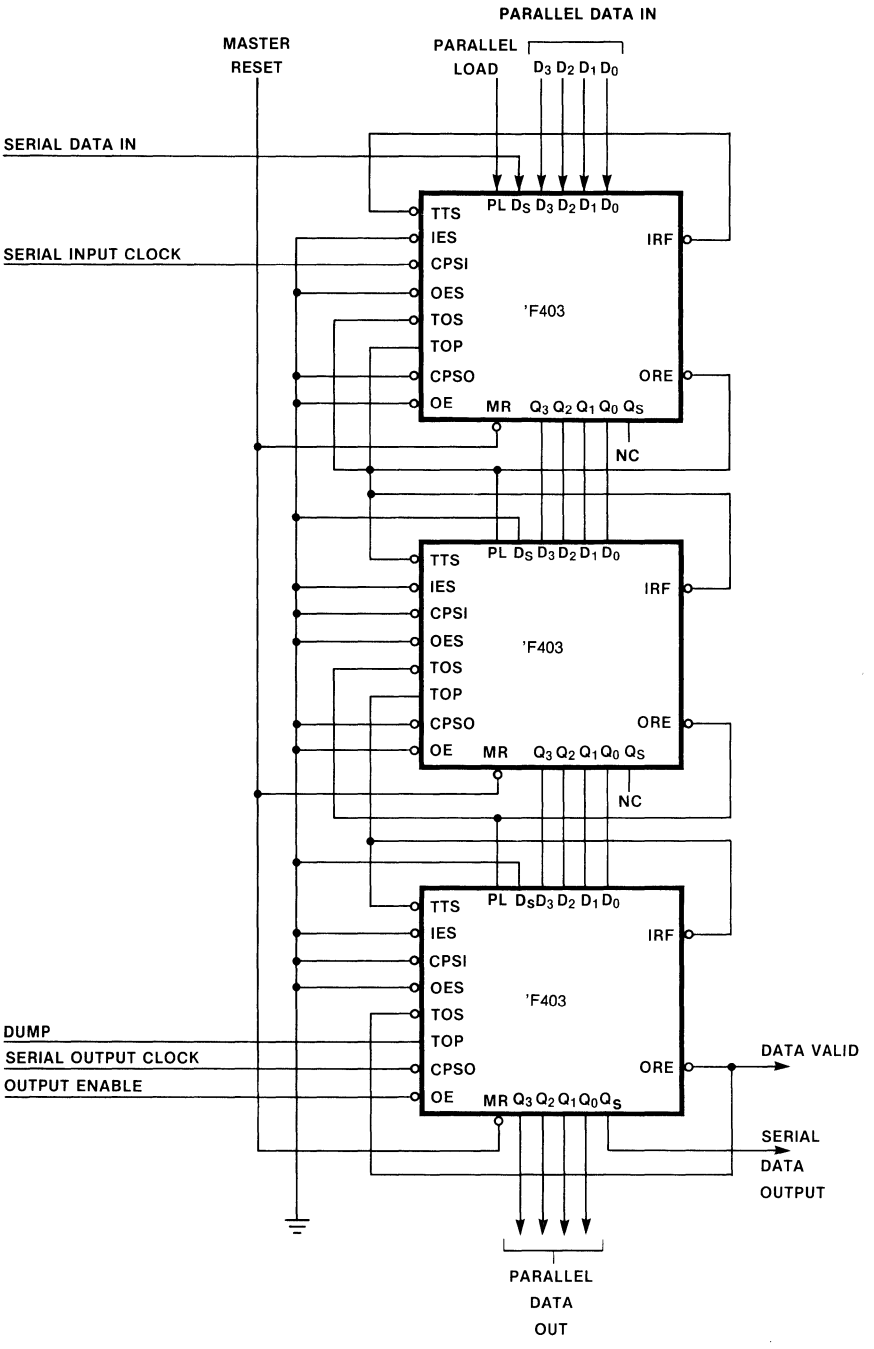


Fig. 5 A Horizontal Expansion Scheme

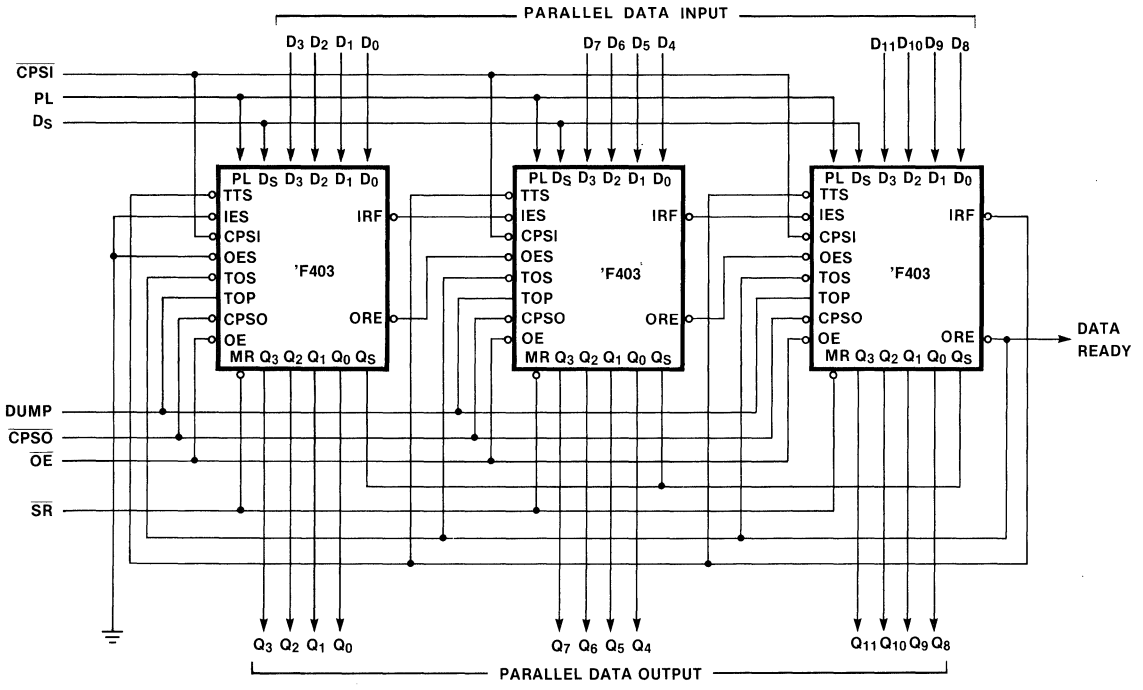


Fig. 6 A 31x16 FIFO Array

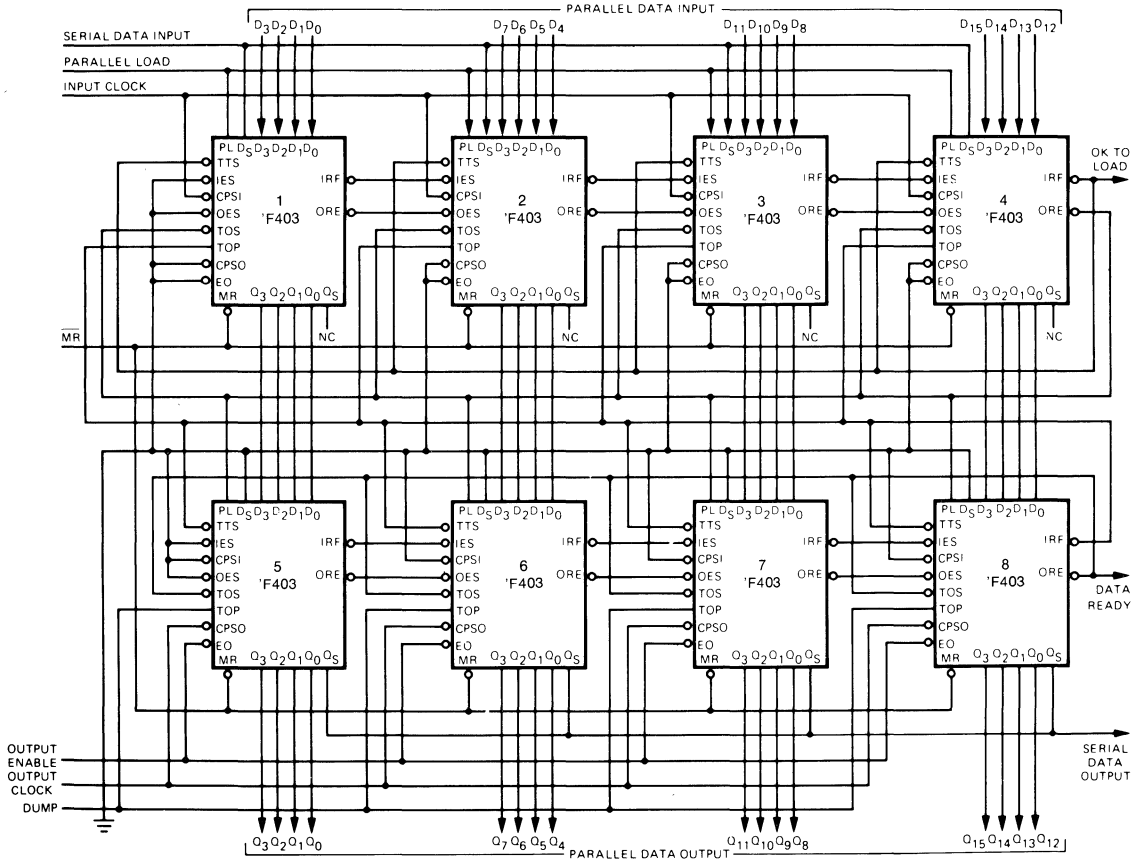


Fig. 7 Serial Data Entry for Array of Fig. 6

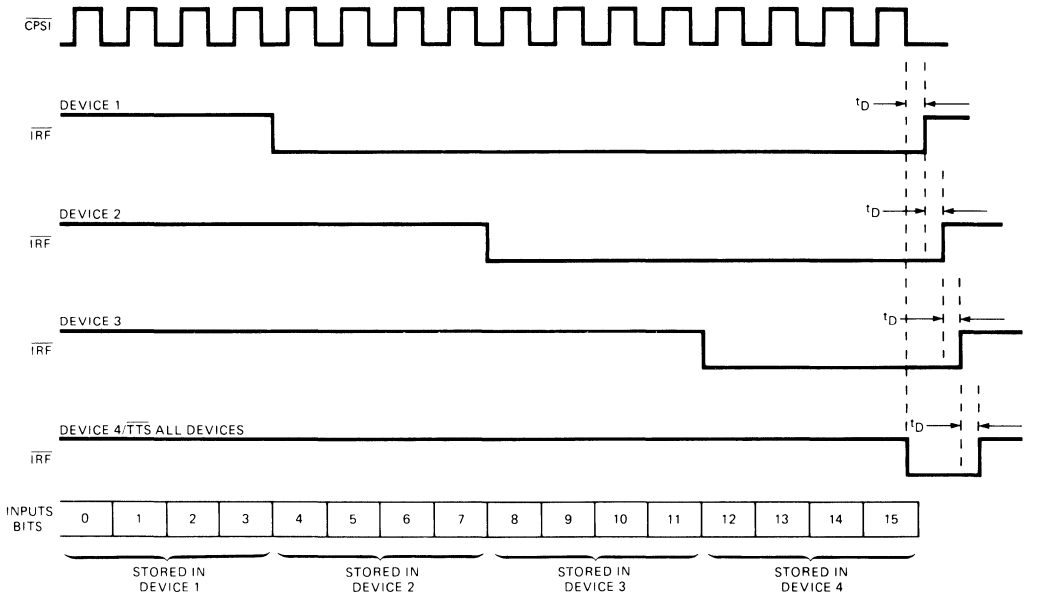


Fig. 8 Serial Data Extraction for Array of Fig. 6

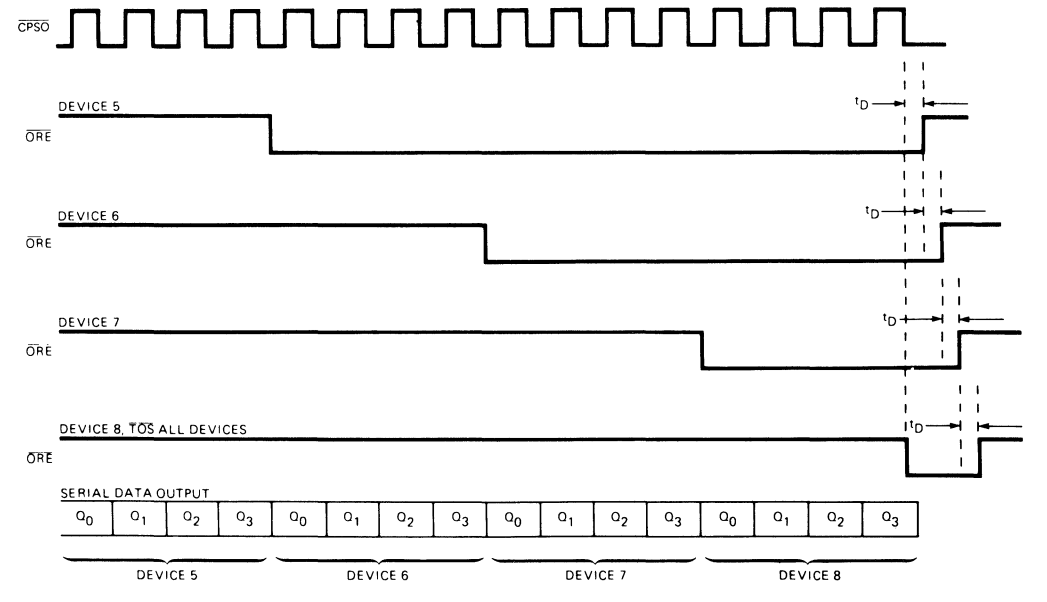


Fig. 9 Final Position of a 496-Bit Serial Input

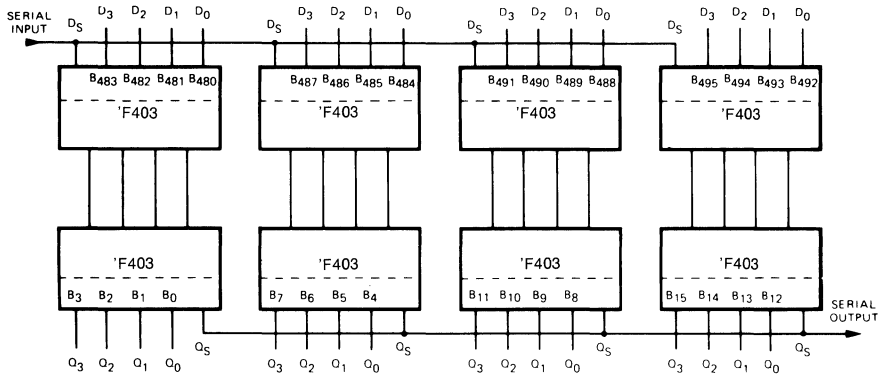
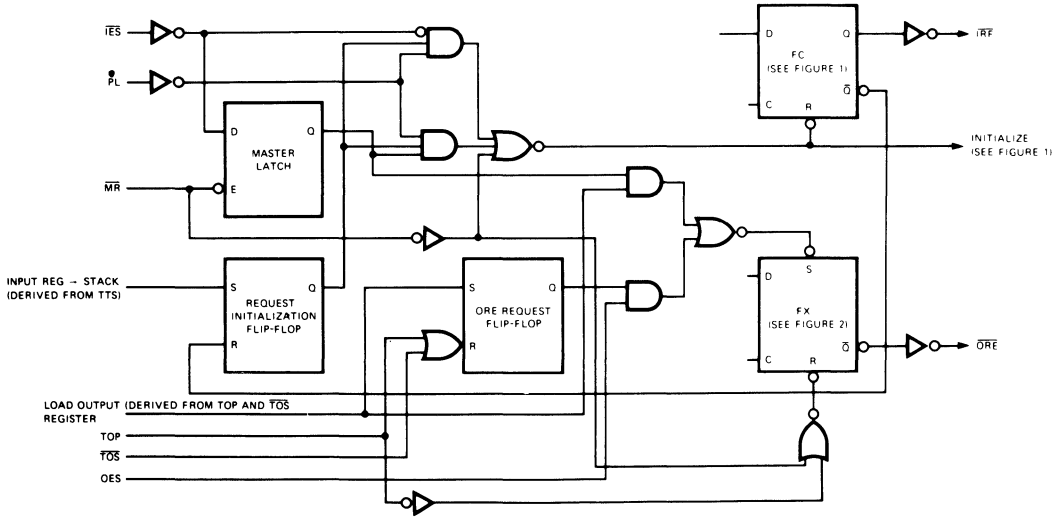


Fig. 10 Conceptual Diagram, Interlocking Circuitry



DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Supply Current		115	170	mA	V_{CC} = Max, Inputs Open

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$			T_A, V_{CC} = Mil $C_L = 50\ pF$		T_A, V_{CC} = Com $C_L = 50\ pF$			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PHL}	Propagation Delay, Negative-Going CP to $\overline{IRF}$ Output			25.0					ns	3-1 403-a 403-b
t_{PLH}	Propagation Delay, Negative-Going $\overline{TTS}$ to $\overline{IRF}$			64.0						
t_{PLH} t_{PHL}	Propagation Delay, Negative-Going $\overline{CPSO}$ to Q_S Output			40.0 23.0					ns	3-1, 403-c 403-d
t_{PLH} t_{PHL}	Propagation Delay, Positive-Going TOP to Outputs Q_0-Q_3			56.0 45.0					ns	3-1 403-e
t_{PHL}	Propagation Delay, Negative-Going $\overline{CPSO}$ to $\overline{ORE}$			42.0					ns	3-1, 403-c 403-d
t_{PHL}	Propagation Delay, Negative-Going TOP to $\overline{ORE}$			54.0					ns	3-1, 403-e
t_{PLH}	Propagation Delay, Positive-Going TOP to $\overline{ORE}$			68.0						
t_{PLH}	Propagation Delay, Negative-Going $\overline{TOS}$ to Postive Going $\overline{ORE}$			53.0					ns	3-1, 403-c 403-d
t_{PHL}	Propagation Delay, Positive-Going PL to Negative-Going $\overline{IRF}$			44.0					ns	3-1 403-g 403-h
t_{PLH}	Propagation Delay, Negative-Going PL to Positive-Going $\overline{IRF}$			28.0						

AC Characteristics (cont'd)

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$	T_A, V_{CC} = Mil $C_L = 50\ pF$	T_A, V_{CC} = Com $C_L = 50\ pF$		
		Min Typ Max	Min Max	Min Max		
t_{PLH}	Propagation Delay, Positive-Going $\overline{OES}$ to $\overline{ORE}$	38.0			ns	3-1
t_{PLH}	Propagation Delay, Positive-Going $\overline{IES}$ to Positive-Going $\overline{IRF}$	40.0			ns	3-1 403-h
t_{PZH} t_{PZL}	Propagation Delay, $\overline{OE}$ to Q_0, Q_1, Q_2, Q_3	14.0 14.0			ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Propagation Delay, $\overline{OE}$ to Q_0, Q_1, Q_2, Q_3	14.0 14.0				
t_{PZH} t_{PZL}	Propagation Delay, Negative-Going $\overline{OES}$ to Q_S	18.0 18.0			ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Propagation Delay, Negative-Going $\overline{OES}$ to Q_S	14.0 14.0				
t_{DFT}	Fall Through Time	600			ns	3-1, 403-f
t_{AP}	Parallel Appearance Time, $\overline{ORE}$ to Q_0-Q_3	-5.0			ns	3-1
t_{AS}	Serial Appearance Time, $\overline{ORE}$ to Q_S	10.0				

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$ $t_s(L)$	Set-up Time, HIGH or LOW D_S to Negative $\overline{CPSI}$	28.0 28.0			ns	403-a 403-b
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D_S to $\overline{CPSI}$	0 0				
$t_s(H)$ $t_s(L)$	Set-up Time, HIGH or LOW $\overline{TTS}$ to $\overline{IRF}$ Serial or Parallel Mode	0 0			ns	403-a 403-b 403-g 403-h
$t_s(L)$	Set-up Time, LOW Negative-Going $\overline{ORE}$ to Negative-Going $\overline{TOS}$	0			ns	403-c 403-d
$t_s(L)$	Set-up Time, LOW Negative-Going $\overline{IES}$ to $\overline{CPSI}$	32.0			ns	403-b
$t_s(L)$	Set-up Time, LOW Negative-Going $\overline{TTS}$ to $\overline{CPSI}$	76.0			ns	403-b
$t_s(H)$ $t_s(L)$	Set-up Time, HIGH or LOW Parallel Inputs to PL	0 0			ns	3-14, 3-15
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW Parallel Inputs to PL	0 0				
$t_w(H)$ $t_w(L)$	$\overline{CPSI}$ Pulse Width HIGH or LOW	25.0 20.0			ns	403-a 403-b
$t_w(H)$	PL Pulse Width, HIGH	40.0			ns	403-g 403-h
$t_w(L)$	$\overline{TTS}$ Pulse Width, LOW Serial or Parallel Mode	20.0			ns	403-a 403-b 403-c 403-d
$t_w(L)$	$\overline{MR}$ Pulse Width, LOW	25.0			ns	403-f
$t_w(H)$ $t_w(L)$	TOP Pulse Width HIGH or LOW	20.0 30.0			ns	403-e
$t_w(H)$ $t_w(L)$	$\overline{CPSO}$ Pulse Width HIGH or LOW	32.0 30.0			ns	403-c 403-d
t_{rec}	Recovery Time $\overline{MR}$ to any Input	10.0			ns	403-f

Fig. 403-a Serial Input, Unexpanded or Master Operation

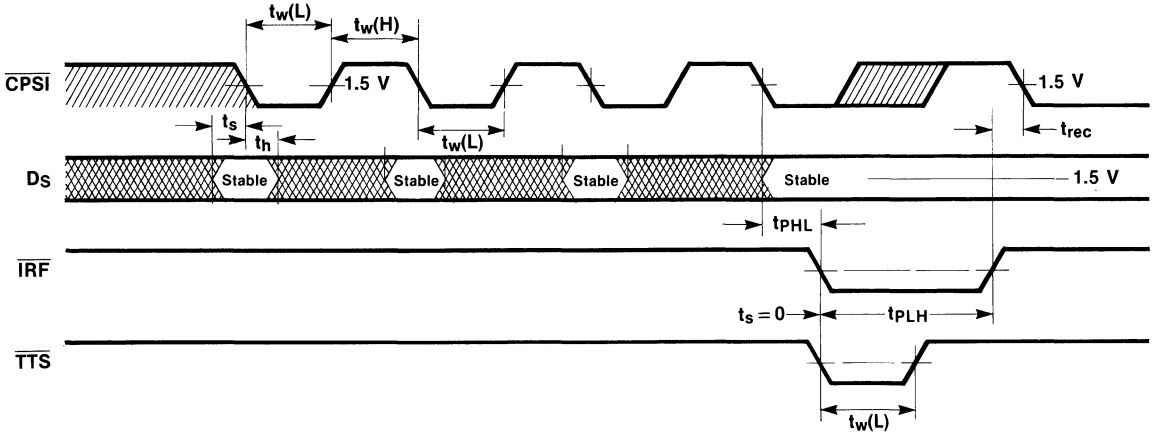


Fig. 403-b Serial Input, Expanded Slave Operation

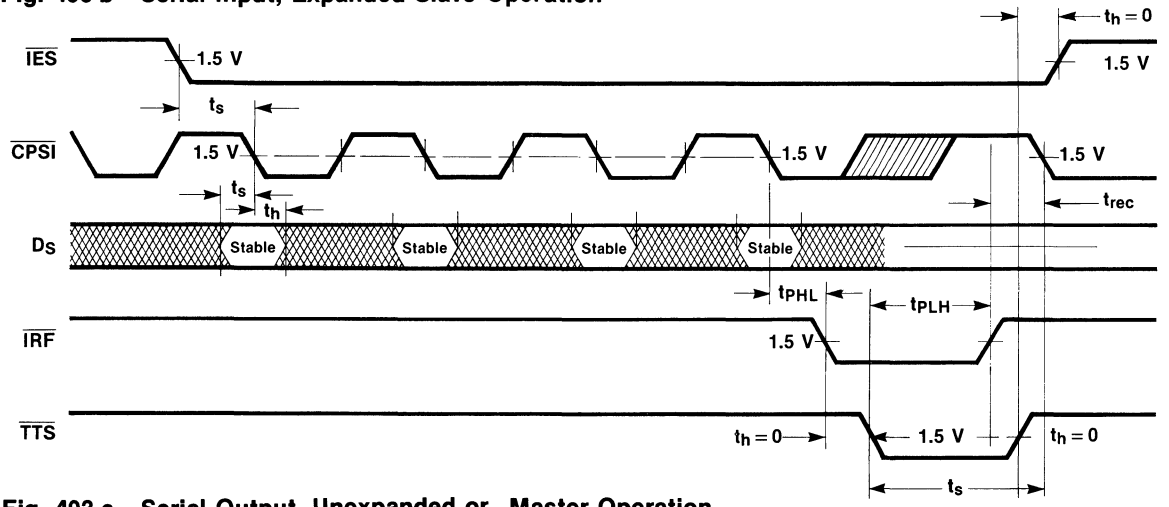
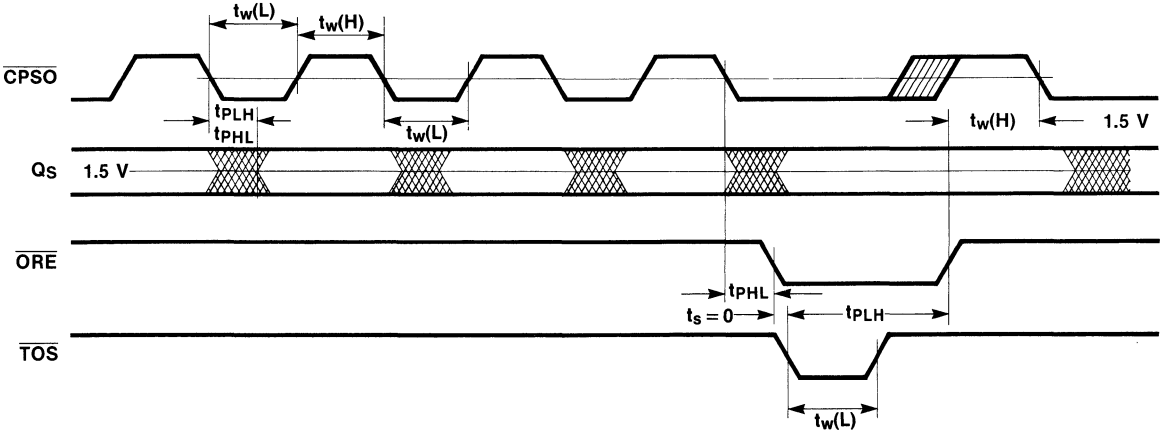


Fig. 403-c Serial Output, Unexpanded or Master Operation



4

Fig. 403-d Serial Output, Slave Operation

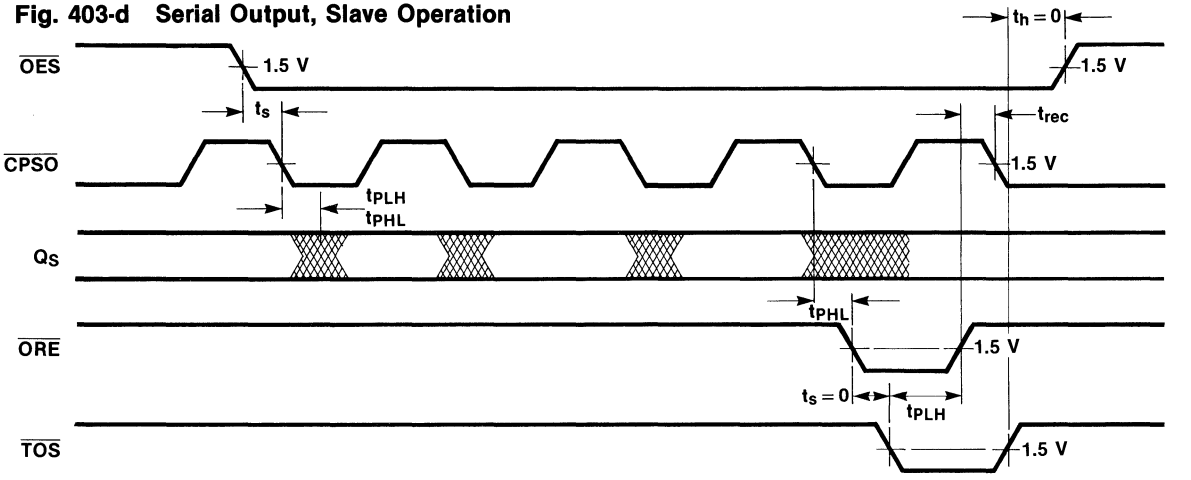


Fig. 403-e Parallel Output, 4-Bit Word or Master in Parallel Expansion

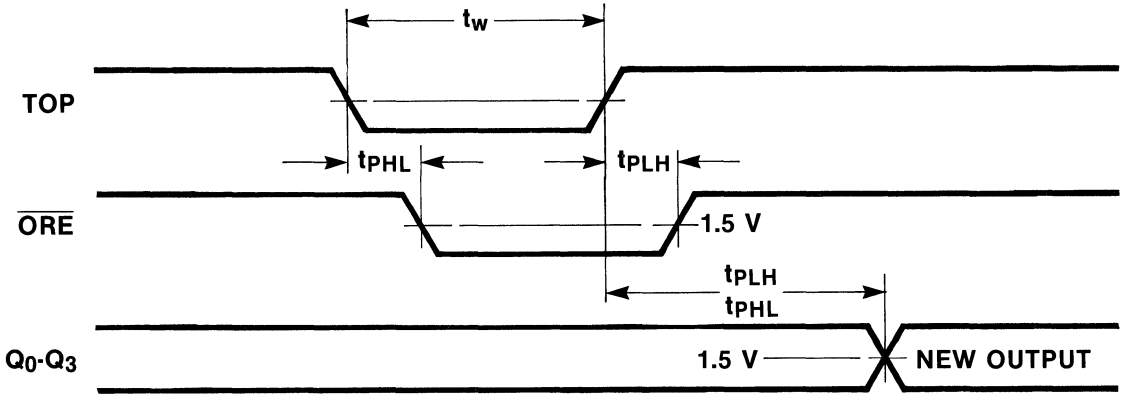


Fig. 403-f Fall Through Time

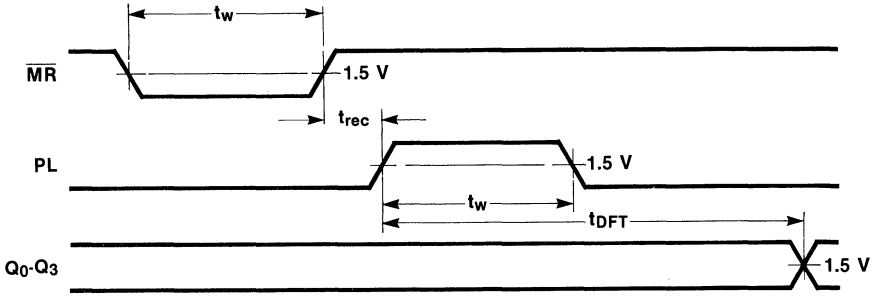


Fig. 403-g Parallel Load Mode, 4-Bit Word (Unexpanded) or master in Parallel Expansion

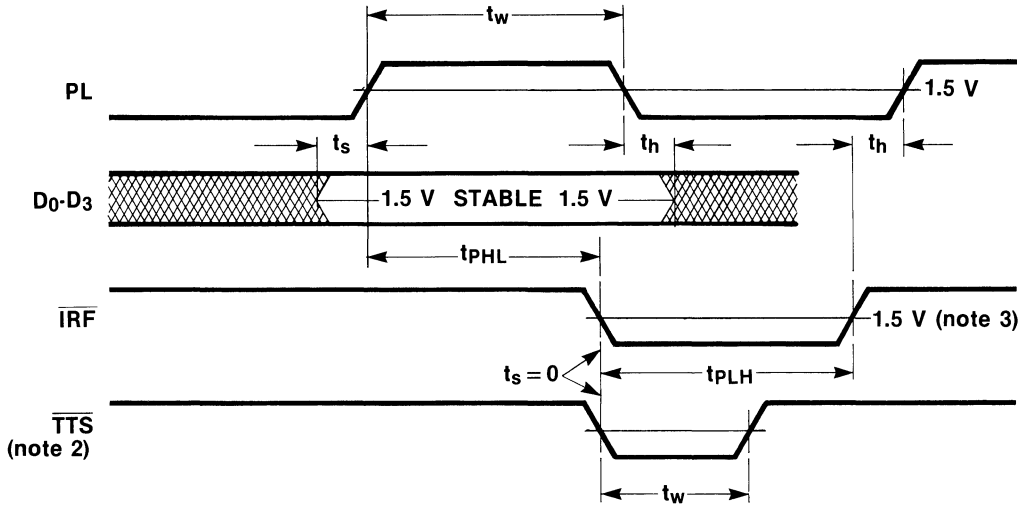
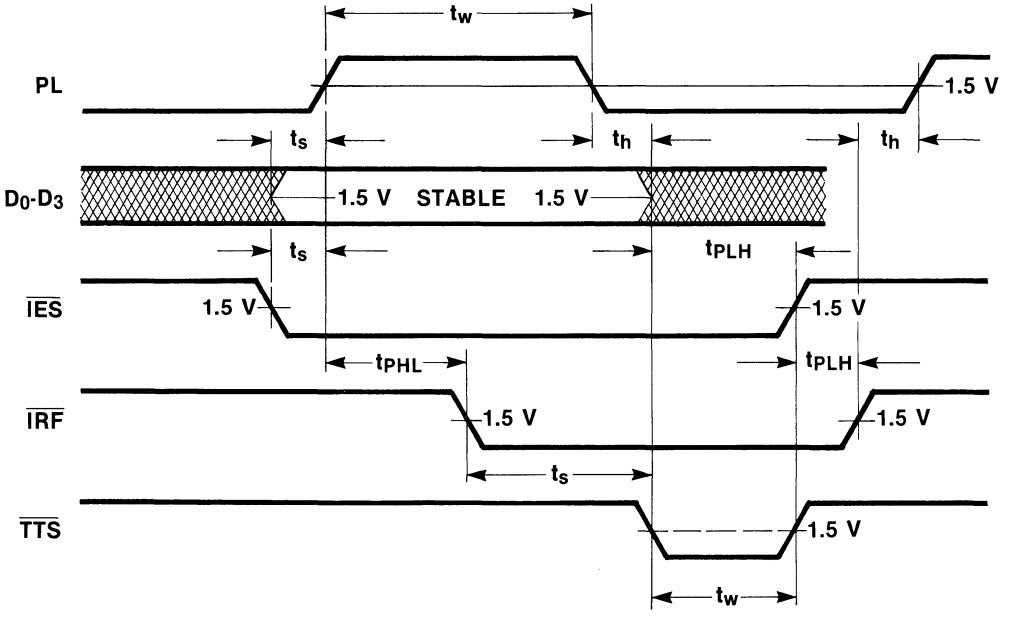


Fig. 403-h Parallel Load, Slave Mode



54F/74F407

Data Access Register

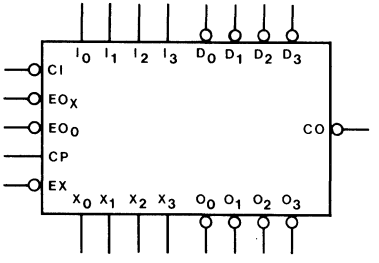
Description

The 'F407 Data Access Register (DAR) performs memory address arithmetic for RAM resident stack applications. It contains three 4-bit registers intended for Program Counter (R_0), Stack Pointer (R_1), and Operand Address (R_2). The 'F407 implements 16 instructions which allow either pre or post decrement/increment and register-to-register transfer in a single clock cycle. It is expandable in 4-bit increments and can operate at a 30 MHz microinstruction rate on a 16-bit word. The 3-state outputs are provided for bus-oriented applications. The 'F407 is fully compatible with all TTL families.

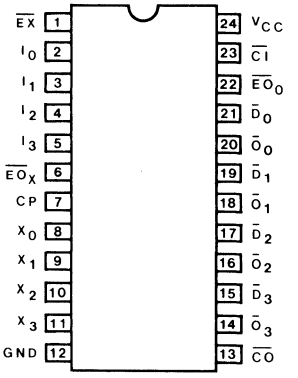
- **High-Speed—Greater than a 30 MHz Microinstruction Rate**
- **Three 4-bit Registers**
- **16 Instructions for Register Manipulation**
- **Two Separate Output Ports, One Transparent**
- **Relative Addressing Capability**
- **3-State Outputs**
- **Optional Pre or Post Arithmetic**
- **Expandable in Multiples of Four Bits**
- **24-Pin Slim Package**

Ordering Code: See Section 5

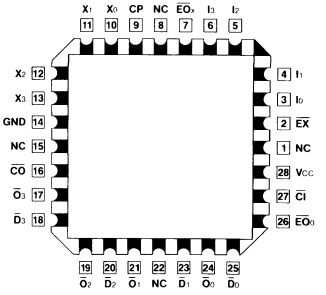
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC

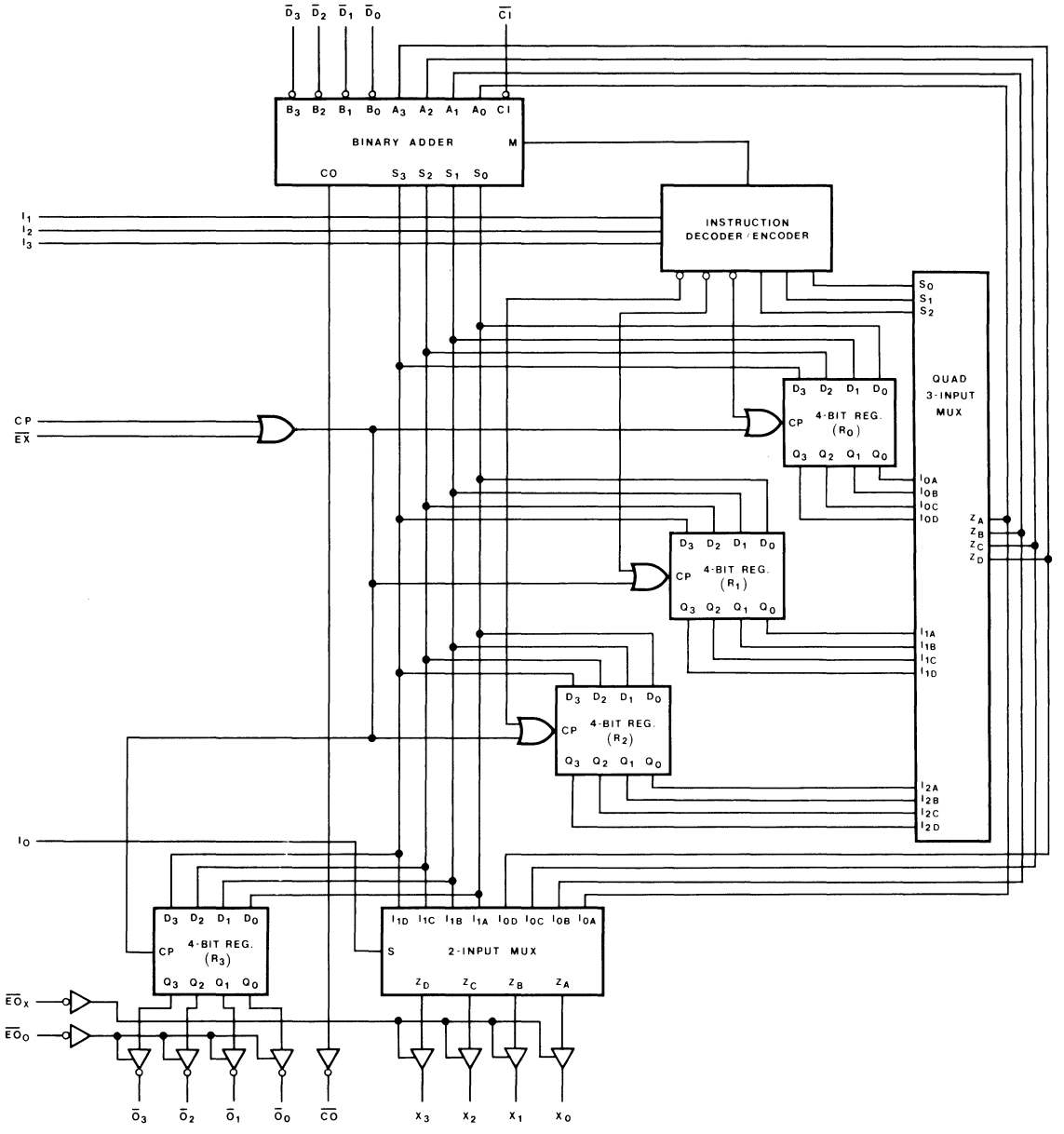


Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
$\overline{D}_0$-$\overline{D}_3$	Data Inputs (Active LOW)	0.5/0.225
I_0-I_3	Instruction Word Inputs	0.5/0.225
$\overline{CI}$	Carry Input (Active LOW)	0.5/0.225
$\overline{CO}$	Carry Output (Active LOW)	10/5 (2.5)
CP	Clock Input (L-H Edge-Triggered)	0.5/0.225
$\overline{EX}$	Execute Input (Active LOW)	0.5/0.225
$\overline{EO}_X$	Address Output Enable Input (Active LOW)	0.5/0.225
$\overline{EO}_0$	Data Output Enable Input (Active LOW)	0.5/0.225
X_0-X_3	Address Outputs	142.5 (50)/10 (5)
$\overline{O}_0$-$\overline{O}_3$	Data Outputs (Active LOW)	142.5 (50)/10 (5)

Block Diagram



Functional Description

The 'F407 contains a 4-bit slice of three Registers (R_0-R_2), a 4-bit Adder, a 3-state Address Output Buffer (X_0-X_3) and a separate Output Register with 3-state buffers ($\overline{O}_0$-$\overline{O}_3$), allowing output of the register contents on the data bus (refer to the Block Diagram). The DAR performs sixteen instructions, selected by I_0-I_3, as listed in the Function Table.

The 'F407 operates on a single clock. CP and $\overline{EX}$ are inputs to a 2-input, active LOW AND gate. For normal operation $\overline{EX}$ is brought LOW while CP is HIGH. A microcycle starts as the clock goes HIGH. Data inputs $\overline{D}_0$-$\overline{D}_3$ are applied to the Adder as one of the operands. Three of the four instruction lines (I_1-I_2-I_3) select which of the three registers, if any, is to be used as the other operand. The LOW-to-HIGH CP transition writes the result from the Adder into a register (R_0-R_2) and into the output register provided $\overline{EX}$ is LOW. If the I_0 instruction input is HIGH, the multiplexer routes the result from the Adder to the 3-state Buffer controlling the address bus (X_0-X_3), independent of $\overline{EX}$ and CP. The 'F407 is organized as a 4-bit register slice. The active LOW $\overline{CI}$ and $\overline{CO}$ lines allow ripple-carry expansion over longer word lengths.

In a typical application, the register utilization in the DAR may be as follows: R_0 is the Program Counter (PC), R_1 is the Stack Pointer (SP) for memory resident stacks and R_2 contains the operand address. For an instruction Fetch, PC can be gated on the X-Bus while it is being incremented (i.e. D-Bus = 1). If the fetched instruction calls for an effective address for execution, which is displaced from the PC, the displacement can be added to the PC and loaded into R_2 during the next microcycle.

Function Table

Instruction				Combinatorial Function Available on the X-Bus	Sequential Function Occurring on the Next Rising CP Edge
I_3	I_2	I_1	I_0		
L	L	L	L	R_0	R_0 plus D plus CI → R_0 and 0-register
L	L	L	H	R_0 plus D plus CI	
L	L	H	L	R_0	R_0 plus D plus CI → R_1 and 0-register
L	L	H	H	R_0 plus D plus CI	
L	H	L	L	R_0	R_0 plus D plus CI → R_2 and 0-register
L	H	L	H	R_0 plus D plus CI	
L	H	H	L	R_1	R_1 plus D plus CI → R_1 and 0-register
L	H	H	H	R_1 plus D plus CI	
H	L	L	L	R_2	D plus CI → R_2 and 0-register
H	L	L	H	D plus CI	
H	L	H	L	R_0	D plus CI → R_0 and 0-register
H	L	H	H	D plus CI	
H	H	L	L	R_2	R_2 plus D plus CI → R_2 and 0-register
H	H	L	H	R_2 plus D plus CI	
H	H	H	L	R_1	D plus CI → R_1 and 0-register
H	H	H	H	D plus CI	

H = HIGH Voltage Level
L = LOW Voltage Level

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Supply Current		90	145	mA	V_{CC} = Max, Inputs Open

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F $T_A = +25°C$, $V_{CC} = +5.0$ V, $C_L = 50$ pF			54F T_A, V_{CC} = Mil, $C_L = 50$ pF		74F T_A, V_{CC} = Com, $C_L = 50$ pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{O}_n^*$ (Note)	8.0 5.0	12.0 7.5	16.0 9.5			7.0 4.0	18.0 10.5	ns	3-1 407-c
t_{PLH} t_{PHL}	Propagation Delay, I_0 LOW I_1-I_3 to X_0-X_3	9.0 9.5	13.0 14.0	17.0 18.0			8.0 8.5	19.0 20.0	ns	3-1 407-a
t_{PLH} t_{PHL}	Propagation Delay, I_0 HIGH I_1-I_3 to X_0-X_3	16.5 11.0	23.5 17.0	30.5 22.5			14.5 10.0	32.5 24.5	ns	3-1 407-a
t_{PLH} t_{PHL}	Propagation Delay, I_0 LOW CP to X_n	9.0 11.5	13.5 18.0	17.5 24.0			8.0 10.5	19.5 26.0	ns	3-1 407-b
t_{PLH} t_{PHL}	Propagation Delay, I_0 HIGH CP to X_n	18.0 12.5	26.5 20.0	35.0 28.5			16.0 11.5	37.0 30.5	ns	3-1 407-b
t_{PLH} t_{PHL}	Propagation Delay $\overline{D}_n$ to X_n	10.5 6.0	15.0 9.0	19.5 12.0			9.5 5.0	21.5 13.5	ns	3-1 407-d
t_{PLH} t_{PHL}	Propagation Delay CI to X_n	7.0 5.5	10.5 9.0	14.0 12.0			6.0 4.5	15.5 13.5	ns	3-1 407-e
t_{PLH} t_{PHL}	Propagation Delay I_0 to X_n	4.5 4.5	9.0 10.0	11.5 13.0			4.0 4.0	13.0 14.5	ns	3-1 407-b
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{CO}$	13.5 13.5	19.0 18.5	24.0 23.5			12.5 12.5	26.0 25.5	ns	3-1 407-a
t_{PLH} t_{PHL}	Propagation Delay $\overline{CI}$ to $\overline{CO}$	3.5 4.5	5.5 7.0	7.5 9.0			3.0 4.0	8.5 10.0	ns	3-1 407-e
t_{PLH} t_{PHL}	Propagation Delay $\overline{D}_n$ to $\overline{CO}$	3.5 4.0	5.5 6.5	7.0 9.0			3.0 3.5	8.0 10.0	ns	3-1 407-d
t_{PLH} t_{PHL}	Propagation Delay I_1-I_3 to $\overline{CO}$	10.0 11.0	15.0 16.0	20.0 21.0			9.0 10.0	22.0 23.0	ns	3-1 407-a

AC Characteristics (cont'd)

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$			T_A, V_{CC} = Mil $C_L = 50\ pF$		T_A, V_{CC} = Com $C_L = 50\ pF$			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PZH} t_{PZL}	Enable Time $\overline{EO}_0$ to $\overline{O}_n$ or $\overline{EO}_x$ to X_n	7.0 6.5	10.0 9.0	12.5 12.0			6.0 5.5	14.0 13.5	ns	3-1, 3-11 3-12
t_{PHZ} t_{PLZ}	Disable Time $\overline{EO}_0$ to$\overline{O}_n$ or $\overline{EO}_x$ to X_n	2.5 7.0	4.0 10.0	5.5 13.0			2.0 6.0	6.5 14.5	ns	3-1, 3-11 3-12

Note: The internal clock is generated from CP and $\overline{EX}$. The internal Clock is HIGH if $\overline{EX}$ or CP is HIGH, LOW if $\overline{EX}$ and CP are LOW.

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
t_{cw}	Clock Period	32.0	26.0				36.0		ns	3-1
$t_s(H)$ $t_s(L)$	Set-Up Time, HIGH or LOW I_1-I_3 to negative going CP	4.0 4.0					4.5 4.5		ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, High or LOW I_1-I_3 to positive-going CP	0 0					0 0			
$t_s(H)$ $t_s(L)$	Set-Up Time, HIGH or LOW $\overline{D}_n$ or $\overline{C}_1$ to negative-going CP	16.5 16.5					18.5 18.5		ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{D}_n$ or $\overline{CI}$ to negative-going clock	0 0					0 0			
$t_s(H)$ $t_s(L)$	Set-Up Time, HIGH or LOW $\overline{CI}$ to positive-going CP	13.0 13.0					14.5 14.5		ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{CI}$ to positive-going CP	0 0					0 0			
$t_w(H)$ $t_w(L)$	Clock Pulse Width HIGH or LOW	7.5 7.5					8.5 8.5		ns	3-7

Timing Diagrams

Fig. 407-a

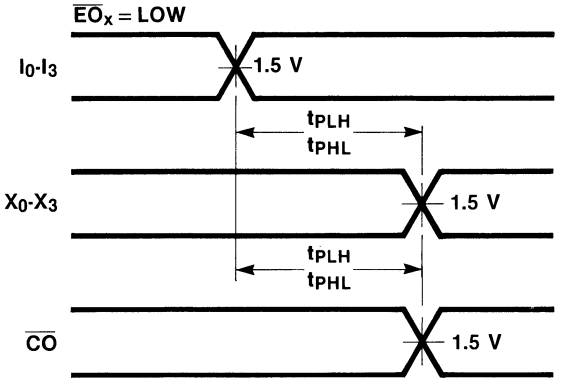


Fig. 407-b

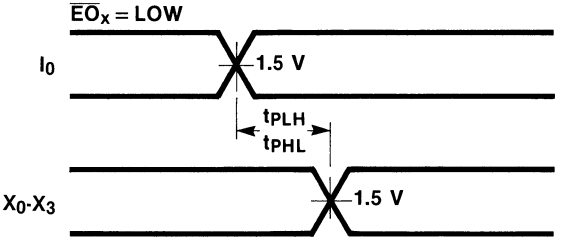


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Fig. 407-c

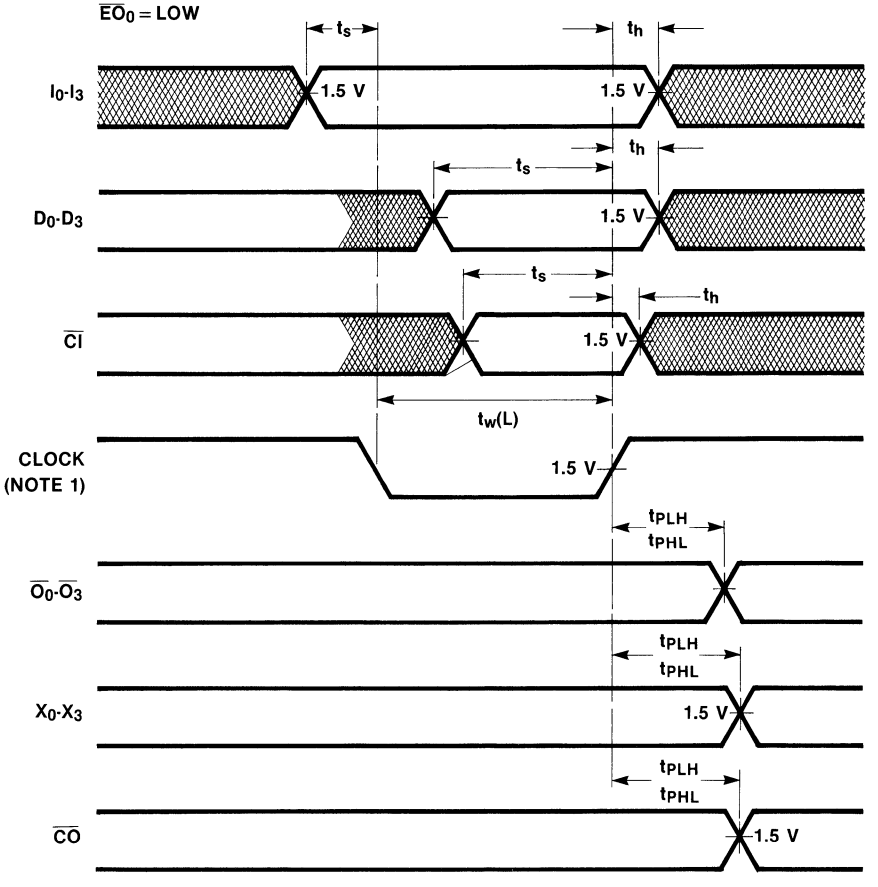


Fig. 407-d

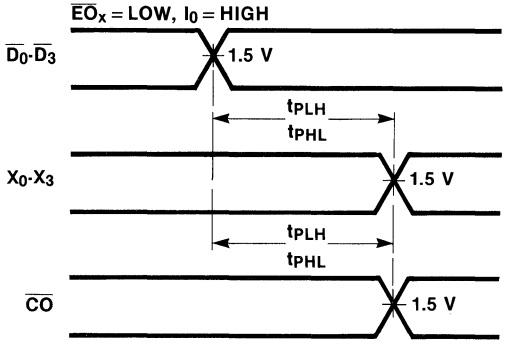
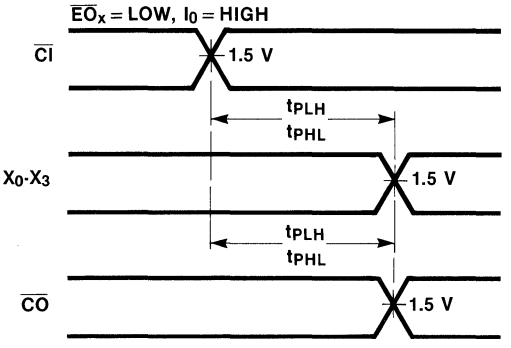


Fig. 407-e



54F/74F410

Register Stack—16x4 RAM
3-State Output Register

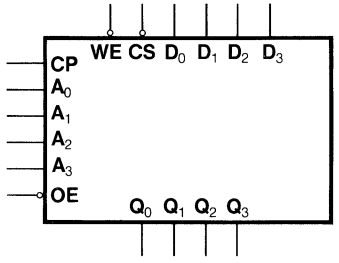
Description

The 'F410 is a register-oriented high-speed 64-bit Read/Write Memory organized as 16-words by 4-bits. An edge-triggered 4-bit output register allows new input data to be written while previous data is held. 3-state outputs are provided for maximum versatility. The 'F410 is fully compatible with all TTL families.

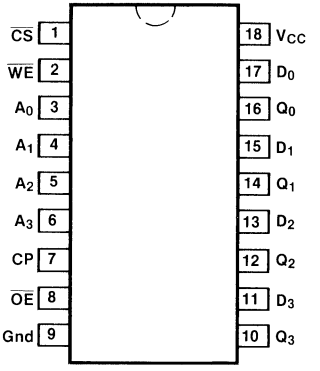
- **Edge-Triggered Output Register**
- **Typical Access Time of 35 ns**
- **3-State Outputs**
- **Optimized for Register Stack Operation**
- **18-Pin Package**

Ordering Code: See Section 5

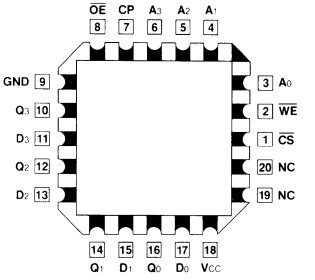
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
A_0-A_3	Address Inputs	0.5/0.375
D_0-D_3	Data Inputs	0.5/0.375
$\overline{CS}$	Chip Select Input (Active LOW)	0.5/0.75
$\overline{OE}$	Output Enable Input (Active LOW)	0.5/0.375
$\overline{WE}$	Write Enable Input (Active LOW)	0.5/0.375
CP	Clock Input (Outputs Change on LOW-to-HIGH Transition)	0.5/0.75
Q_0-Q_3	Outputs	75/15 (12.5)

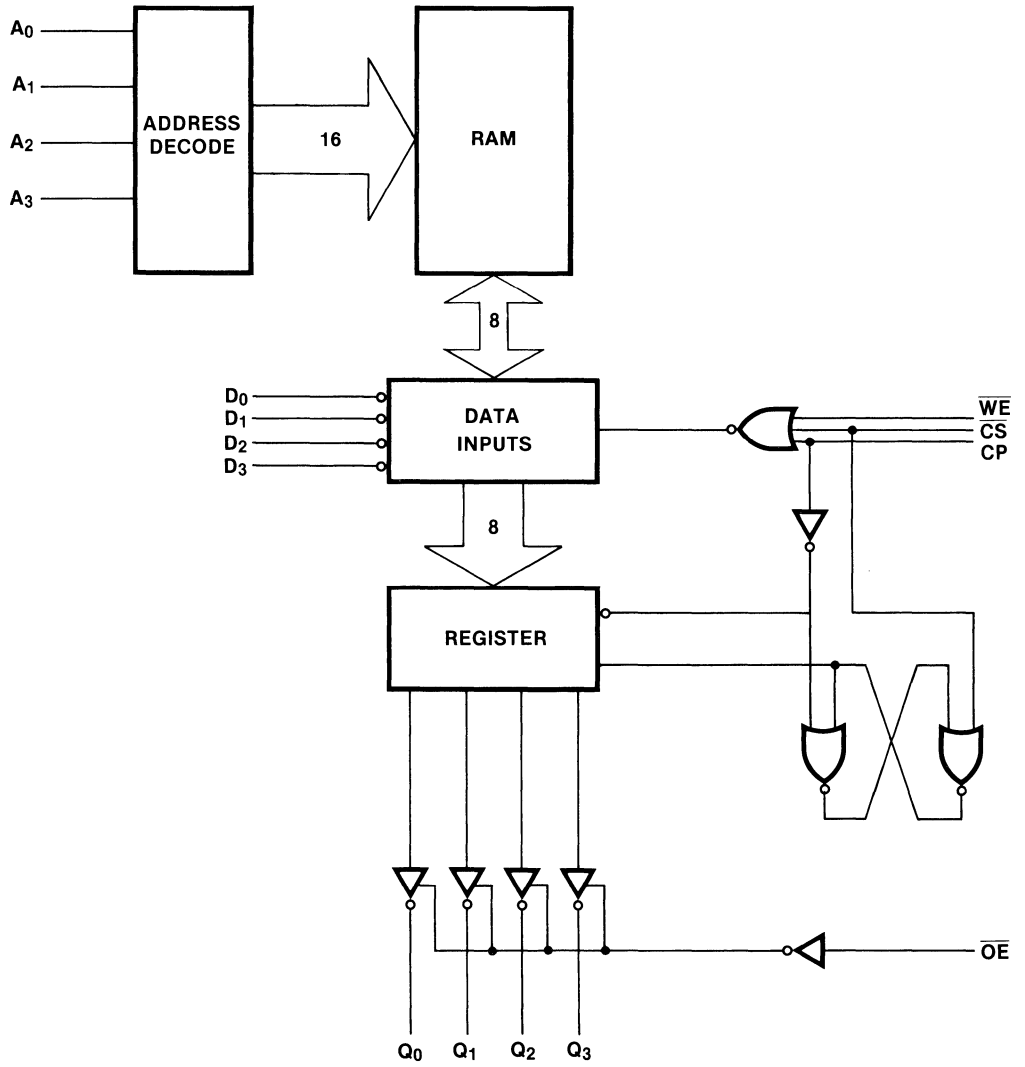
Functional Description

Write Operation—When the three control inputs, Write Enable ($\overline{WE}$), Chip Select ($\overline{CS}$), and Clock (CP), are LOW the information on the data inputs (D_0-D_3) is written into the memory location selected by the address inputs (A_0-A_3). If the input data changes while $\overline{WE}$, $\overline{CS}$, and CP are LOW, the contents of the selected memory location follow these changes, provided set-up and hold time criteria are met.

Read Operation—Whenever $\overline{CS}$ is LOW and CP goes from LOW-to-HIGH, the contents of the memory location selected by the address inputs (A_0-A_3) are edge-triggered into the Output Register.

The ($\overline{OE}$) input controls the output buffers. When $\overline{OE}$ is HIGH the four outputs (Q_0-Q_3) are in a high impedance or OFF state; when $\overline{OE}$ is LOW, the outputs are determined by the state of the Output Register.

Block Diagram



DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Supply Current		47	70	mA	V_{CC} = Max, Inputs Open

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	3.0	6.5	8.5			2.5	9.5	ns	3-1
t_{PHL}	CP to Q	3.5	7.0	9.0			3.0	10.0		3-7
t_{PZH}	Enable Time	3.0	6.0	8.0			2.5	9.0	ns	3-1, 3-12, 3-13
t_{PZL}	$\overline{OE}$ to Q	3.5	7.0	9.0			3.0	10.0		
t_{PHZ}	Disable Time	2.5	4.5	6.5			2.0	7.5		
t_{PLZ}	$\overline{OE}$ to Q	2.5	5.0	7.5			2.0	8.0		

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F $T_A = +25°C$ $V_{CC} = +5.0\ V$			54F T_A, V_{CC} = Mil		74F T_A, V_{CC} = Com		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
READ MODE										
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW A_n to CP	15.0 15.0					17.0 17.0		ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW A_n to CP	0 0					0 0			
WRITE MODE										
$t_s(H)$ $t_s(L)$	Setup Time HIGH or LOW A_n to $\overline{WE}$	0 0					0 0		ns	3-16
$t_h(H)$ $t_h(L)$	Hold Time HIGH or LOW A_n to $\overline{WE}$	0 0					0 0			
$t_s(H)$ $t_s(L)$	Setup Time HIGH or LOW D_n to $\overline{WE}$	5.0 5.0					6.0 6.0		ns	3-15
$t_h(H)$ $t_h(L)$	Hold Time HIGH or LOW D_n to $\overline{WE}$	0 0					0 0			
t_w	$\overline{WE}$ Pulse Width Required to Write	7.5					8.5		ns	3-8
t_w	$\overline{CS}$ Pulse Width Required to Write	7.5					8.5		ns	3-8
t_w	CP Pulse Width Required to Write	7.5					8.5		ns	3-7

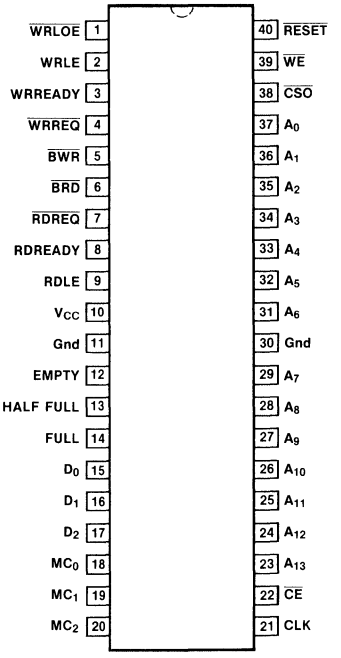
54F/74F411

FIFO RAM Controller

Description

The 'F411 FIFO RAM Controller (FRC) is an address and status generator designed to implement a high-speed First-In/First-Out (FIFO) stack utilizing standard off-the-shelf RAMs. The 'F411 can control up to 16K words of buffer memory; intermediate buffer sizes can be selected (see device functional description). Built-in arbitration logic controls read/write operations on first-come/first-served basis.

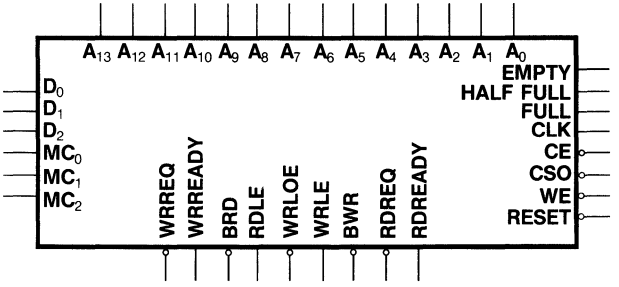
Connection Diagrams

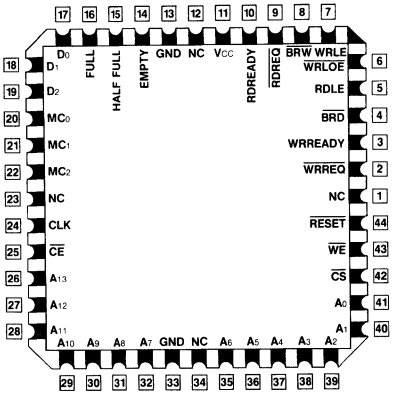


Pin Assignment for DIP

Ordering Code: See Section 5

Logic Symbol





Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
A_0-A_{13}	Read/Write Address	75/15 (12.5)
MC_0-MC_2	Memory Clock Select	0.5/0.375
D_0-D_2	FIFO Depth Select	0.5/0.375
EMPTY	Status Line	25/12.5
HALF FULL	Status Line	25/12.5
FULL	Status Line	25/12.5
$\overline{BRD}$, $\overline{BWR}$	Burst Read, Burst Write	0.5/0.375
WRLE, RDLE	Write Latch Enable, Read Latch Enable	25/12.5
$\overline{RDREQ}$	Read Request	0.5/0.375
$\overline{WRREQ}$	Write Request	0.5/0.375
$\overline{WE}$	RAM Write Enable	25/12.5
$\overline{CSO}$	RAM Chip Select Output	25.12.5
$\overline{RESET}$	Master Reset	0.5/0.375
CLK	Clock	0.5/0.375
$\overline{CE}$	Chip Enable	0.5/0.375
WRREADY	Write Ready	25/12.5
RDREADY	Read Ready	25/12.5
$\overline{WRLOE}$	Write Latch Output Enable	25/12.5

Functional Description

The 'F411 FIFO RAM Controller consists of three 14-bit counters. Two of these counters provide read/write addresses for FIFO read/write operations respectively. The third counter is an up-down counter. Depending on the operation of FIFO, the counter is either incremented (write operation) or decremented (read operation). The output of the counter is decoded according to the memory length select lines D_0-D_2 to produce EMPTY, HALF FULL, or FULL status lines. (See Table 2).

The arbitration logic handles all read/write requests on first-come/first-served basis. In the event of a tie, the priority is based on the HALF FULL status signal. Normally write requests have higher priority over read requests unless the HALF FULL signal is active, in which case the read requests have priority over write requests. The arbiter decision can be disabled by Burst Read or Burst Write request in which case all subsequent read or write requests are denied until burst read or write operation is terminated. The priority will be the same as normal read and write should Burst Write and Burst Read become active simultaneously. (See Table 3.)

The WRLE and RDLE signals control the external latches at the top and bottom of the FIFO stack. Read (RD) and Write (WR) pulses are used to transfer data to and from the RAM locations specified by the address bus. Read and Write pulse widths can be programmed using memory clock pins MC_0-MC_2, (See Table 1). RESET will reset all counters to zero. HALF FULL and FULL status lines are forced LOW and EMPTY status forced HIGH.

Functional Operation

A_0-A_{13}

Fourteen 3-state outputs are capable of driving an 8 mA DC load. The FIFO can address up to 16K words of data.

The three Memory Clock select lines determine the number of master clock cycles by which Write or Read pulse width is extended. See Table 1 for selection guide.

D_0-D_2

The length of the FIFO memory can be hardware-selected via the length select (D_0-D_2) inputs. When less than the maximum length is selected, the unused high-order bits of the address outputs are held in the high-impedance state.

Write Request ($\overline{WRREQ}$)

Write request for write cycle; active LOW input.

Read Request ($\overline{RDREQ}$)

Read request for read cycle; active LOW input.

Write Enable ($\overline{WE}$)

Write cycle address valid, active LOW 3-State output.

Chip Select Output ($\overline{CSO}$)

When active, the RAM will be selected. Active LOW, 3-State output.

RESET

Active LOW master reset input. The user must force the RESET input LOW to initialize the chip. The following actions occur when RESET is active:

1. All internal counters are set to '0'.
2. Half Full and Full outputs are forced LOW.
3. $\overline{WE}$, $\overline{CSO}$ and EMPTY outputs are forced HIGH.
4. WRREADY and RDREADY signals are forced HIGH and LOW respectively.
5. Write latch will be disabled and transparent.
6. Read latch will be disabled and transparent.
7. RAM write address selected.

Burst Read ($\overline{BRD}$)

Active LOW input; the following actions occur when $\overline{BRD}$ is active:

1. Write Ready is forced HIGH.
2. Priority is always given to read requests.

Burst Write ($\overline{BWR}$)

Active LOW input; the following actions occur when $\overline{BWR}$ is active:

1. Read Ready is forced HIGH.
2. Priority is always given to write requests.

Write Ready (WRREADY)

Active HIGH output; WRREADY HIGH signals that FIFO is ready to accept write requests. WRREADY goes LOW on the positive-going edge of Master Clock on a pending write request. The WRREADY will go from LOW-to-HIGH one clock cycle later if FULL signal is LOW.

Read Ready (RDREADY)

Active HIGH output; RDREADY HIGH signals that FIFO is ready to accept read requests. RDREADY goes LOW on the positive-going edge of Master Clock on a pending read request. The RDREADY will go from LOW-to-HIGH on the positive going edge of $\overline{CS}$ if EMPTY signal is LOW.

Clock (CLK)

Clock input to the FIFO (variable); typical clock = 50 MHz.

Chip Enable ($\overline{CE}$)

Active LOW input; when inactive all RAM interface signals are held in high impedance state and further read or write requests are denied. Read or Write cycles in progress when $\overline{CE}$ goes HIGH will finish before the chip is deactivated.

Read Latch Enable (RDLE)

Active HIGH output; on the HIGH-to-LOW transition of RDLE, FIFO data is latched into the external output data latch.

Note RDLE will remain HIGH for modes 0-3 of MC.

Write Latch Enable (WRLE)

Active HIGH output; on the HIGH-to-LOW transition of WRLE data to be written into the FIFO is latched into the external input data latch.

Write Latch Output Enable ($\overline{WRLOE}$)

Active LOW output; on the HIGH-to-LOW transition of WRLOE the output of external input data latch is enabled.

FULL

Memory Full status output. The FULL signal goes HIGH on the negative-going edge of Master Clock if WRREADY is LOW and all bits of status counter for selected length are equal to '1'. The FULL signal goes from HIGH-to-LOW on the negative-going edge of Master Clock if RDREADY is LOW.

Note: WRREADY will remain LOW so long as full signal is active.

HALF FULL

Memory Half Full status output. The HALF FULL operates in the same way as FULL signal except that it goes HIGH when status counter reaches a count of 127 ($D_2 = H$, $D_1 = H$, $D_0 = L$). The HALF FULL signal goes from HIGH-to-LOW on the negative-going edge of Master Clock if RDREADY is LOW.

EMPTY

Memory Empty Status Output. The EMPTY signal goes HIGH on the negative-going edge of Master Clock if status counter contains a value of '1' and RDREADY is LOW. The EMPTY signal goes from HIGH-to-LOW on the negative-going edge of Master Clock if WRREADY is LOW.

Note: RDREADY will remain LOW so long as EMPTY signal is valid.

Block Diagram

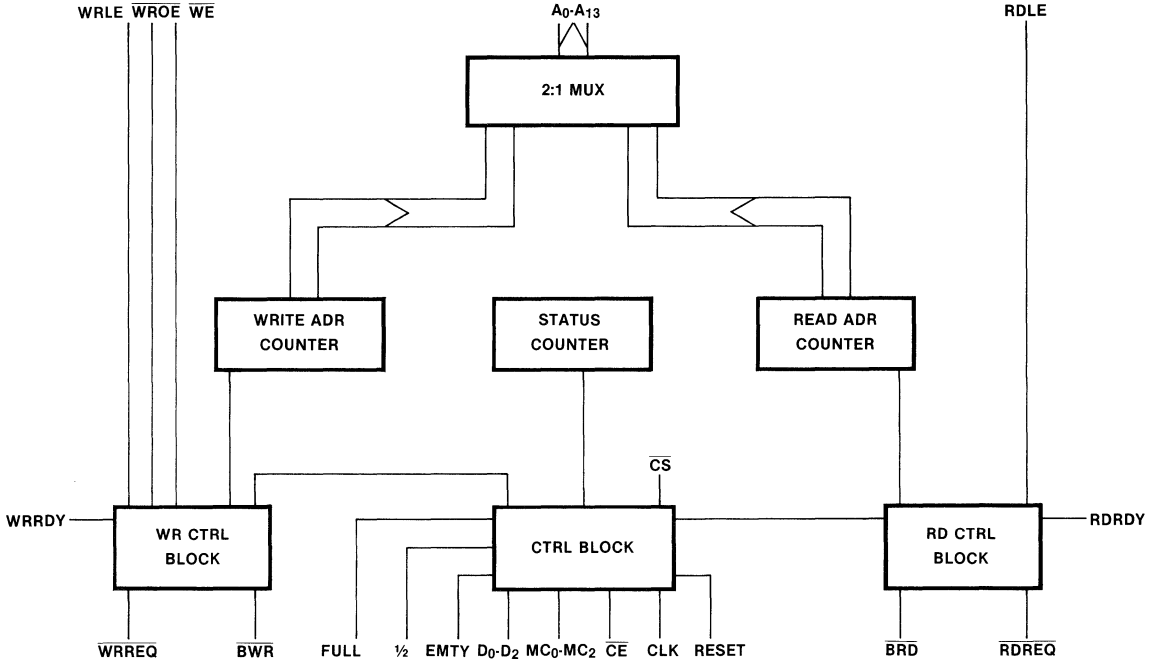


Table 1

MC_2	MC_1	MC_0	Mode	$\overline{WE}$ Duration	$\overline{CS}$ Duration
0	0	0	0	1	LOW*
0	0	1	1	2	LOW*
0	1	0	2	3	LOW*
0	1	1	3	4	LOW*
1	0	0	4	1	1
1	0	1	5	2	2
1	1	0	6	3	3
1	1	1	7	4	4

*Chip Select output remains LOW irrespective of MC_nsettings.

Table 2

D_2	D_1	D_0	Half Length Words	Full Length Words
0	0	0	8K	16K
0	0	1	4K	8K
0	1	0	2K	4K
0	1	1	1K	2K
1	0	0	512	1024
1	0	1	256	512
1	1	0	128	256
1	1	1	64	128

Table 3

$\overline{RDREQ}$	$\overline{WRREQ}$	$\overline{BWR}$	$\overline{BRD}$	Half Full	Priority
L	L	L	L	L	NOOP
L	L	L	L	H	NOOP
L	L	L	H	L	WRITE
L	L	L	H	H	WRITE
L	L	H	L	L	READ
L	L	H	L	H	READ
L	L	H	H	L	WRITE
L	L	H	H	H	READ
L	H	L	L	L	NOOP
L	H	L	L	H	NOOP
L	H	L	H	L	NOOP
L	H	L	H	H	NOOP
L	H	H	L	L	READ
L	H	H	L	H	READ
L	H	H	H	L	READ
L	H	H	H	H	READ
H	L	L	L	L	NOOP
H	L	L	L	H	NOOP
H	L	L	H	L	WRITE
H	L	L	H	H	WRITE
H	L	H	L	L	NOOP
H	L	H	L	H	NOOP
H	L	H	H	L	WRITE
H	L	H	H	H	WRITE
H	H	X	X	X	NOOP

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		125	190	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units
		T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency Data Rate with 20 ns SRAM	50 25							MHz
t_{PHL}	Propagation Delay $\overline{CSO}$ to $\overline{WE}$			5.0					ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{WRREQ}$ to WRREADY			13.0 13.0					ns
t_{PLH} t_{PHL}	Propagation Delay WRREADY to WRLE			10.0 10.0					ns
t_{PLH} t_{PHL}	Propagation Delay WRREADY to $\overline{WRLOE}$			10.0 10.0					ns
t_{PLH} t_{PHL}	Propagation Delay Clock to WRREADY			6.0 6.0					ns
t_{PLH} t_{PHL}	Propagation Delay WRREADY to Status Output			20.0 20.0					ns
t_{PLH} t_{PHL}	Propagation Delay RDREADY to RDLE			25.0 25.0					ns

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com	
		Min Typ Max	Min Max	Min Max	
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW RAM Add	5.0 5.0			ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW RAM Add	5.0 5.0			
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{WRREQ}$	5.0 5.0			ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{WRREQ}$	5.0 5.0			
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{BWR}$	5.0 5.0			ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{BWR}$	5.0 5.0			
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{BRD}$	5.0 5.0			ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{BRD}$	5.0 5.0			ns
$t_w(H)$ $t_w(L)$	$\overline{CSO}$ Pulse Width HIGH or LOW	20.0 20.0			ns

Fig. 411-a Write Cycle

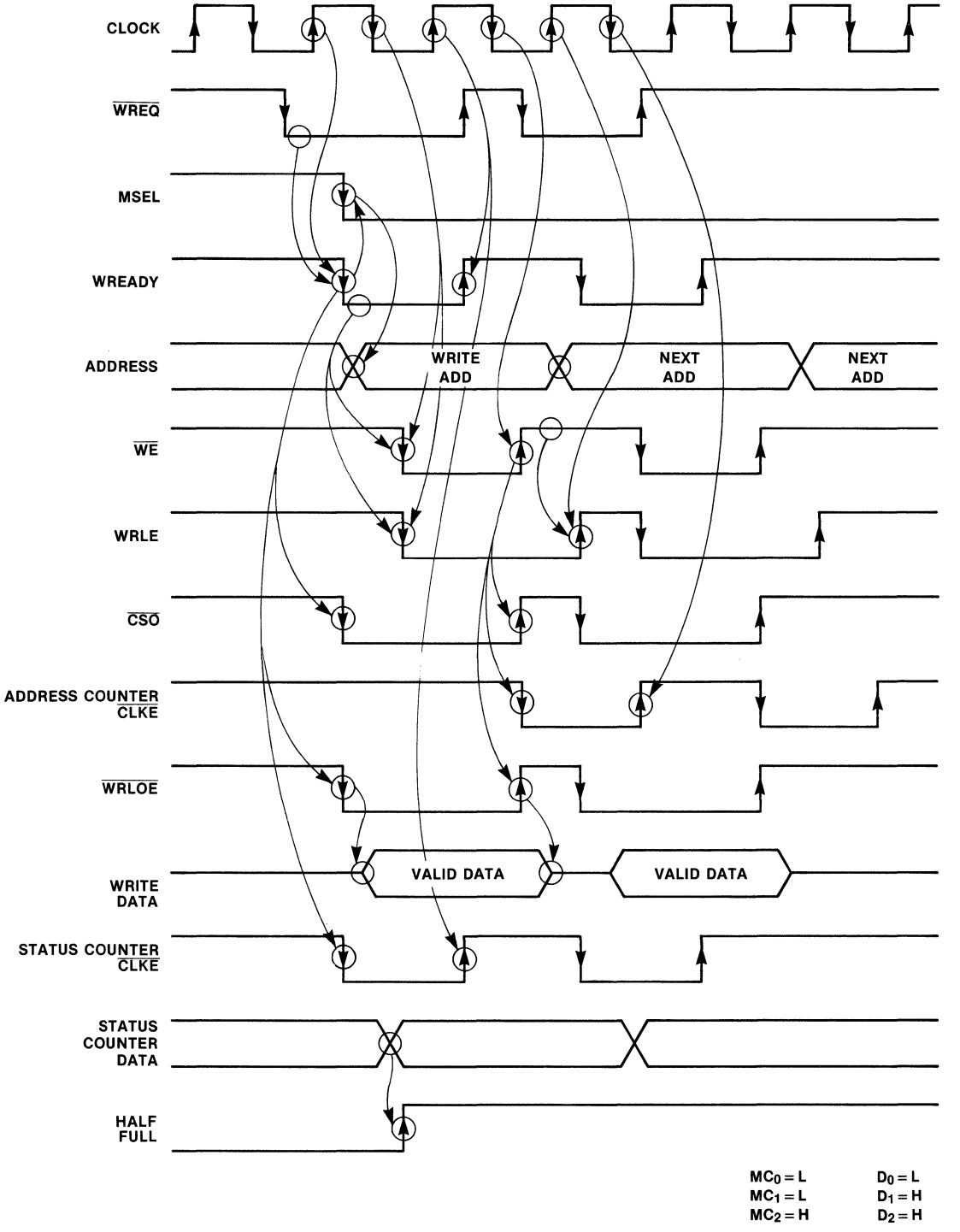
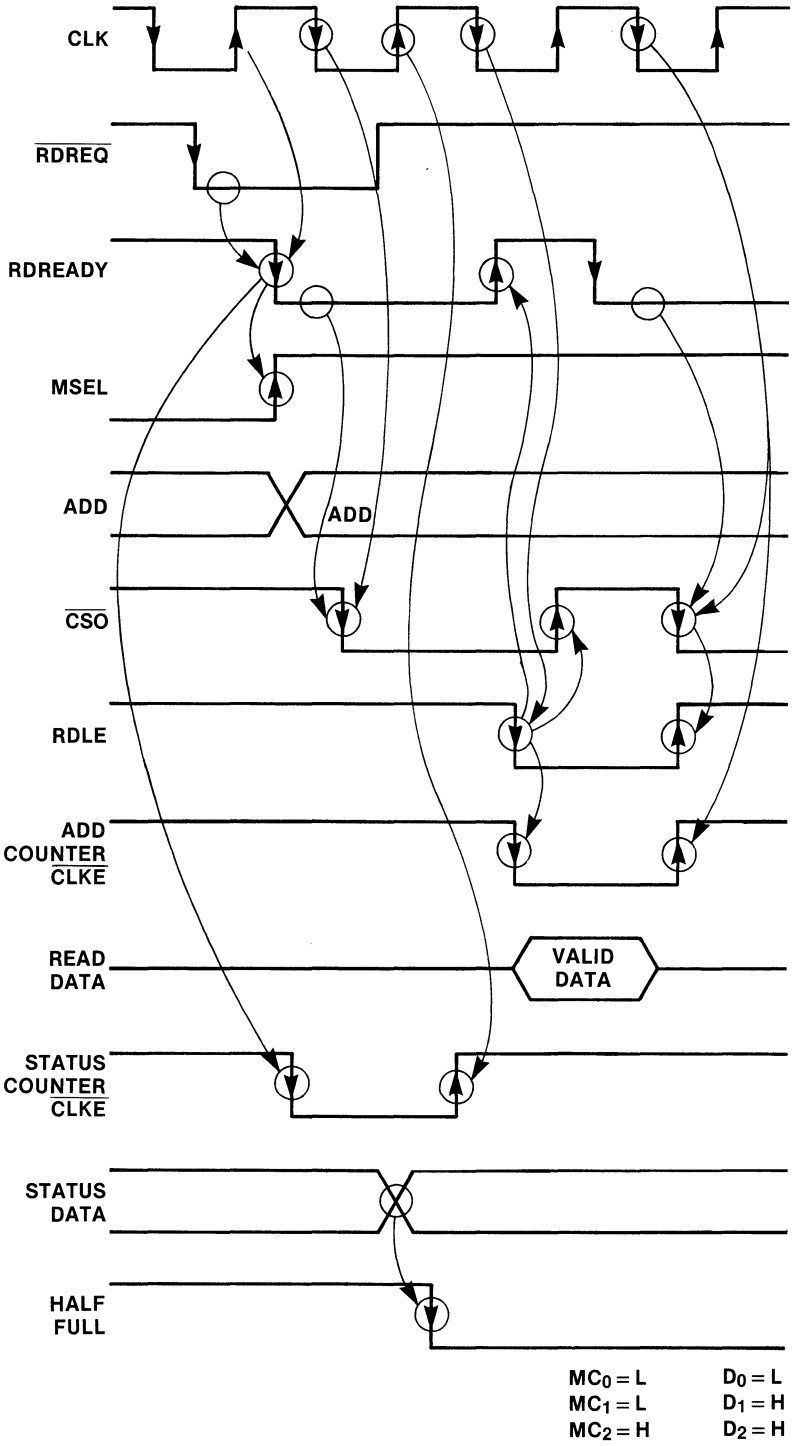


Fig. 411-b Read Cycle



54F/74F412

Multi-Mode Buffered Latch With 3-State Outputs

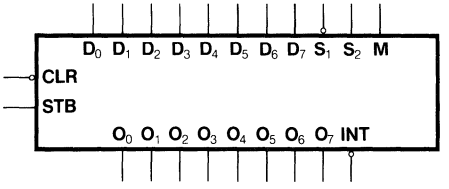
Description

The 'F412 is an 8-bit latch with 3-state output buffers. Also included is a status flip-flop for providing device-busy or request-interrupt commands. Separate Mode and Select inputs allow data to be stored with the outputs enabled or disabled. The device can also operate in a fully transparent mode. The 'F412 is the functional equivalent of the Intel 8212.

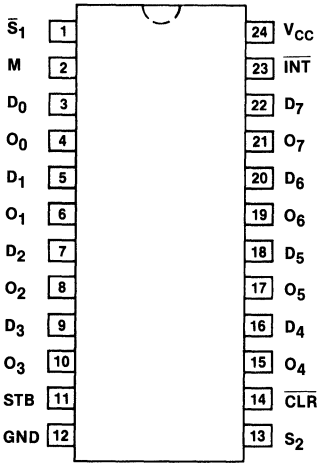
- **3-State Outputs**
- **Status Flip-flop for Interrupt Commands**
- **Asynchronous or Latched Receiver Modes**
- **300 mil 24-Pin Slim Package**

Ordering Code: See Section 5

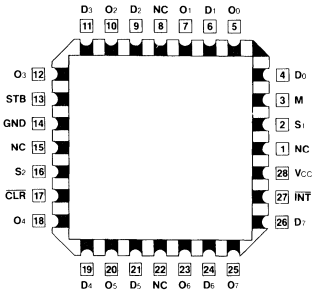
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
O_0-O_7	Latch Outputs	75/15 (12.5)
D_0-D_7	Data Inputs	0.5/0.375
$\overline{CLR}$	Clear	0.5/0.375
STB	Strobe	0.5/0.375
$\overline{INT}$	Interrupt	25/12.5
M	Mode Control Input	0.5/0.375
$\overline{S}_1$,S_2	Select Inputs	0.5/0.375

Functional Description

This high-performance eight-bit parallel expandable buffer register incorporates package and mode selection inputs and an edge-triggered status flip-flop designed specifically for implementing bus-organized input/output ports. The 3-state data outputs can be connected to a common data bus and controlled from the appropriate select inputs to receive or transmit data. An integral status flip-flop provides busy or request interrupt commands.

The eight data latches are fully transparent when the internal gate enable, G, input is HIGH and the outputs are enabled. Latch transparency is selected by the mode control (M), select ($\overline{S}_1$ and S_2), and the strobe (STB) inputs and during transparency each data output (O_n) follows its respective data input (D_n). This mode of operation can be terminated by clearing, de-selecting, or holding the data latches.

An input mode or an output mode is selectable from the M input. In the input mode, M = L, the eight data latch inputs are enabled when the strobe is HIGH regardless of device selection. If selected during an input mode, the outputs will follow the data inputs. When the strobe input is taken LOW, the latches will store the most-recently setup data.

In the output mode, M = H, the output buffers are enabled regardless of any other control input. During the output mode the content of the register is under control of the select ($\overline{S}_1$ and S_2) inputs.

4

Data Latches Function Table

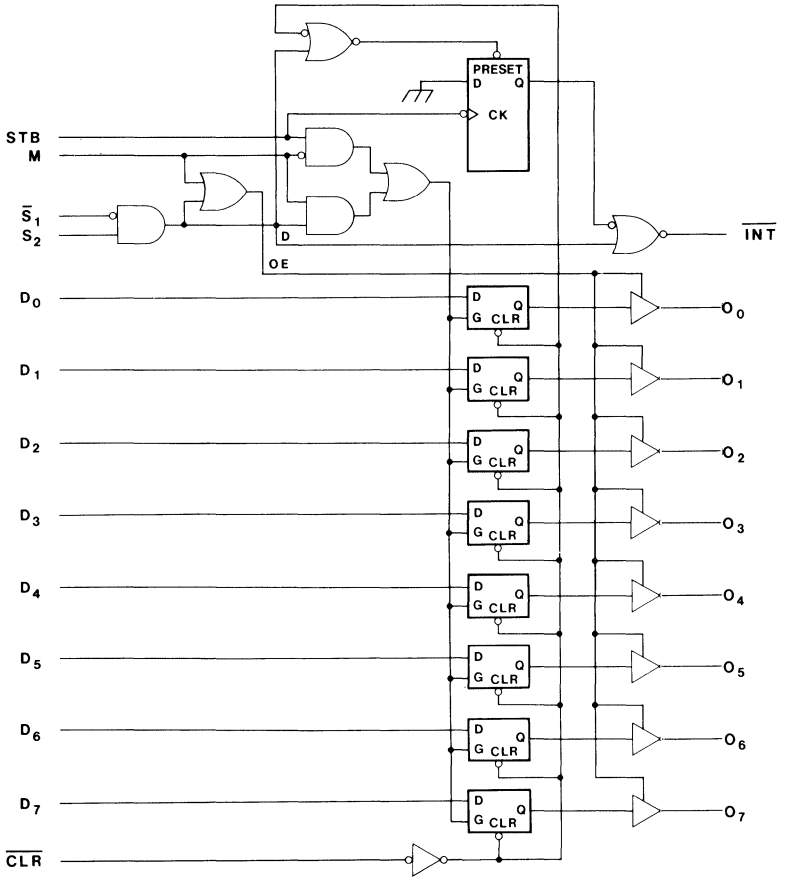
Function	$\overline{CLR}$	M	$\overline{S}_1$	S_2	STB	Data In	Data Out
Clear	L	H	H	X	X	X	L
	L	L	L	H	L	X	L
De-select	X	L	X	L	X	X	Z
	X	L	H	X	X	X	Z
Hold	H	H	H	L	X	X	Q_0
	H	L	L	H	L	X	Q_0
Data Bus	H	H	L	H	X	L	L
	H	H	L	H	X	H	H
Data Bus	H	L	L	H	H	L	L
	H	L	L	H	H	H	H

Status Flip-flop Function Table

$\overline{CLR}$	$\overline{S}_1$	S_2	STB	$\overline{INT}$
L	H	X	X	H
L	X	L	X	H
H	X	X	⌐	L
H	L	H	X	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CCH}	Power Supply Current		33	50	mA	V_{CC} = Max
I_{CCL}			40	60		
I_{CCZ}			40	60		

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F $T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$			54F $T_A, V_{CC} =$ Mil $C_L = 50\ pF$		74F $T_A, V_{CC} =$ Com $C_L = 50\ pF$		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to O_n	3.5 2.5	6.5 5.0	8.5 6.5	3.0 2.0	11.5 8.5	3.0 2.0	9.5 7.5	ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay $\overline{S}_1$, S_2 or STB to O_n	8.5 7.5	14.5 12.5	18.5 16.0	6.5 6.0	23.0 19.0	7.5 6.5	20.5 17.5	ns	3-1 3-7
t_{PLH} t_{PHL}	Propagation Delay $\overline{S}_1$ or S_2 to $\overline{INT}$	4.5 4.5	7.5 8.0	9.5 10.5	3.5 3.5	12.0 12.5	4.0 4.0	10.5 11.5	ns	3-1 3-10
t_{PHL}	Propagation Delay $\overline{CLR}$ to O_n	7.5	12.5	16.0	5.5	18.5	6.5	17.5	ns	3-1 3-9
t_{PHL}	Propagation Delay STB to $\overline{INT}$	6.5	11.0	14.0	5.5	17.5	5.5	15.0	ns	3-1 3-10
t_{PZH} t_{PZL}	Access Time, HIGH or LOW $\overline{S}_1$ to O_n	8.0 6.5	12.5 11.0	18.0 14.0	6.5 5.5	20.0 18.0	7.0 5.5	19.0 15.0	ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Disable Time, HIGH or LOW $\overline{S}_1$ to O_n	4.5 6.5	8.0 11.0	10.5 14.0	4.0 5.5	14.5 17.0	4.0 5.5	11.5 15.0		
t_{PZH} t_{PZL}	Access Time, HIGH or LOW S_2 to O_n	7.5 5.0	12.5 9.0	16.0 11.5	6.5 4.0	18.5 15.5	6.5 4.5	17.5 12.5	ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Disable Time, HIGH or LOW S_2 to O_n	4.5 5.5	7.5 9.5	9.5 12.0	3.5 4.5	12.5 14.5	4.0 4.5	10.5 13.0		
t_{PZH} t_{PZL}	Access Time, HIGH or LOW M to O_n	5.0 5.0	8.5 8.5	11.0 11.0	4.5 4.0	16.0 15.0	4.5 4.5	12.0 12.0	ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Disable Time, HIGH or LOW M to O_n	4.0 5.0	7.0 8.5	9.0 11.0	3.5 4.5	11.5 14.0	3.5 4.5	10.0 12.0		

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW D_n to $\overline{S}_1$, S_2 or STB	0 0	2.0 2.0	1.0 1.0	ns	3-15
$t_h(H)$ $t_h(L)$	Hold Time D_n to $\overline{S}_1$, S_2 or STB	8.0 8.0	10.0 10.0	9.0 9.0		
$t_w(H)$ $t_w(L)$	$\overline{S}_1$, S_2 or STB Pulse Width, HIGH or LOW	8.0 8.0	11.0 11.0	9.0 9.0	ns	3-9
$t_w(L)$	$\overline{CLR}$ Pulse Width, LOW	8.0	11.5	9.0	ns	3-9

54F/74F413

64x4 First-In First-Out Buffer Memory With Serial and Parallel I/O

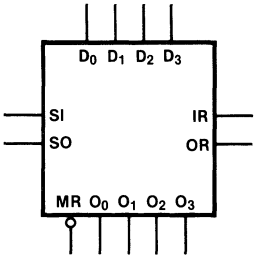
Description

The 'F413 is an expandable fall-through type high-speed First-In First-Out (FIFO) buffer memory organized as 64 words by four bits. The 4-bit input and output registers record and transmit, respectively, asynchronous data in parallel form. Control pins on the input and output allow for handshaking and expansion. The 4-bit wide, 62-bit deep fall-through stack has self-contained control logic.

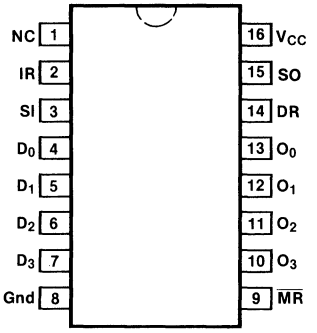
- **Separate Input and Output Clocks**
- **Serial or Parallel Input and Output**
- **Expandable without External Logic**
- **15 MHz Data Rate**
- **Supply Current 160 mA Max**

Ordering Code: See Section 5

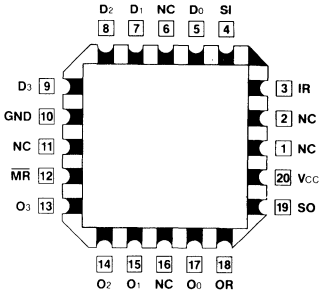
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
D_0-D_3	Data Inputs	0.5/0.375
O_0-O_3	Data Outputs	25/12.5
IR	Input Ready	0.5/0.375
SI	Shift In	0.5/0.375
SO	Shift Out	0.5/0.375
$\overline{OR}$	Output Ready	0.5/0.375
$\overline{MR}$	Master Reset	0.5/0.375

Functional Description

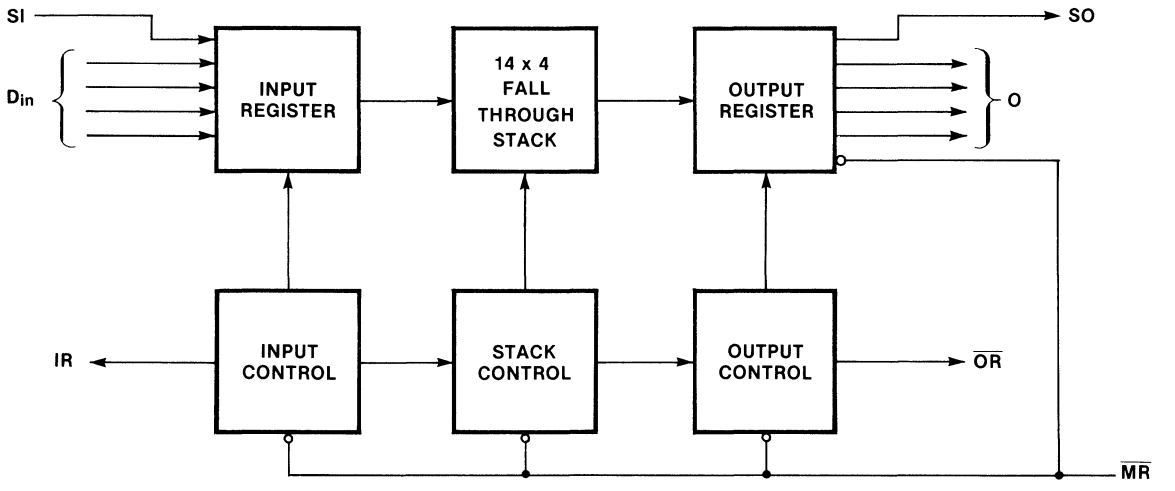
Data Input—Data is entered into the FIFO on D_0-D_3 inputs. To enter data the Input Ready (IR) should be HIGH, indicating that the first location is ready to accept data. Data then present at the four data inputs is entered into the first location when the Shift In (SI) is brought HIGH. An SI HIGH signal causes the IR to go LOW. Data remains at the first location until SI is brought LOW. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating that more room is available. Simultaneously, data will propagate to the second location and continue shifting until it reaches the output stage or a full location. If the memory is full, IR will remain LOW.

Data Transfer—Once data is entered into the second cell, the transfer of any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will 'bubble' to the front. The t_{PT} parameter defines the time required for the first data to travel from input to the output of a previously empty device.

Data Output—Data is read from the O_0-O_3 outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW, the upstream data, provided that stage has valid data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW, and O_0-O_3 remains as before, i.e., data does not change if FIFO is empty.

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t_{PT}) or completely empty (Output Ready stays LOW for at least t_{PT}).

Block Diagram



DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		115	160	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units
		T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
f_{max}	Shift In Rate	10							MHz
f_{max}	Shift Out Rate	10							MHz
t_{PLH} t_{PHL}	Propagation Delay Shift In to IR		45.0 45.0						ns
t_{PLH} t_{PHL}	Propagation Delay Shift Out to OR		55.0 55.0						ns
t_{PLH} t_{PHL}	Propagation Delay Output Data Delay		55.0 55.0						ns
t_{PLH}	Propagation Delay Master Reset to IR		60.0						ns
t_{PHL}	Propagation Delay Master Reset to OR		60.0						ns

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com	
		Min Typ Max	Min Max	Min Max	
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW D_n to SI	5.0 5.0			ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW SI to D_n	45.0 45.0			
$t_w(H)$ $t_w(L)$	Shift In Pulse Width HIGH or LOW	35.0 35.0			ns
$t_w(H)$ $t_w(L)$	Shift Out Pulse Width HIGH or LOW	35.0 35.0			
$t_w(H)$	Input Ready Pulse Width, HIGH	20.0			ns
$t_w(L)$	Output Ready Pulse Width, LOW	20.0			ns
$t_w(H)$ $t_w(L)$	Master Reset Pulse Width HIGH or LOW	35.0 35.0			ns
t_{rec}	Recovery Time, MR to SI	35.0			ns
t_{PT}	Data Throughput Time	3.0			μs

54F/74F418

32-Bit Memory Error Detection And Correction Circuit

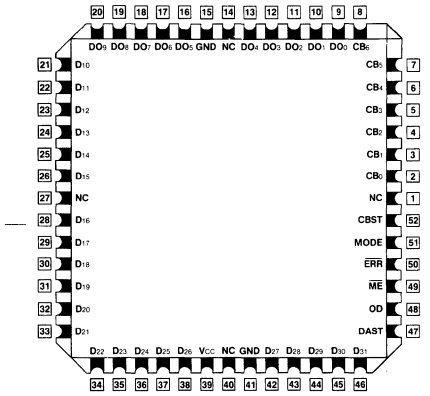
Description

The 'F418 Memory Error Detection And Correction (EDAC) circuit contains the logic to generate seven check bits on a 32-bit data field, according to a modified Hamming code. The check bits are then stored in memory with the data word. On a subsequent read from memory, the device will detect and correct any single-bit data error, and detect any double-bit error.

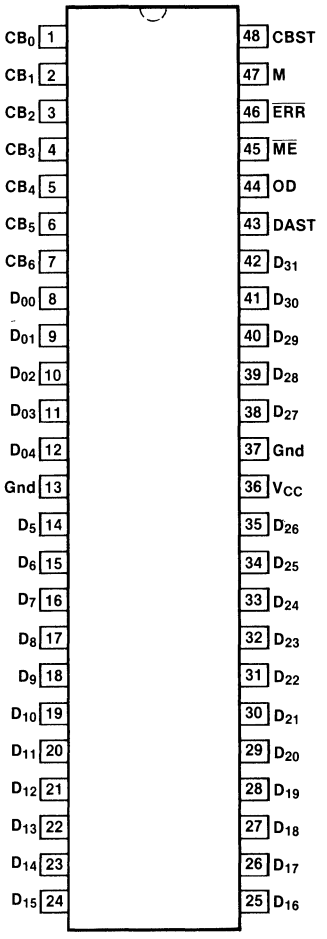
The 'F418 is fully compatible with all TTL families. Data and check bit signals are bidirectional 3-state lines.

- **Increases Memory System Reliability**
- **Corrects Single-Bit Errors in 60 ns**
- **Detects Double-Bit Errors in 85 ns**

Connection Diagrams



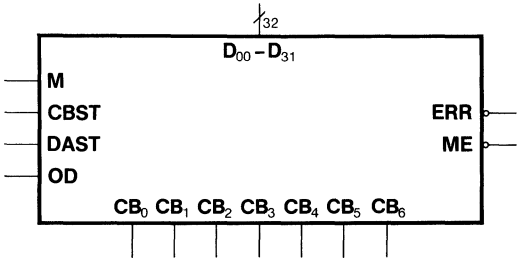
Pin Assignment for LCC and PCC



Pin Assignment for DIP

Ordering Code: See Section 5

Logic Symbol



Input Loading/Fan-Out: See Section 3 for U.L. definitions

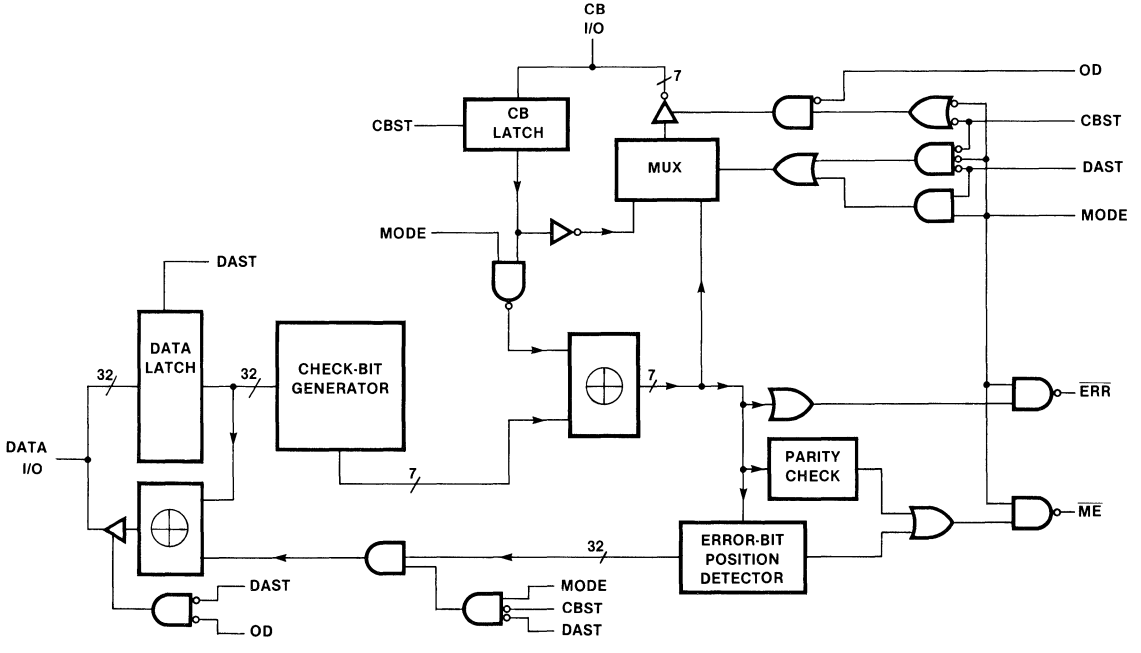
Pin Names	Description	54F/74F(U.L.) HIGH/LOW
D_0-D_{31}	Data Input/ Output Lines	0.5/0.375 75/15 (12.5)
CB_0-CB_6	Check Bit Input/ Output Lines	0.5/0.375 75/15 (12.5)
DAST	Data Strobe	0.5/0.375
OD	Output Disable	0.5/0.375
$\overline{ME}$	Multiple Error	25/12.5
$\overline{ERR}$	Error	25/12.5
MODE	Mode	0.5/0.375
CBST	Check Bit Strobe	0.5/0.375

Functional Description

During generate mode, MODE is LOW, CB_2 through CB_5 are calculated so that the indicated bits are an even number of ones (i.e. even parity) while CB_0, CB_1, and CB_6 are calculated for an odd number of ones. This modification of the Hamming code makes the device respond to a memory read of all ones or all zeroes (all 39 bits) with an $\overline{ME}$ indication.

During correction mode, with DAST LOW and CBST LOW, the fail pattern will be placed on the CB I/O lines. Each zero in the fail pattern indicates a discrepancy between that particular bit in the input (latched) checkbit (based on D_0 through D_{31}). A fail pattern of all ones indicates no error. A single zero indicates that the corresponding bit is in error and no correction of the data is required. This situation is still flagged with a LOW $\overline{ERR}$.

Block Diagram



Function Table

Control Inputs			Outputs			Function
DAST	MODE	CBST	DATA I/O*	CB I/O*	$\overline{ERR}$, $\overline{ME}$	
0	0	0	O/P Latched Data	O/P Latched CB's	1	Read Latches
0	0	1	O/P	O/P New CB's	1	Latched, Generate CB's
0	1	0	O/P Corrected Data	O/P Syndromes	Active	Correct
0	1	1	O/P Uncorrected Data	O/P Latched CB's	Active	Monitor w/Latched Data
1	0	X	I/P	O/P New CB's	1	Unlatched Data, Generate CB's
1	1	0	I/P	O/P Latched CB's	Active	Monitor w/Latched CB's
1	1	1	I/P	I/P	Active	Monitor Inputs

*OD must be LOW to enable the output drivers

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current			400	mA	V_{CC} = Max, OD = 4.5 V

AC Characteristics: See Section 3 for waveforms and load configurations

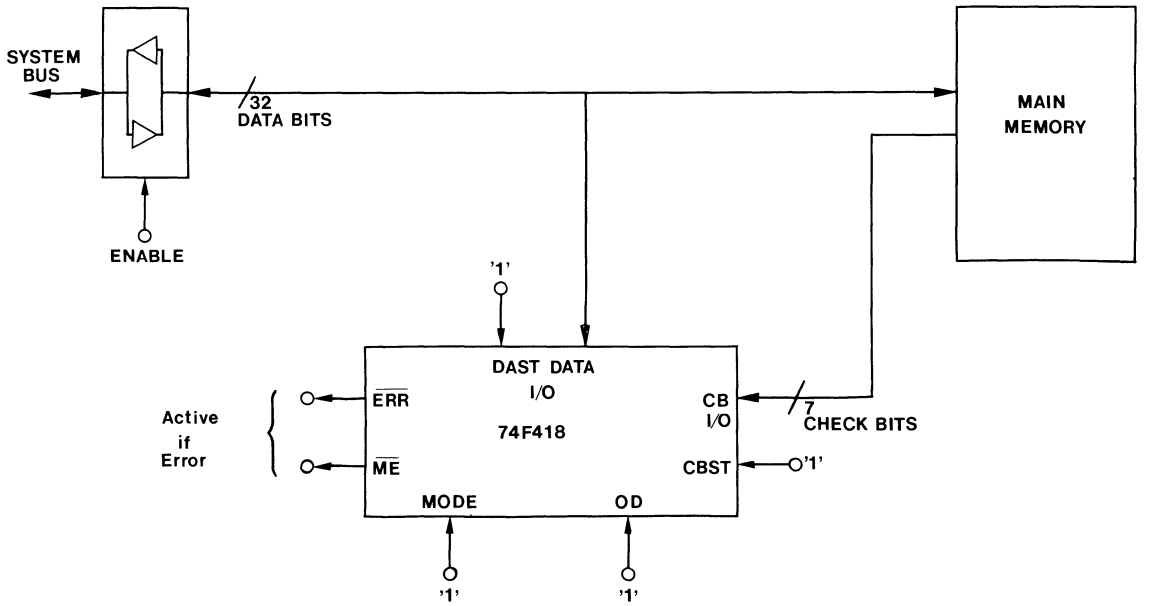
Symbol	Parameter	54F/74F	54F	74F	Units
		$T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$	T_A, V_{CC} = Mil $C_L = 50\ pF$	T_A, V_{CC} = Com $C_L = 50\ pF$	
		Min Typ Max	Min Max	Min Max	
t_{PLH} t_{PHL}	Propagation Delay Data to CB	63.0 63.0			ns
t_{PLH} t_{PHL}	Propagation Delay Data or Check Bit to $\overline{ERR}$	55.0 55.0			ns
t_{PLH} t_{PHL}	Propagation Delay Data or Check Bit to $\overline{ME}$	75.0 75.0			ns
t_{PLH} t_{PHL}	Propagation Delay MODE to $\overline{ERR}$	23.0 23.0			ns
t_{PLH} t_{PHL}	Propagation Delay MODE to $\overline{ME}$	24.0 24.0			ns
t_{PLH} t_{PHL}	Propagation Delay MODE to Corrected Data	52.0 52.0			ns
t_{PLH} t_{PHL}	Propagation Delay MODE to Syndromes	35.0 35.0			ns
t_{PLH} t_{PHL}	Propagation Delay DAST+ to $\overline{ERR}$	68.0 68.0			ns
t_{PLH} t_{PHL}	Propagation Delay DAST+ to $\overline{ME}$	86.0 86.0			ns
t_{PLH} t_{PHL}	Propagation Delay CBST+ to $\overline{ERR}$	43.0 43.0			ns
t_{PLH} t_{PHL}	Propagation Delay CBST+ to $\overline{ME}$	50.0 50.0			ns
t_{PLH} t_{PHL}	Propagation Delay DAST+ to Corrected Data	84.0 84.0			ns
t_{PLH} t_{PHL}	Propagation Delay CBST+ to Syndromes	70.0 70.0			ns
t_{PHZ} t_{PLZ}	Enable Times	22.0 22.0			ns
t_{PZH} t_{PZL}	Disable Times	24.0 24.0			ns

AC Operating Requirements: See Section 3 for waveforms

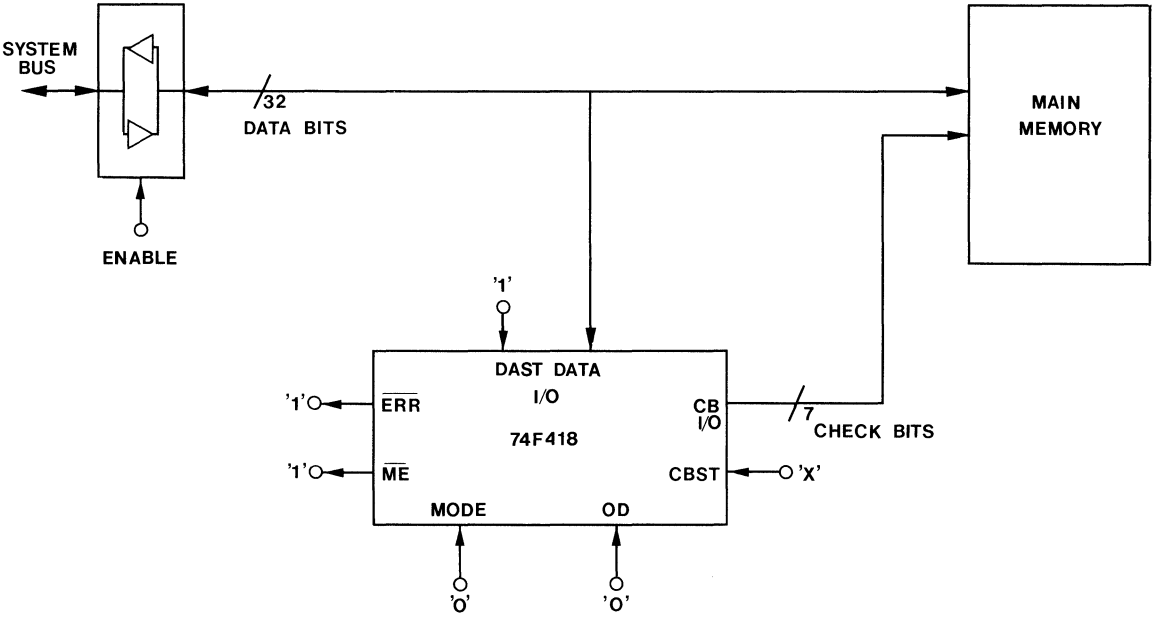
Symbol	Parameter	54F/74F	54F	74F	Units
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com	
		Min Typ Max	Min Max	Min Max	
$t_s(H)$	Setup Time, HIGH Data to DAST-	11.0			ns
$t_h(H)$	Hold Time, HIGH DAST- to Data	9.0			
$t_s(L)$	Setup Time, LOW Check Bits to CBST+	7.0			ns
$t_h(L)$	Hold Time, LOW CBST- to Check Bits	7.0			
$t_w(H)$	DAST Pulse Width	26.0			ns
$t_w(H)$	CBST Pulse Width	15.0			ns

4

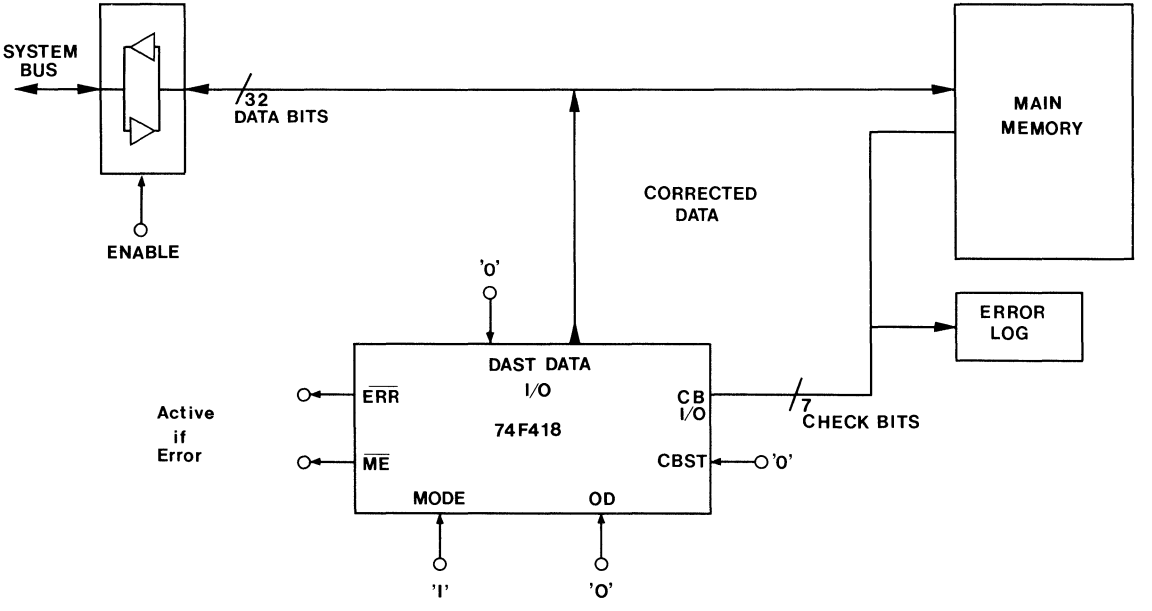
Memory Read Operation
Check for Error



Memory Write Operation



Single-Bit Error Correction



54F/74F420

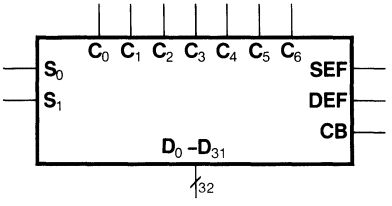
Parallel Check Bit/Syndrome Bit Generator

Description

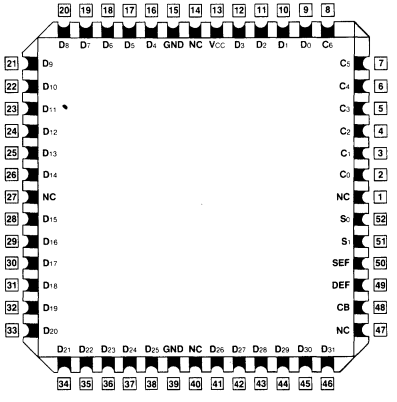
The 'F420 is a parallel check bit/syndrome bit generator. The 'F420 utilizes a modified hamming code to generate 7 check bits from a 32-bit dataword, in 15 ns, when operated in the check bit generate mode. When operated in the syndrome generate mode, the check bits and data bits read from memory are utilized in a parity summer to generate syndrome bits upon error detection. The maximum error count detectable is 2. A single error detect can occur in 18 ns; a double error detect in 22 ns. The syndrome bit generation can be output in 15 ns (maximum).

Ordering Code: See Section 5

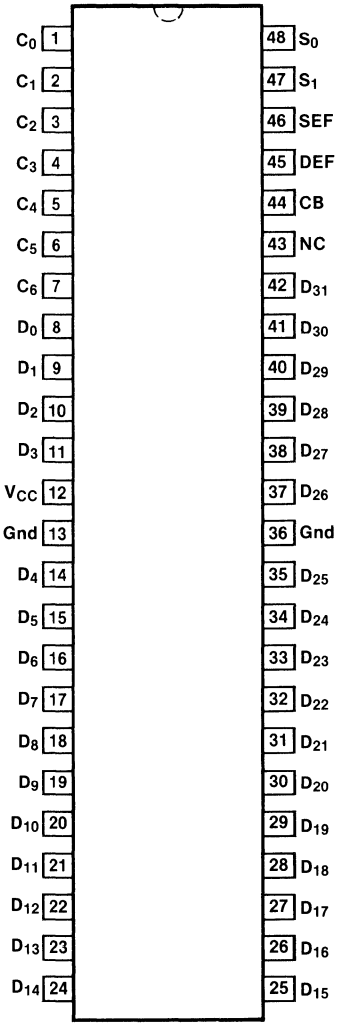
Logic Diagram



Connection Diagrams



Pin Assignment for LCC and PCC



Pin Assignment for DIP

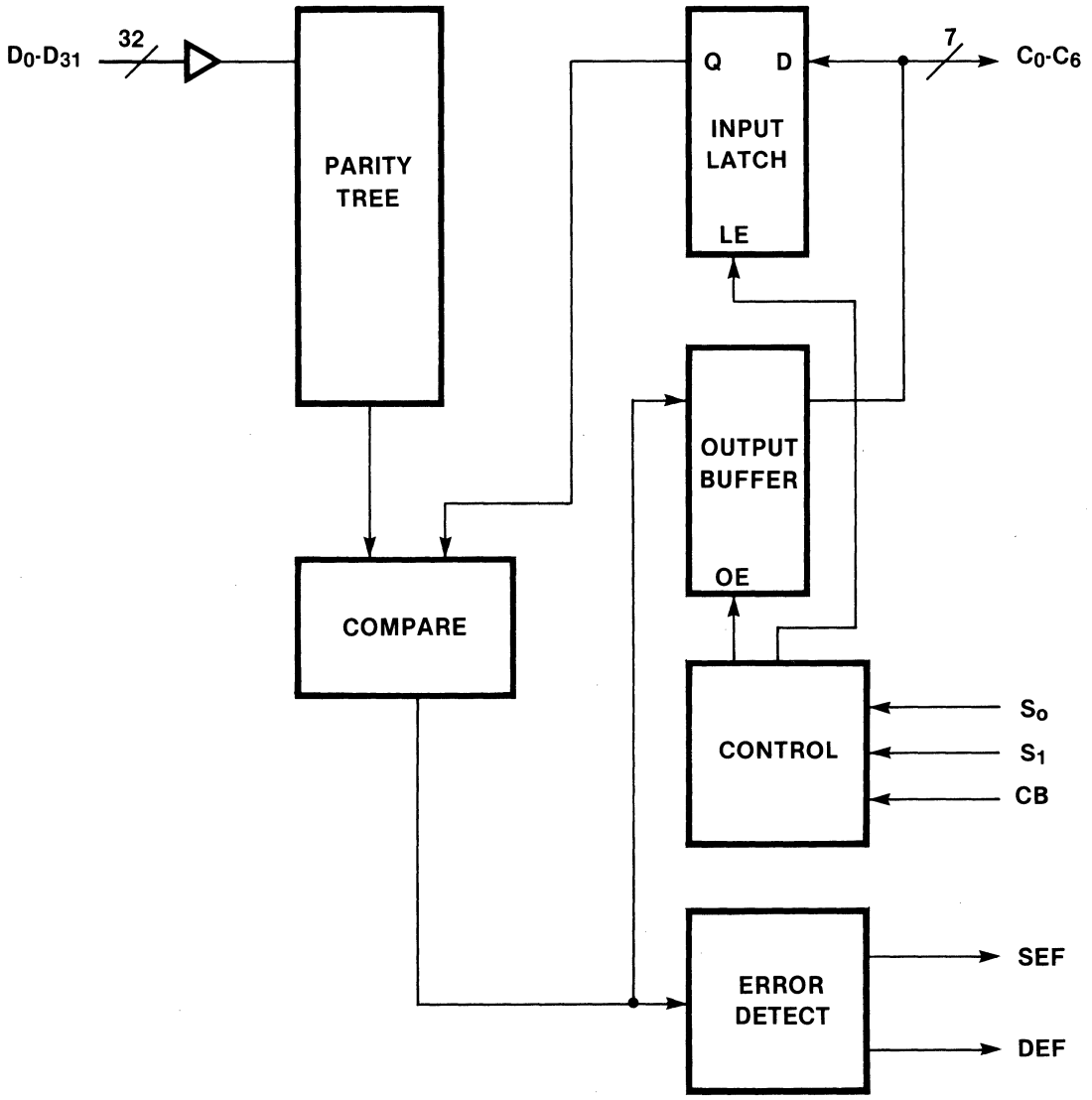
Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
C_0-C_6	Check Bit/Syndrome Bus	0.5/0.375
D_0-D_{31}	Data Bit Bus	0.5/0.375
CB	Check Bit Control	0.5/0.375
DEF	Double Error Flag	25/12.5
SEF	Single Error Flag	25/12.5
S_0-S_1	Mode Control	0.5/0.375

Function Table

Memory Cycle	Function	Control S_1	Control S_0	Check Bit	CB Control I/O	Error Flags SEF	Error Flags DEF
Write	Generate Check Bits	L	L	Output Check	L	H	H
Read	Read & Flag	H	L	Input	H	Enabled	
Read	Latch Check Bits	H	H	Inputs	H	Enabled	
Read	Output Syndrome Bits	H	H	Output Syndrome Bits	L	Enabled	
Diagnostics	Input Diagnostic Data Word	H	H	Latched Check Outputs High Z	H	Enabled	
Diagnostics	Input Diagnostic Data Word	L	H	Output Latched Check Bits	L	Enabled	
Diagnostics	Input Diagnostic Data Word	H	H	Output Syndrome Bits	L	Enabled	

Block Diagram



DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		125	200	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units
		T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay Check Bit Generate			20.0 20.0					ns
t_{PLH} t_{PHL}	Propagation Delay Single Error Detect			20.0 20.0					ns
t_{PLH} t_{PHL}	Propagation Delay Multiple Error Detect			30.0 30.0					ns
t_{PLH} t_{PHL}	Propagation Delay Select to Syndrome			15.0 15.0					ns
t_{PZH} t_{PZL}	Output Enable Time			10.0 10.0					ns
t_{PHZ} t_{PLZ}	Output Disable Time			10.0 10.0					ns

Fig. 420-a Timing Waveforms

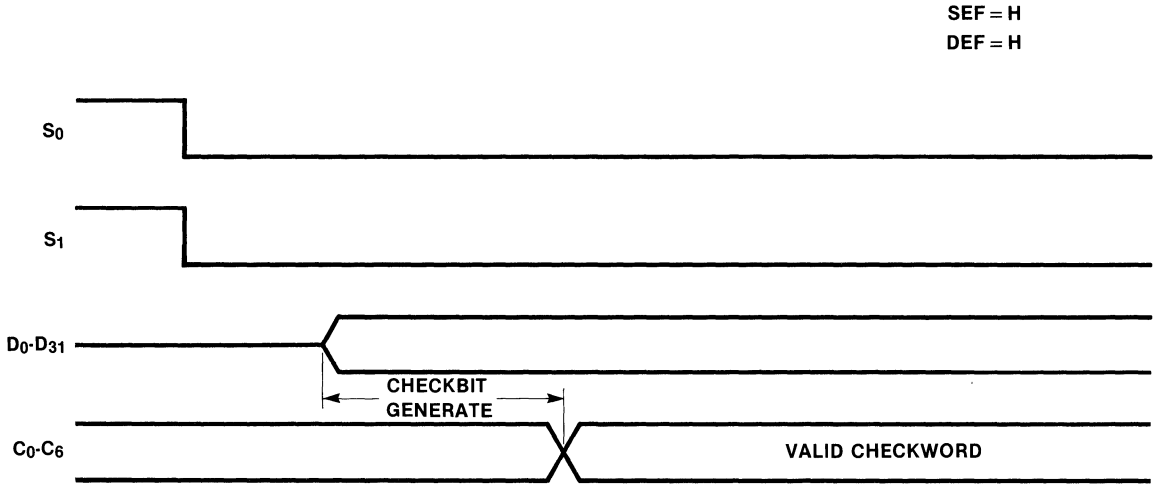
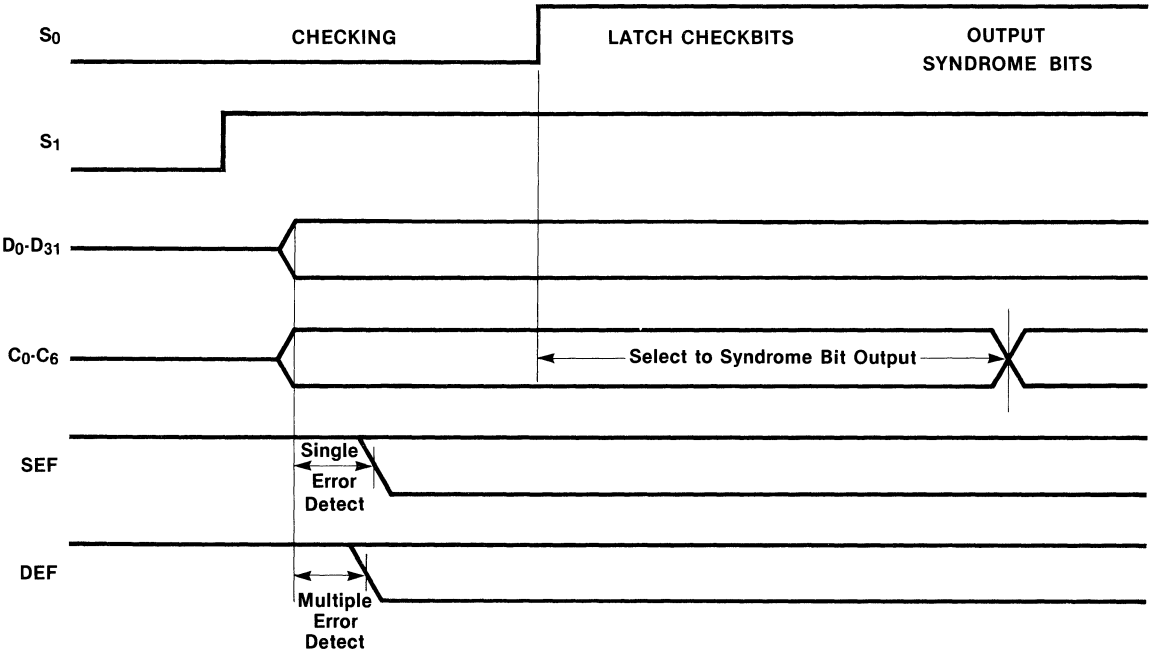


Fig. 420-b Timing Waveforms



54F/74F432

Multi-Mode Buffered Latch With 3-State Outputs

Description

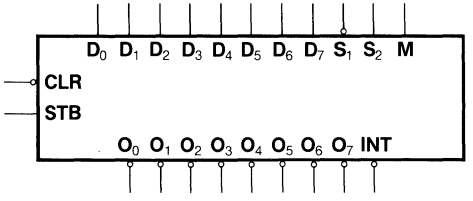
The 'F432 is an 8-bit latch with 3-state output buffers and control and device selection logic. Also included is a status flip-flop for providing device-busy or request-interrupt commands. Separate Mode and Select inputs allow data to be stored with the outputs enabled or disabled. The device can also operate in a fully transparent mode.

The 'F432 is the functional equivalent of the Intel 8212, but with inverting outputs.

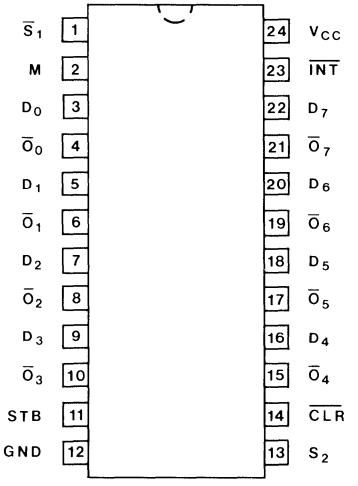
- 3-State Inverting Outputs
- Status Flip-Flop for Interrupt Commands
- Asynchronous or Latched Receiver Modes
- Data to Output Propagation Delay Typically 8.5 ns
- Supply Current 43 mA Typ
- 24-Pin Slim Package

Ordering Code: See Section 5

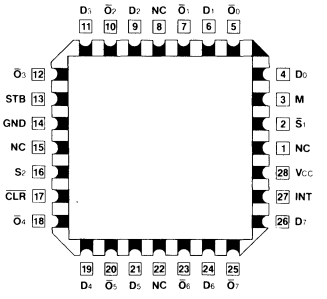
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
D_0-D_7	Data Inputs	0.5/0.375
$\overline{O}_0$-$\overline{O}_7$	Latch Outputs	75/15 (12.5)
$\overline{S}_1$,S_2	Select Inputs	0.5/0.375
M	Mode Control Input	0.5/0.375
STB	Strobe	0.5/0.375
$\overline{INT}$	Interrupt	25/12.5
$\overline{CLR}$	Clear	0.5/0.375

Functional Description

This high-performance eight-bit parallel expandable buffer register incorporates package and mode selection inputs and an edge-triggered status flip-flop designed specifically for implementing bus-organized input/output ports. The 3-state data outputs can be connected to a common data bus and controlled from the appropriate select inputs to receive or transmit data. An integral status flip-flop provides busy or request interrupt commands.

The eight data latches are fully transparent when the internal gate enable, G, input is HIGH and the outputs are enabled. Latch transparency is selected by the mode control (M), select ($\overline{S}_1$ and S_2), and the strobe (STB) inputs and during transparency each data output ($\overline{O}_n$) follows its respective data input (D_n). This mode of operation can be terminated by clearing, de-selecting, or holding the data latches. See Data Latches Function Table.

An input mode or an output mode is selectable from this single input line. In the input mode, M = L, the eight data latch inputs are enabled when the strobe is HIGH regardless of device selection. If selected during an input mode, the outputs will follow the data inputs. When the strobe input is taken LOW the latches will store the most recently setup data.

In the output mode, M = H, the output buffers are enabled regardless of any other control input. During the output mode the content of the register is under control of the select ($\overline{S}_1$ and S_2) inputs. See Data Latches Function Table.

4

Data Latches Function Table

Function	$\overline{CLR}$	M	$\overline{S}_1$	S_2	STB	Data In	Data Out
Clear	L	H	H	X	X	X	H
	L	L	L	H	L	X	H
De-select	X	L	X	L	X	X	Z
	X	L	H	X	X	X	Z
Hold	H	H	H	L	X	X	$\overline{Q}_0$
	H	L	L	H	L	X	$\overline{Q}_0$
Data Bus	H	H	L	H	X	L	H
	H	H	L	H	X	H	L
Data Bus	H	L	L	H	H	L	H
	H	L	L	H	H	H	L

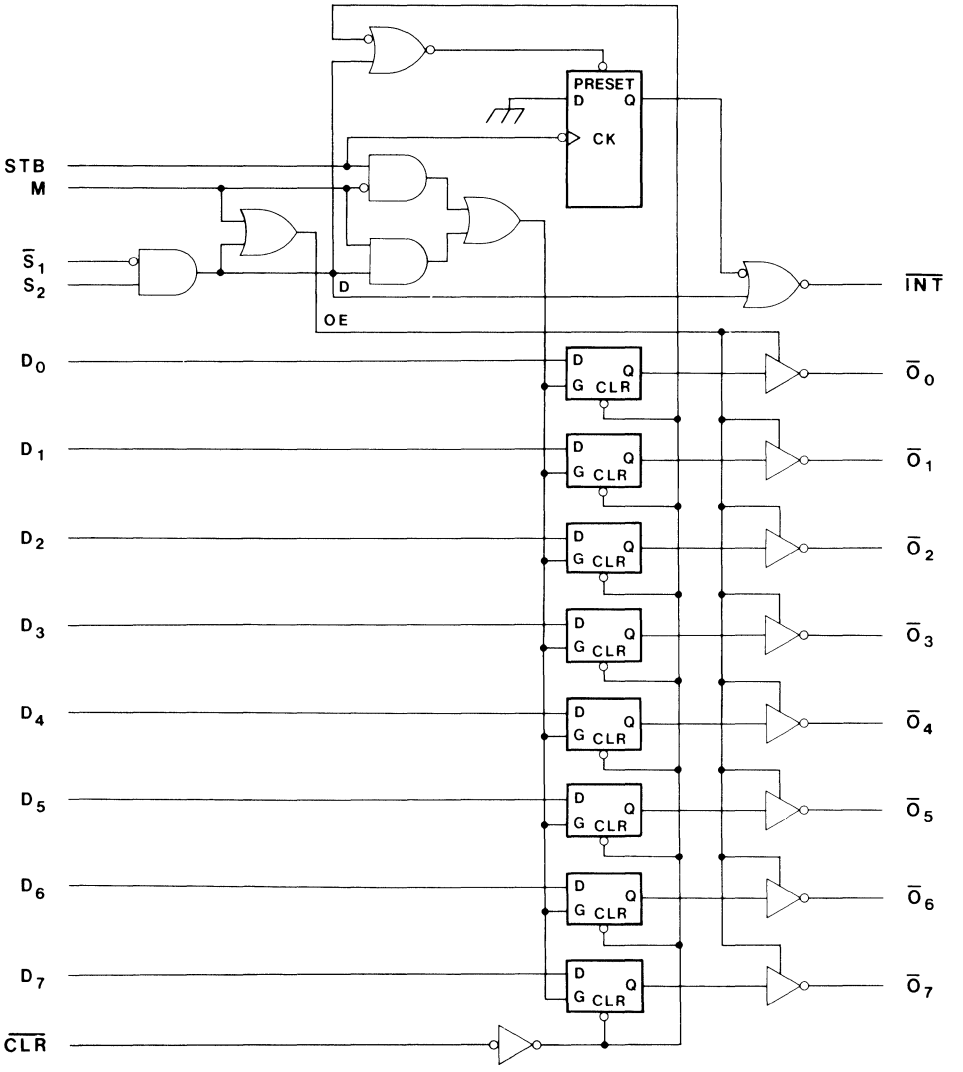
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Status Flip-Flop Function Table

$\overline{CLR}$	$\overline{S}_1$	S_2	STB	$\overline{INT}$
L	H	X	X	H
L	X	L	X	H
H	X	X	↑	L
H	L	H	X	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↑ = LOW-to-HIGH Transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CCH}	Power Supply Current		43	65	mA	V_{CC} = Max
I_{CCL}			29	43		
I_{CCZ}			29	43		

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	3.5	8.5	10.5			3.0	12.0	ns	3-1
t_{PHL}	D_n to O_n	2.5	5.5	7.0			3.0	12.0		3-3
t_{PLH}	Propagation Delay	8.5	16.0	21.0			7.5	23.0	ns	3-1
t_{PHL}	$\overline{S}_1$, S_2 or STB to $\overline{O}_n$	6.5	12.5	16.0			5.5	18.0		3-7
t_{PHL}	Propagation Delay $\overline{CLR}$ to $\overline{O}_n$	7.0	15.0	18.5			6.0	20.5	ns	3-1, 3-9
t_{PHL}	Propagation Delay STB to $\overline{INT}$	6.0	11.5	14.5			5.0	16.0	ns	3-1, 3-10
t_{PLH}	Propagation Delay $\overline{S}_1$ or S_2 to $\overline{INT}$	4.0	7.5	9.5			3.5	10.5	ns	3-1, 3-10
t_{PLH}	Propagation Delay	9.0	15.0	19.0			9.0	20.0	ns	3-1
t_{PHL}	M to $\overline{O}_n$	6.5	11.0	14.0			6.5	15.0		3-3
t_{PZH}	Enable Time	4.5	13.0	18.0			4.0	20.0	ns	3-1, 3-12, 3-13
t_{PZL}	$\overline{S}_1$, S_2 to $\overline{O}_n$	5.0	11.0	15.0			4.0	17.0		
t_{PHZ}	Disable Time	4.0	8.0	11.0			3.5	12.5		
t_{PLZ}	$\overline{S}_1$, S_2 to $\overline{O}_n$	5.0	11.0	15.5			4.0	17.5		

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW D_n to $\overline{S}_1$, S_2, STB	0 0		0 0	ns	3-15
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D_n to $\overline{S}_1$, S_2, STB	11.0 8.5		12.5 9.5		
$t_w(H)$ $t_w(L)$	STB, $\overline{S}_1$, S_2 Pulse Width HIGH or LOW	8.0 8.0		9.0 9.0	ns	3-9
$t_w(L)$	$\overline{CLR}$ Pulse Width, LOW	8.0		9.0	ns	3-9

54F/74F433

First-In First-Out (FIFO) Buffer Memory

Description

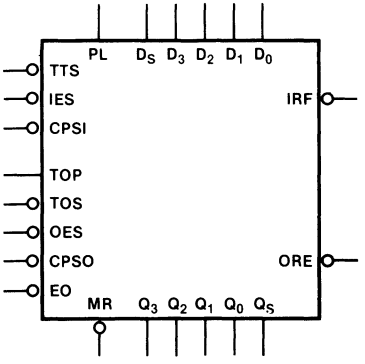
The 'F433 is an expandable fall-through type high-speed first-in first-out (FIFO) buffer memory that is optimized for high-speed disk or tape controller and communication buffer applications. It is organized as 64 words by 4 bits and may be expanded to any number of words or any number of bits in multiples of four. Data may be entered or extracted asynchronously in serial or parallel, allowing economical implementation of buffer memories.

The 'F433 has 3-state outputs that provide added versatility, and is fully compatible with all TTL families.

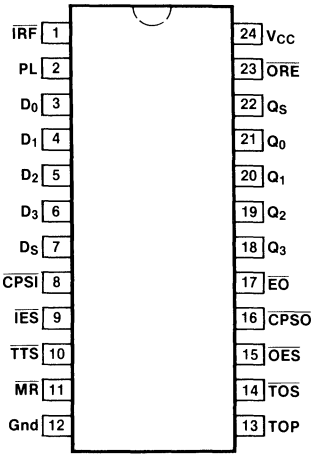
- **Serial or Parallel Input**
- **Serial or Parallel Output**
- **Expandable without Additional Logic**
- **3-State Outputs**
- **Fully Compatible with all TTL Families**
- **Slim 24-Pin Package**

Ordering Code: See Section 5

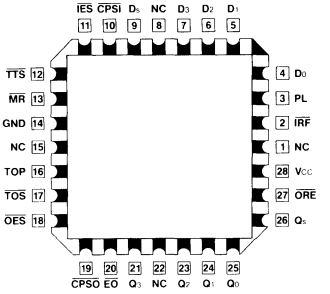
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
PL	Parallel Load Input	1.0/0.23
$\overline{CPSI}$	Serial Input Clock	1.0/0.23
$\overline{IES}$	Serial Input Enable	1.0/0.23
$\overline{TTS}$	Transfer to Stack Input	1.0/0.23
$\overline{MR}$	Master Reset	1.0/0.23
$\overline{OES}$	Serial Output Enable	1.0/0.6
TOP	Transfer Out Parallel	1.0/0.23
$\overline{TOS}$	Transfer Out Serial	1.0/0.23
$\overline{CPSO}$	Serial Output Clock	1.0/0.23
$\overline{OE}$	Output Enable	1.0/0.23
D_0-D_3	Parallel Data Inputs	1.0/0.23
D_S	Serial Data Input	1.0/0.23
Q_0-Q_3	Parallel Data Outputs	130/10
Q_S	Serial Data Output	10/10
$\overline{IRF}$	Input Register Full	10/5
$\overline{ORE}$	Output Register Empty	10/5

Functional Description

As shown in the block diagram, the 'F433 consists of three sections:

1. An Input Register with parallel and serial data inputs, as well as control inputs and outputs for input handshaking and expansion.
2. A 4-bit-wide, 14-word-deep fall-through stack with self-contained control logic.
3. An Output Register with parallel and serial data outputs, as well as control inputs and outputs for output handshaking and expansion.

These three sections operate asynchronously and are virtually independent of one another.

Input Register (Data Entry)

The Input Register can receive data in either bit-serial or 4-bit parallel form. It stores this data until it is sent to the fall-through stack, and also generates the necessary status and control signals.

This 5-bit register (see Figure 1) is initialized by setting flip-flop F_3 and resetting the other flip-flops. The Q-output of the last flip-flop (FC) is brought out as the Input Register Full (IRF) signal. After initialization, this output is HIGH.

Parallel Entry—A HIGH on the Parallel Load (PL) input loads the D_0-D_3 inputs into the F_0-F_3 flip-flops and sets the FC flip-flop. This forces the $\overline{IRF}$ output LOW, indicating that the input register if full. During parallel entry, the Serial Input Clock ($\overline{CPSI}$) input must be LOW.

Serial Entry—Data on the Serial Data (D_S) input is serially entered into the shift register (F_3, F_2, F_1, F_0, FC) on each HIGH-to-LOW transition of the $\overline{CPSI}$ input when the Serial Input Enable ($\overline{IES}$) signal is LOW. During serial entry, the PL input should be LOW.

After the fourth clock transition, the four data bits are located in flip-flops F_0-F_3. The FC flip-flop is set, forcing the $\overline{IRF}$ output LOW and internally inhibiting $\overline{CPSI}$ pulses from affecting the register. Figure 2 illustrates the final positions in an 'F433 resulting from a 256-bit serial bit train (B_0 is the first bit, B_{255} the last).

Fall-Through Stack—The outputs of flip-flops F_0-F_1 feed the stack. A LOW level on the Transfer to Stack ($\overline{TTS}$) input initiates a fall-through action; if the top location of the stack is empty, data is loaded into the stack and the input register is reinitialized. (Note that this initialization is delayed until PL is LOW.) Thus, automatic FIFO action is achieved by connecting the $\overline{IRF}$ output to the $\overline{TTS}$ input.

An RS-type flip-flop (the initialization flip-flop) in the control section records the fact that data has been transferred to the stack. This prevents multiple entry of the same word into the stack even through $\overline{IRF}$ and $\overline{TTS}$ may still be LOW; the initialization flip-flop is not cleared until PL goes LOW.

Once in the stack, data falls through automatically, pausing only when it is necessary to wait for an empty next location. In the 'F433, the master reset ($\overline{MR}$) input only initializes the stack control section and does not clear the data.

Output Register

The Output Register (see Figure 3) receives 4-bit data words from the bottom stack location, stores them, and outputs data on a 3-state, 4-bit parallel data bus or on a 3-state serial data bus. The output section generates and receives the necessary status and control signals.

Parallel Extraction—When the FIFO is empty after a LOW pulse is applied to the MR input, the Output Register Empty ($\overline{ORE}$) output is LOW. After data has been entered into the FIFO and has fallen through to the bottom stack location, it is transferred into the output register, if the Transfer Out Parallel (TOP) input is HIGH. As a result of the data transfer, $\overline{ORE}$ goes HIGH, indicating valid data on the data outputs (provided that the 3-state buffer is enabled). The TOP input can then be used to clock out the next word.

When TOP goes LOW, $\overline{ORE}$ also goes LOW, indicating that the output data has been extracted; however, the data itself remains on the output bus until a HIGH level on TOP permits the transfer of the next word (if available) into the output register. During parallel data extraction, the serial output clock ($\overline{CPSO}$) line should be LOW. The Transfer Out Serial ($\overline{TOS}$) line should be grounded for single-slice operation or connected to the appropriate $\overline{ORE}$ line for expanded operation (refer to the 'Expansion' section).

The TOP signal is not edge-triggered. Therefore, if TOP goes HIGH before data is available from the stack but data becomes available before TOP again goes LOW, that data is transferred into the output register. However, internal control circuitry prevents the same data from being transferred twice. If TOP goes HIGH and returns to LOW before data is available from the stack, $\overline{ORE}$ remains LOW, indicating that there is no valid data at the outputs.

Serial Extraction—When the FIFO is empty after a LOW is applied to the MR input, the $\overline{ORE}$ output is LOW. After data has been entered into the FIFO and has fallen through to the bottom stack location, it is transferred into the output register, if the $\overline{TOS}$ input is LOW and TOP is HIGH. As a result of the data transfer, $\overline{ORE}$ goes HIGH, indicating that valid data is in the register.

The 3-state Serial Data Output (Q_S) is automatically enabled and puts the first data bit on the output bus. Data is serially shifted out on the HIGH-to-LOW transition of $\overline{CPSO}$. To prevent false shifting, $\overline{CPSO}$ should be LOW when the new word is being loaded into the output register. The fourth transition empties the shift register, forces $\overline{ORE}$ LOW, and disables the serial output, Q_S. For serial operation, the $\overline{ORE}$ output may be tied to the $\overline{TOS}$ input, requesting a new word from the stack as soon as the previous one has been shifted out.

Expansion

Vertical Expansion—The 'F433 may be vertically expanded, without external components, to store more words. The interconnections necessary to form a 190-word by 4-bit FIFO are shown in Figure 4. Using the same technique, any FIFO of (63n + 1)-words by 4-bits can be configured, where n is the number of devices. Note that expansion does not sacrifice any of the 'F433 flexibility for serial/parallel input and output.

Horizontal Expansion—The 'F433 can be horizontally expanded, without external logic, to store long words (in multiples of 4-bits). The interconnections necessary to form a 64-word by 12-bit FIFO are shown in Figure 5. Using the same technique, any FIFO of 64-words by 4n-bits can be constructed, where n is the number of devices.

The right-most (most significant) device is connected to the $\overline{TTS}$ inputs of all devices. Similarly, the $\overline{ORE}$ output of the most significant device is connected to the $\overline{TOS}$ inputs of all devices. As in the vertical expansion scheme, horizontal expansion does not sacrifice any of the 'F433 flexibility for serial/parallel input and output.

It should be noted that the horizontal expansion scheme shown in Figure 5 exacts a penalty in speed.

Horizontal and Vertical Expansion—The 'F433 can be expanded in both the horizontal and vertical directions without any external components and without sacrificing any of its FIFO flexibility for serial/parallel input and output. The interconnections necessary to form a 127-word by 16-bit FIFO are shown in Figure 6. Using the same technique, any FIFO of (63m + 1)-words by 4n-bits can be configured, where m is the number of devices in a column and n is the number of devices in a row. Figures 7 and 8 illustrate the timing diagrams for serial data entry and extraction for the FIFO shown in Figure 6. Figure 9 illustrates the final positions of bits in an expanded 'F433 FIFO resulting from a 2032-bit serial bit train.

Interlocking Circuitry—Most conventional FIFO designs provide status signal analogous to $\overline{IRF}$ and $\overline{ORE}$. However, when these devices are operated in arrays, variations in unit-to-unit operating speed require external gating to ensure that all devices have completed an operation. The 'F433 incorporates simple but effective 'master/slave' interlocking circuitry to eliminate the need for external gating.

In the 'F433 array of Figure 6, devices 1 and 5 are the row masters; the other devices are slaves to the master in their rows. No slave in a given row initializes its input register until it has received a LOW on its $\overline{IES}$ input from a row master or a slave of higher priority.

Similarly, the $\overline{ORE}$ outputs of slaves do not go HIGH until their inputs have gone HIGH. This interlocking scheme ensures that new input data may be accepted by the array when the $\overline{IRF}$ output of the final slave in that row goes HIGH and that output data for the array may be extracted when the $\overline{ORE}$ output of the final slave in the output row goes HIGH.

The row master is established by connecting its $\overline{IES}$ input to ground, while a slave receives its $\overline{IES}$ input from the $\overline{IRF}$ output of the next-higher priority device. When an array of 'F433 FIFOs is initialized with a LOW on the MR inputs of all devices, the $\overline{IRF}$ outputs of all devices are HIGH. Thus, only the row master receives a LOW on the $\overline{IES}$ input during initialization.

Figure 10 is a conceptual logic diagram of the internal circuitry that determines master/slave operation. When $\overline{MR}$ and $\overline{IES}$ are LOW, the master latch is set. When $\overline{TTS}$ goes LOW, the initialization flip-flop is set. If the master latch if HIGH, the input register is immediately initialized and the initialization flip-flop reset. If the master latch is reset, the input register is not initialized until $\overline{IES}$ goes LOW. In array operation, activating $\overline{TTS}$ initiates a ripple input register initialization from the row master to the last slave.

A similar operation takes place for the output register. Either a $\overline{TOS}$ or TOP input initiates a load-from-stack operation and sets the $\overline{ORE}$ request flip-flop. If the master latch is set, the last output register flip-flop is set and the $\overline{ORE}$ line goes HIGH. If the master latch is reset, the $\overline{ORE}$ output is LOW until a Serial Output Enable ($\overline{OES}$) input is received.

Block Diagram

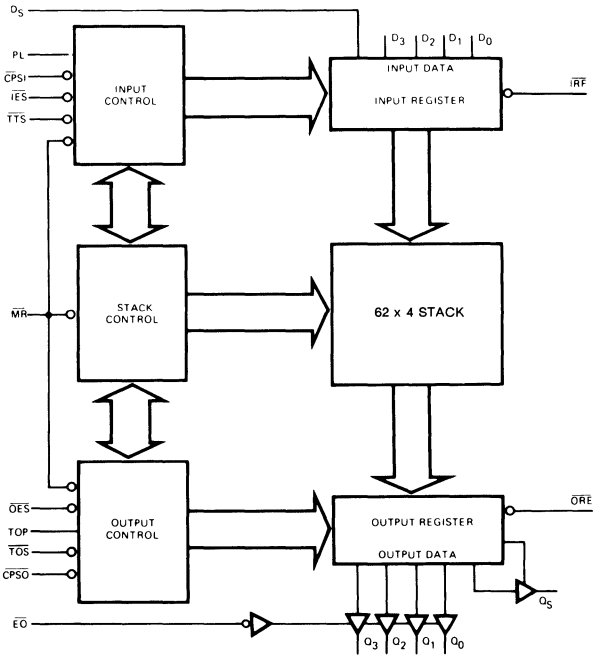


Fig. 1 Conceptual Input Section

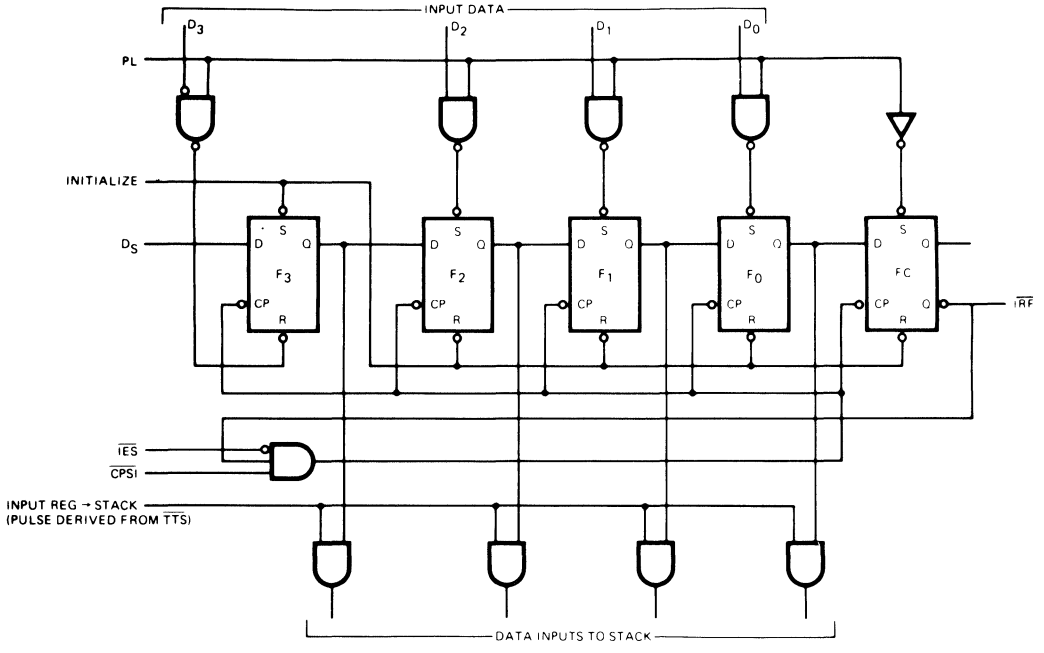


Fig. 2 Final Positions in an 'F433 Resulting from a 256-Bit Serial Train

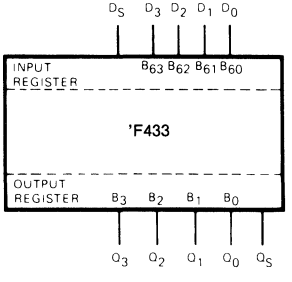


Fig. 3 Conceptual Output Section

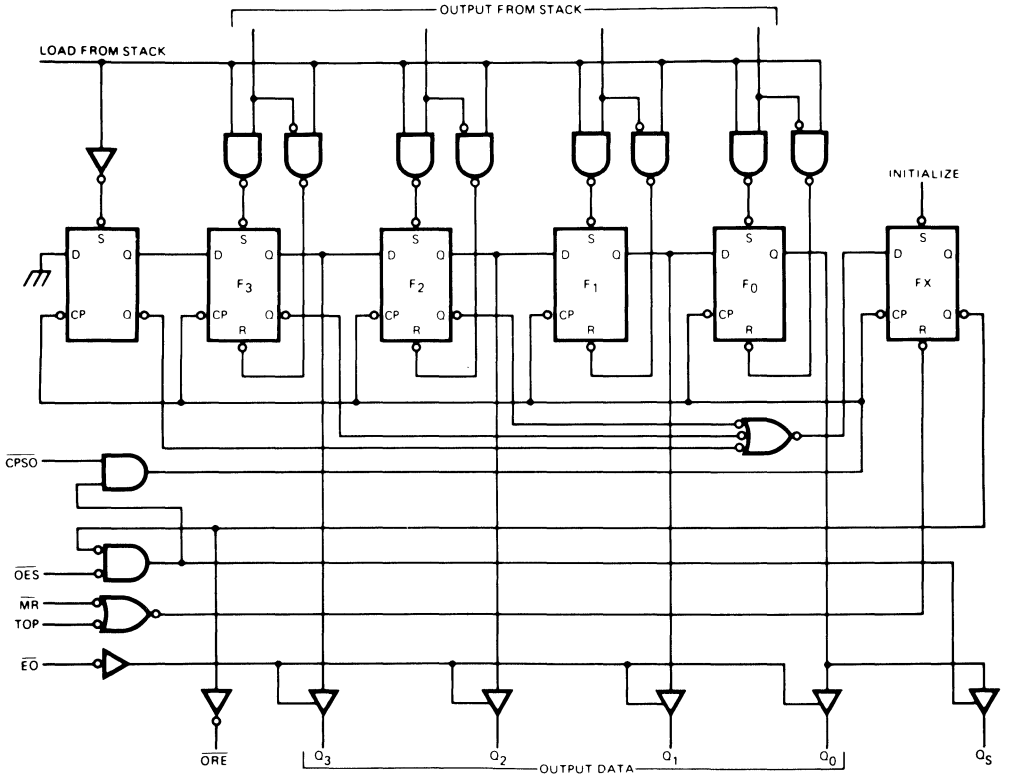


Fig. 4 A Vertical Expansion Scheme

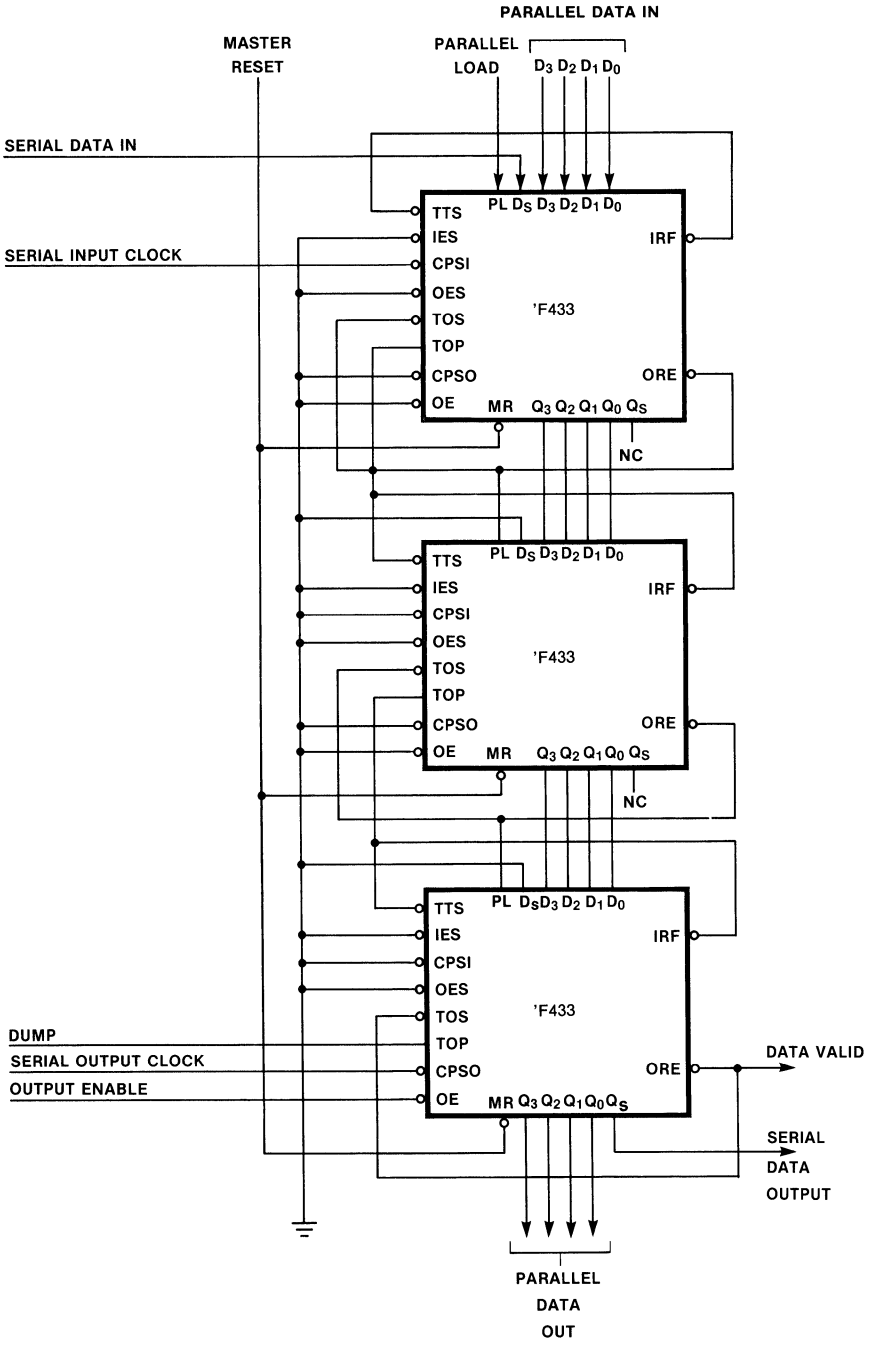


Fig. 5 A Horizontal Expansion Scheme

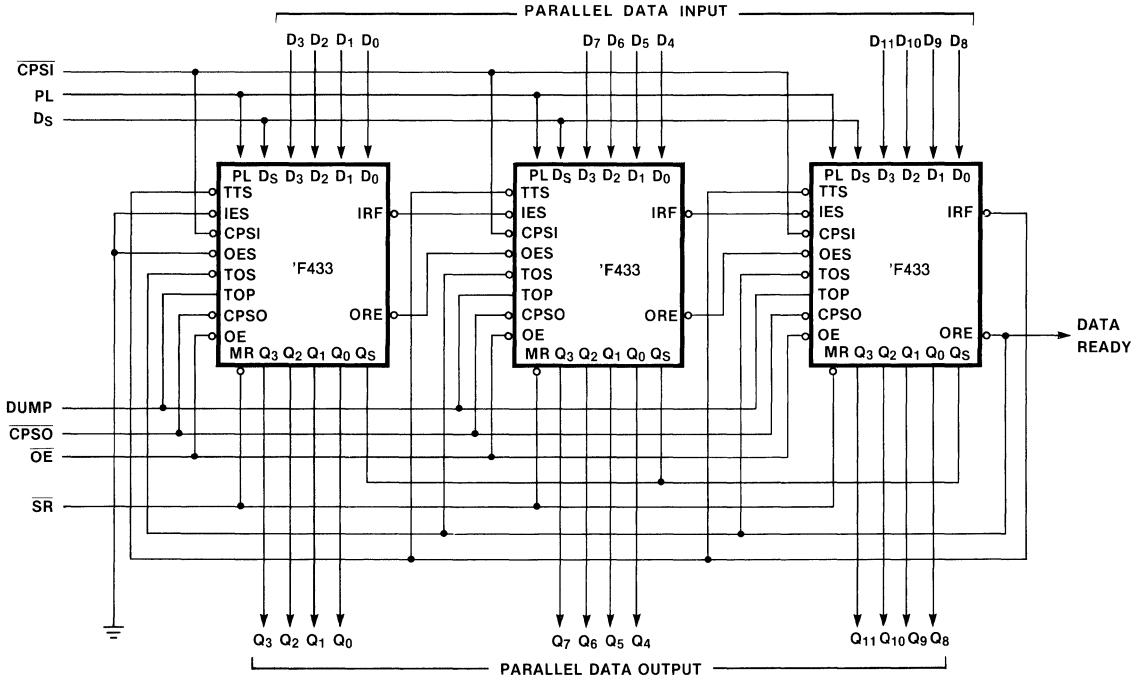


Fig. 6 A 127x16 FIFO Array

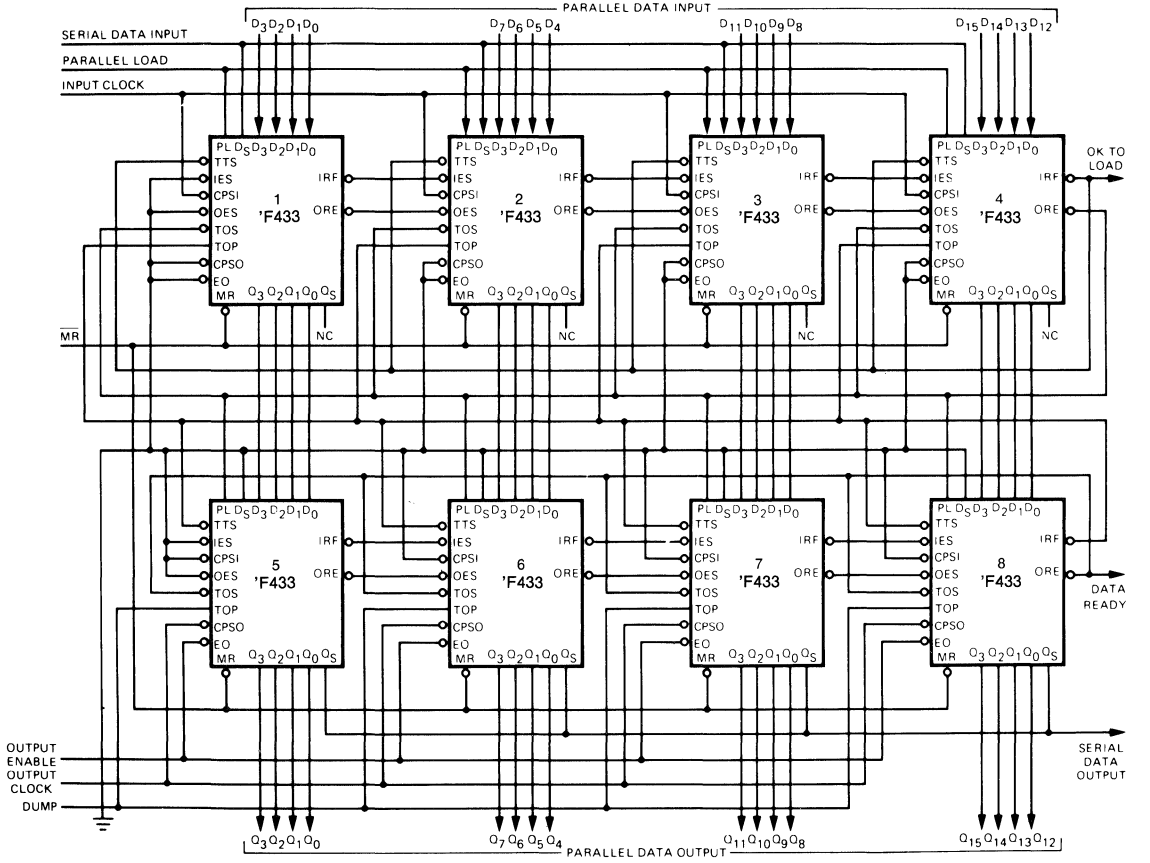


Fig. 7 Serial Data Entry for Array of Fig. 6

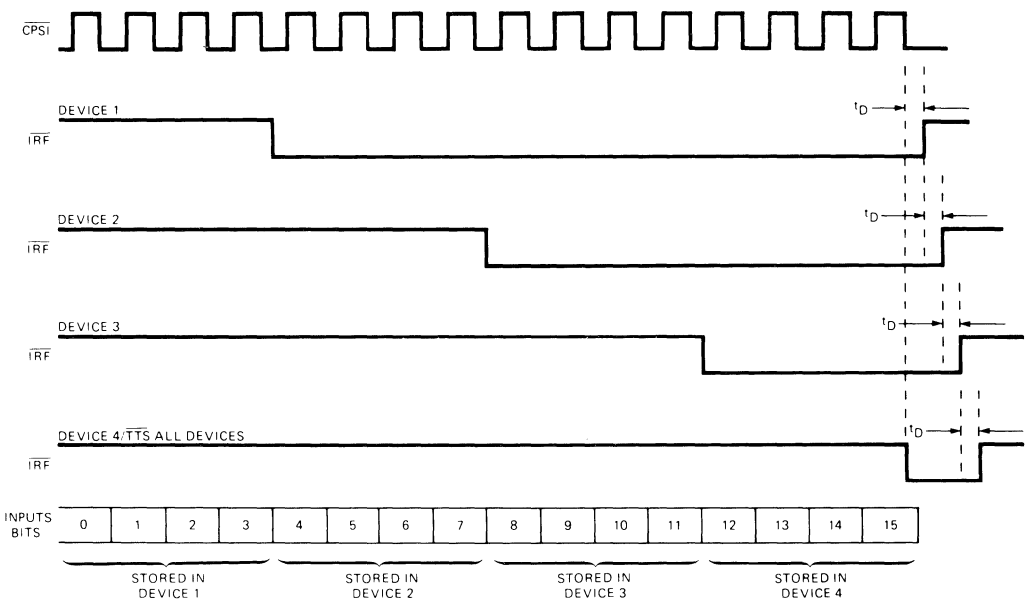


Fig. 8 Serial Data Extraction for Array of Fig. 6

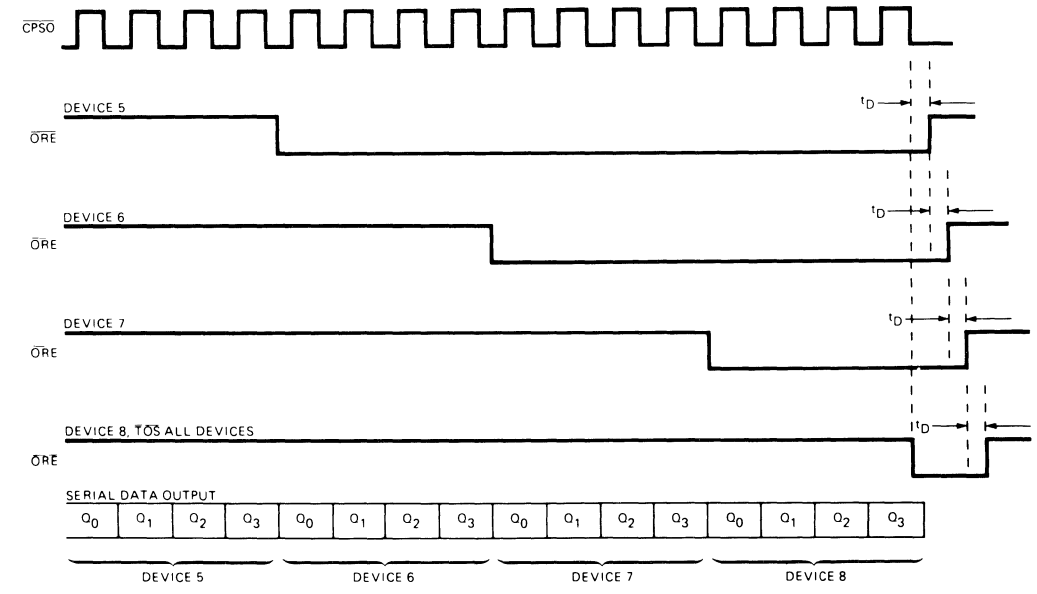


Fig. 9 Final Position of a 2032-Bit Serial Input

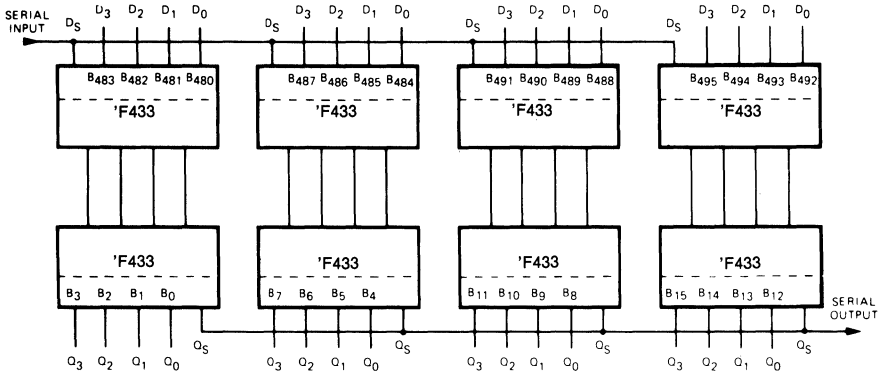
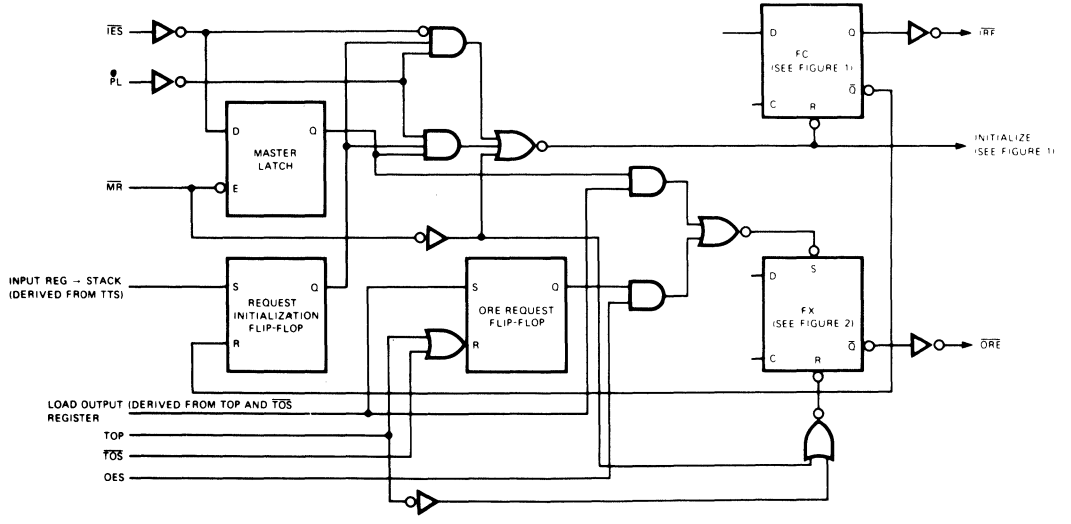


Fig. 10 Conceptual Diagram, Interlocking Circuitry



DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Supply Current		75	110	mA	V_{CC} = Max, Inputs Open

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$	T_A, V_{CC} = Mil $C_L = 50\ pF$	T_A, V_{CC} = Com $C_L = 50\ pF$		
		Min Typ Max	Min Max	Min Max		
t_{PHL}	Propagation Delay, Negative-Going CP to $\overline{IRF}$ Output	27.0			ns	3-1 403-a 403-b
t_{PLH}	Propagation Delay, Negative-Going $\overline{TTS}$ to $\overline{IRF}$	62.0				
t_{PLH} t_{PHL}	Propagation Delay, Negative-Going $\overline{CPSO}$ to Q_S Output	39.0 26.0			ns	3-1, 403-c 403-d
t_{PLH} t_{PHL}	Propagation Delay, Positive-Going TOP to Q_0-Q_3 Outputs	73.0 61.0			ns	3-1 403-e
t_{PHL}	Propagation Delay, Negative-Going $\overline{CPSO}$ to $\overline{ORE}$	27.0			ns	3-1, 403-c 403-d
t_{PHL}	Propagation Delay, Negative-Going TOP to $\overline{ORE}$	40.0			ns	3-1, 403-e
t_{PLH}	Propagation Delay, Positive-Going TOP to $\overline{ORE}$	70.0				
t_{PLH}	Propagation Delay, Negative-Going $\overline{TOS}$ to Positive-Going $\overline{ORE}$	70.0			ns	3-1 403-c 403-d
t_{PHL}	Propagation Delay, Positive-Going PL to Negative-Going $\overline{IRF}$	34.0			ns	3-1 403-g 403-h
t_{PLH}	Propagation Delay, Negative-Going PL to Positive-Going $\overline{IRF}$	38.0				
t_{PLH}	Propagation Delay, Positive-Going $\overline{OES}$ to $\overline{ORE}$	31.0			ns	3-1
t_{PLH}	Propagation Delay Positive-Going $\overline{IES}$ to Positive-Going $\overline{IRF}$	28.0			ns	3-1, 403-h

AC Characteristics (cont'd)

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$	T_A, V_{CC} = Mil $C_L = 50\ pF$	T_A, V_{CC} = Com $C_L = 50\ pF$		
		Min Typ Max	Min Max	Min Max		
t_{PZH} t_{PZL}	Enable Time $\overline{OE}$ to Q_0-Q_3	12.0 12.0			ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Disable Time $\overline{OE}$ to Q_0-Q_3	14.0 14.0				
t_{PZH} t_{PZL}	Enable Time Negative-Going $\overline{OES}$ to Q_s	12.0 12.0			ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Disable Time Negative-Going $\overline{OES}$ to Q_s	14.0 14.0				
t_{DFT}	Fall-Through Time	3.6			μs	3-1, 403-f
t_{AP}	Parallel Appearance Time $\overline{ORE}$ to Q_0-Q_3	12.0			ns	3-1
t_{AS}	Serial Appearance Time $\overline{ORE}$ to Q_s	14.0				

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW D_S to Negative $\overline{CPSI}$	6.0 6.0			ns	403-a 403-b
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D_S to $\overline{CPSI}$	3.0 3.0				
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{TTS}$ to $\overline{IRF}$ Serial or Parallel Mode	-22.0 -22.0			ns	403-a 403-b 403-g, 403-h
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW Negative-Going $\overline{ORE}$ to Negative-Going $\overline{TOS}$	0 0			ns	403-c 403-d
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW Negative-Going $\overline{IES}$ to $\overline{CPSI}$	17.0 17.0			ns	403-b
$t_s(H)$ $t_s(L)$	Set-Up Time, HIGH or LOW Negative-Going $\overline{TTS}$ to $\overline{CPSI}$	85.0 85.0			ns	403-b
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW Parallel Inputs to PL	-16.0 -16.0			ns	3-14
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW Parallel Inputs to PL	10.0 10.0				
$t_w(H)$ $t_w(L)$	CPSI Pulse Width HIGH or LOW	10.0 15.0			ns	403-a 403-b
$t_w(H)$	PL Pulse Width, HIGH	10.0			ns	403-g 403-h
$t_w(L)$	$\overline{TTS}$ Pulse Width, LOW Serial or Parallel Mode	23.0			ns	403-a 403-b 403-g 403-h
$t_w(L)$	$\overline{MR}$ Pulse Width, LOW	22.0			ns	403-f
$t_w(H)$ $t_w(L)$	TOP Pulse Width HIGH or LOW	40.0 24.0			ns	403-e
$t_w(H)$ $t_w(L)$	$\overline{CPSO}$ Pulse Width HIGH or LOW	10.0 16.0			ns	403-c 403-d
t_{rec}	Recovery Time $\overline{MR}$ to Any Input	23.0			ns	403-f

Fig. 433-a Serial Input, Unexpanded or Master Operation

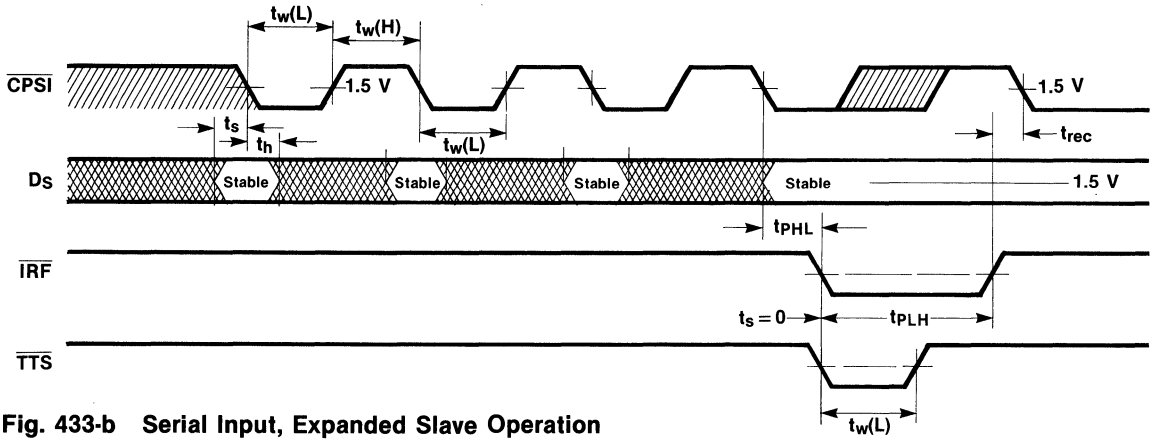


Fig. 433-b Serial Input, Expanded Slave Operation

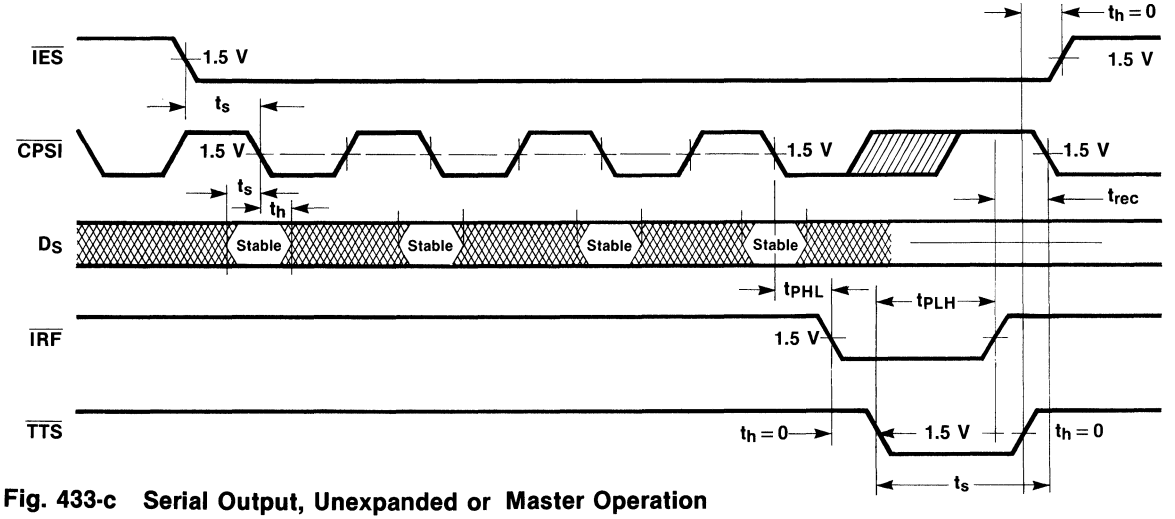


Fig. 433-c Serial Output, Unexpanded or Master Operation

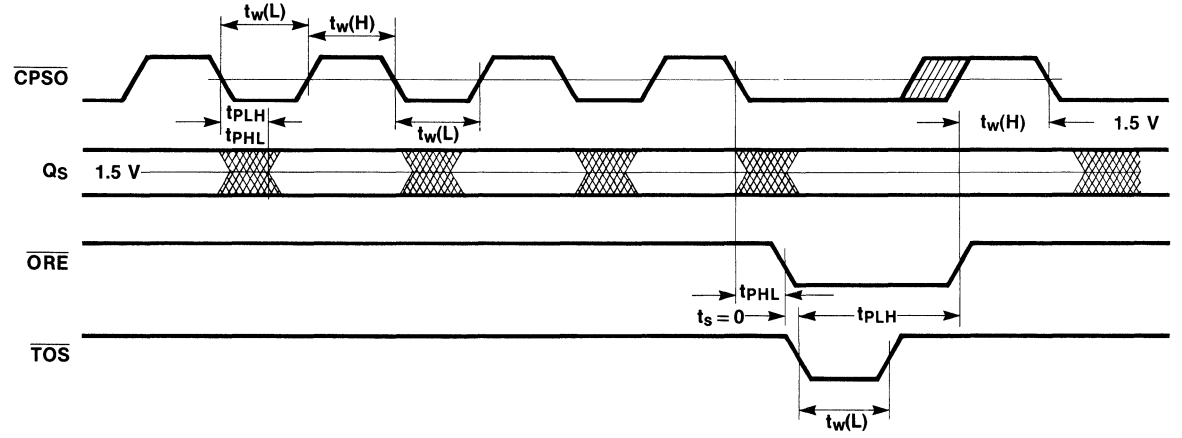


Fig. 433-d Serial Output, Slave Operation

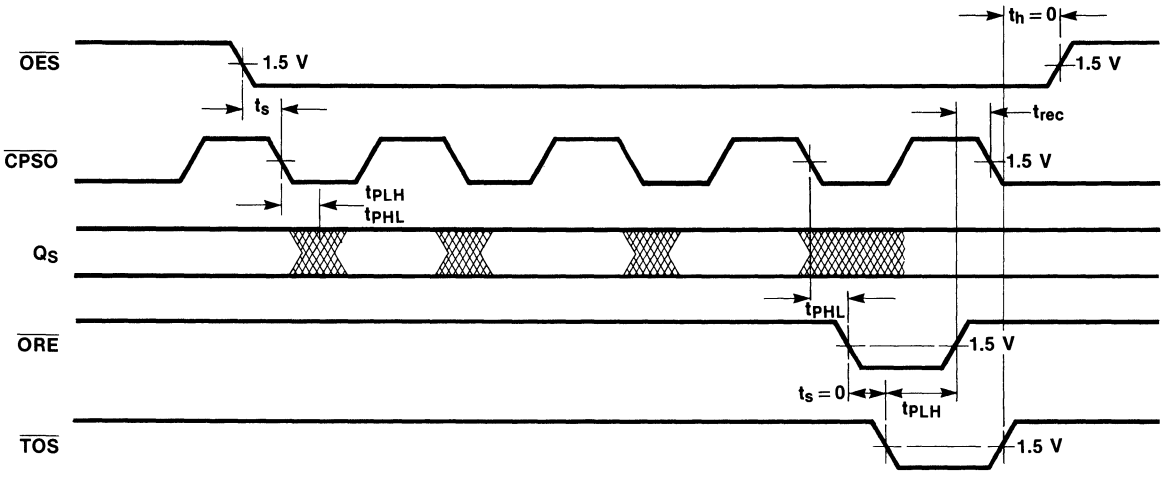


Fig. 433-e Parallel Output, 4-Bit Word or Master in Parallel Expansion

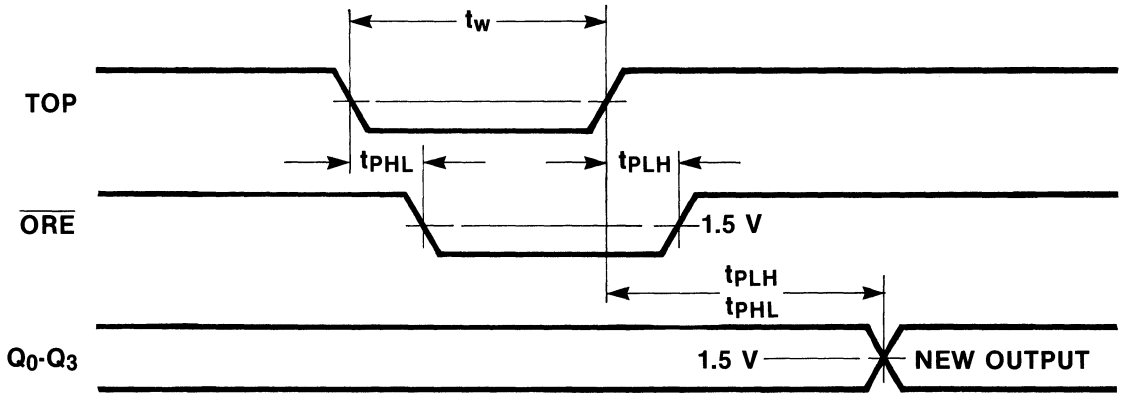


Fig. 433-f Fall Through Time

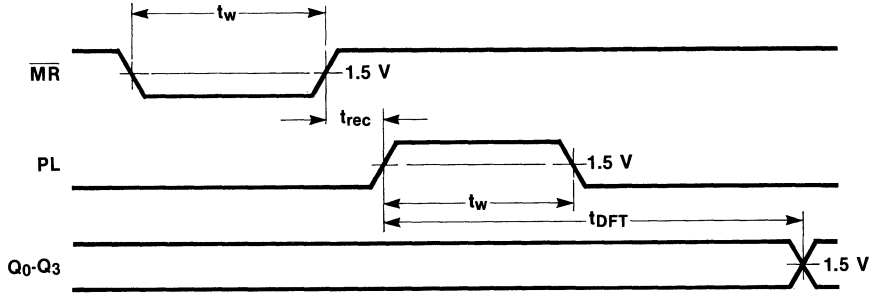


Fig. 433-g Parallel Load Mode, 4-Bit Word (Unexpanded) or Master in Parallel Expansion

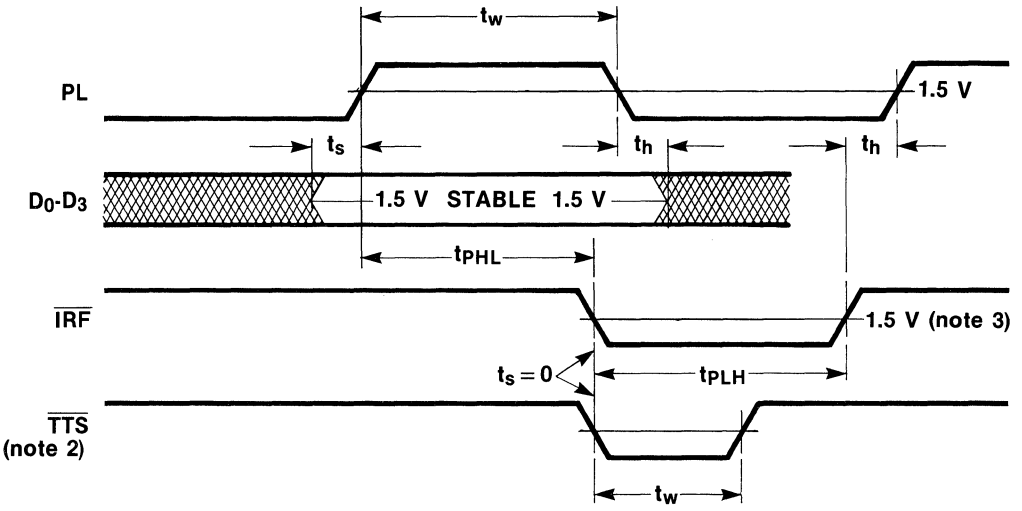
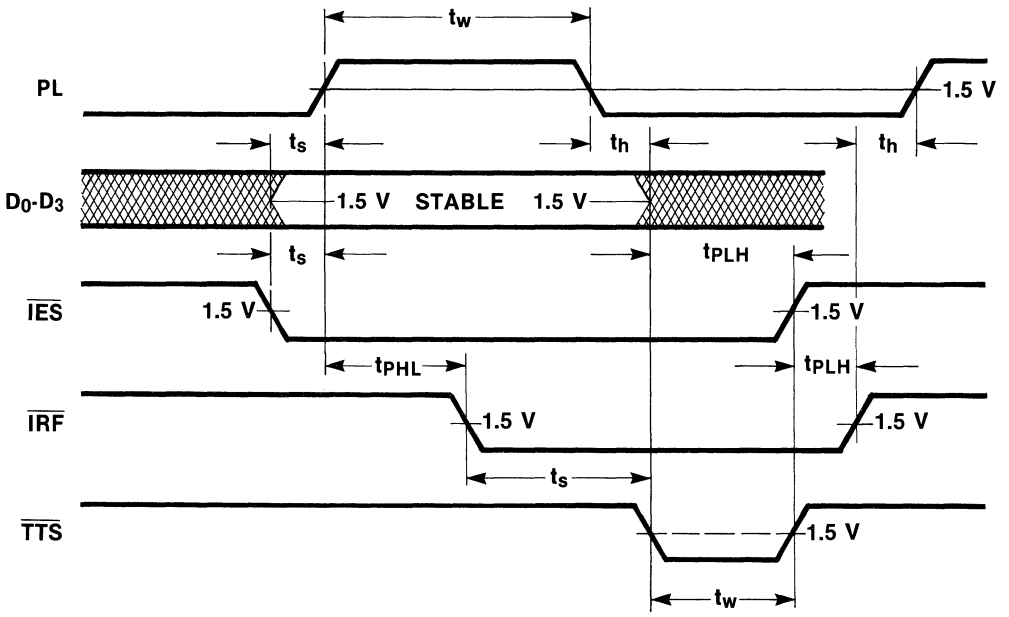


Fig. 433-h Parallel Load, Slave Mode



54F/74F500

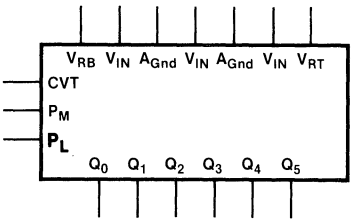
6-Bit Analog-to-Digital Flash Converter

Description

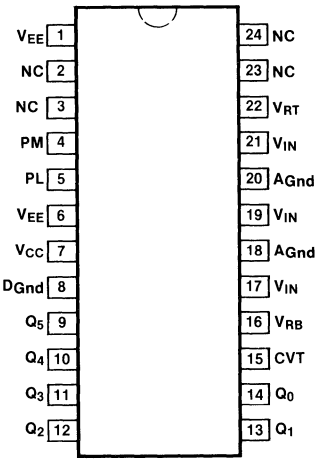
The 'F500 is a 6-bit, fully parallel analog-to-digital converter capable of sampling at rates from 0 to 50 MHz. Conversion is accomplished by 63 comparators spaced one quanta apart on a voltage reference ladder. All comparators measure the analog input against their reference simultaneously. The most significant comparator that finds the analog input to be greater than its reference has its output encoded to a 6-bit, active HIGH binary number, stored in latches. Two polarity control inputs are provided: P_M complements the most significant output bit and P_L complements the lesser five output bits. The circuit operates from +5.0 V and −6.0 V supplies and has separate digital and analog grounds. Both ends of the reference ladder are brought out, one to V_{RT} (nominally zero volts) and the other to V_{RB} (nominally −1.0 V).

Ordering Code: See Section 5

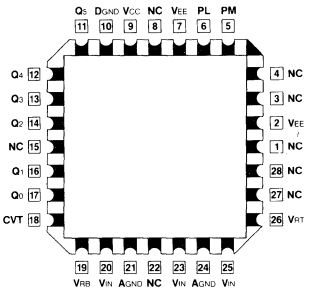
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC

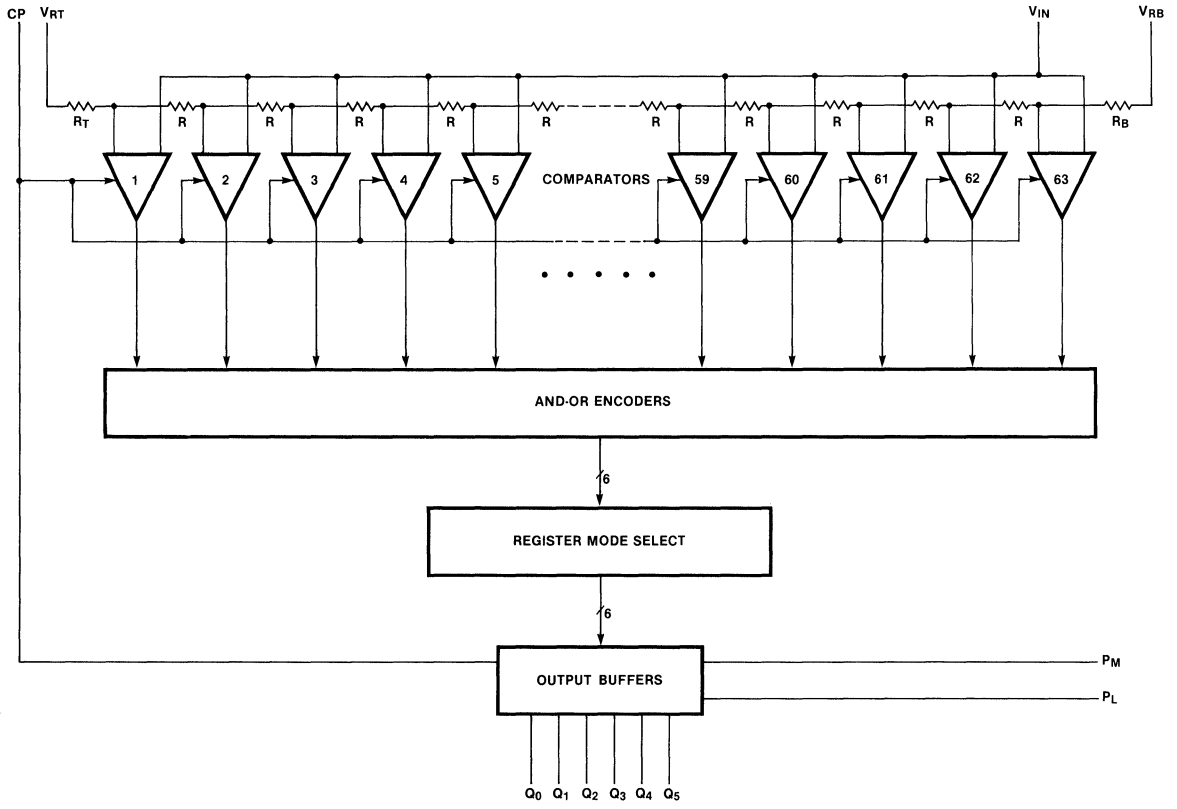


Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
AV_{EE}	Analog Supply Voltage	N/A
DV_{CC}	TTL Supply Voltage	N/A
D_{GND}	TTL Ground	N/A
A_{GND}	Analog Ground	N/A
Q_0-Q_5	Digital Output, Q_0 = MSB, Q_5 = LSB	25/12.5
P_M	Polarity Control MSB Output	0.5/0.375
P_L	Polarity Control LSB Outputs	0.5/0.375
V_{RT}	Reference Voltage (Top)	N/A
V_{RB}	Reference Voltage (Bottom)	N/A
V_{IN}	Analog Voltage Input	N/A
CNV	Convert	0.5/0.375

Block Diagram



Performance Characteristics over Recommended Operating Temperature Range

Parameter	54F/74F			Units
	Min	Typ	Max	
Resolution		6 1.6		Bits %
Input Range		1.0		V
Linearity Error		0.4		%
Offset Error, Top Bottom		+27 −27		mV
Aperture Jitter		30		psec
Bandwidth, Small Signal 3.0 dB 0.1 dB		 45 8		 MHz
Transient Response		20		ns
Signal-to-Noise Ratio Peak Signal/RMS Noise RMS Signal/RMS Noise		 43 42 34 33		 dB
Noise Power Ratio		25.5		dB

Interface Specifications over Recommended Operating Temperature Range

Power Supply

Symbol	Parameter	54F/74F $T_A = +25°C$ V_{CC} (TTL) = +5.0 V V_{EE} (Analog) = −5.0 V C_L = 50 pF			Units
		Min	Typ	Max	
I_{CC}	Supply Current		20	30	mA
I_{EE}	Supply Current		−105	−150	mA
V_{CC}	Supply Voltage	+4.50	+5.00	+5.50	V
V_{EE}	Supply Voltage	−5.75	−6.00	−6.25	V

Analog

Symbol	Parameter	54F/74F $T_A = +25°C$ V_{CC} (TTL) = +5.0 V V_{EE} (Analog) = −5.0 V C_L = 50 pF			Units
		Min	Typ	Max	
Signal Input:					
V_{IN}	Input Voltage				V
R_{IN}	Equivalent Input Impedance	15		∞	KΩ
C_{IN}	Input Capacitance			85	pF
I_{BIAS}	Constant Input Bus			110	μA
I_B	Clock Synchronous Bias			25	μA
Reference Input:					
I_{RT}	Reference Current, Top			8	mA
I_{RB}	Reference Current Bottom			−8	mA
R	Reference Resistor	1.9	2.0		Ω
V_{RT}	Reference Voltage	−1.1	0	+0.1	V
V_{RB}	Reference Voltage	−0.9	−1.0	−2.1	V
V_{RT}-V_{RB}	Input Voltage Range	0.8	1.0	1.2	V

AC Characteristics

Symbol	Parameter	54F/74F $T_A = +25°C$ V_{CC} (TTL) = +5.0 V V_{EE} (Analog) = −6.0 V C_L = 50 pF			54F $T_A = -55°C$ to $+125°C$ V_{CC} (TTL) = +5.0 V ± 10% V_{EE} (Analog) = −6.0 V + 0.25 V C_L = 50 pF		74F $T_A = 0°C$ to $+70°C$ V_{CC} (TTL) = +5.0 V ± 5% V_{EE} (Analog) = −6.0 V ± 0.25 V C_L = 50 pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency	25	40						MHz
t_{PLH} t_{PHL}	Propagation Delay Aperture Delay		18.0 18.0						ns
t_A	Aperture Delay		10.0						ns
$t_w(H)$ $t_w(L)$	Convert Pulse Width HIGH or LOW	12.0 12.0							ns

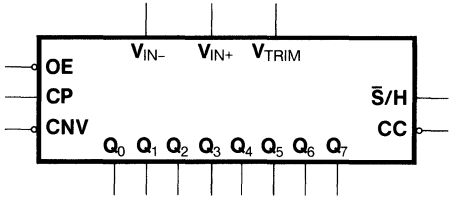
54F/74F505

8-Bit Successive Approximation Analog-to-Digital Converter

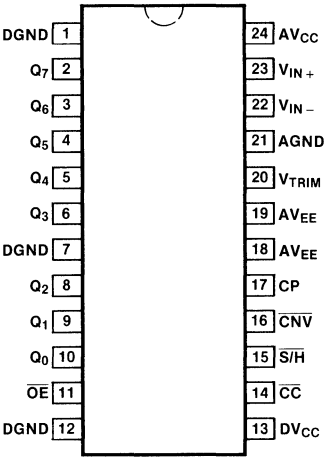
- **Microprocessor Compatible**
- **Conversion Time 100 ns Typ**
- **Power Dissipation 450 mW Typ**
- **+5 V and −5 V Power Supplies**
- **Input Range +1 V to −1 V**
- **Linearity ±0.5 LSB**
- **Output Code Offset Binary (+1 V = 11111111, −1 V = 00000000)**
- **On Chip Temperature Stable Reference Voltage**
- **User Gain Trim**
- **3-State Latched Outputs**

Ordering Code: See Section 5

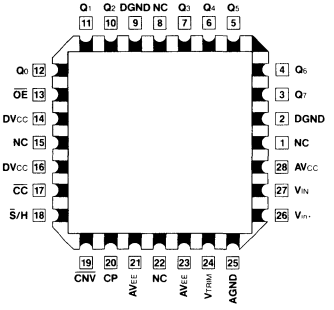
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC

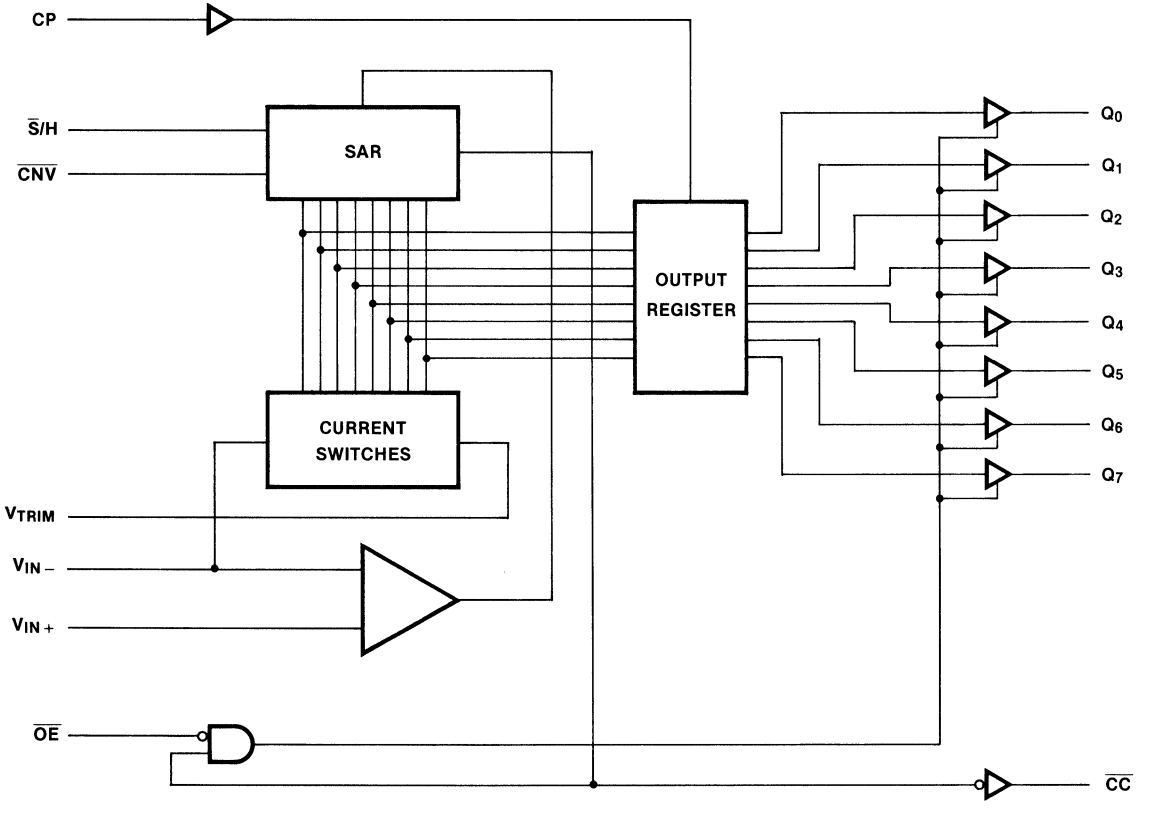


Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
AV_{CC}	Analog +5 V Supply Voltage	N/A
A_{GND}	Analog 0 V	N/A
AV_{EE}	Analog −5 V Supply Voltage	N/A
DV_{CC}	Digital +5 V Supply Voltage	N/A
D_{GND}	Digital 0 V	N/A
$V_{IN}+$	Analog Input +	N/A
$V_{IN}-$	Analog Input −	N/A
V_{TRIM}	Gain Trim	N/A
$\overline{S/H}$	Sample/Hold	0.5/0.375
$\overline{CNV}$	Convert	0.5/0.375
$\overline{CC}$	Conversion Complete	25/12.5
$\overline{OE}$	Output Enable	0.5/0.375
Q_0-Q_7	Data Out	75/15 (12.5)
CP	Clock	0.5/0.375

Block Diagram



Functional Description

The 'F505 is a high-speed, 8-bit successive approximation analog to digital converter. It is intended for use up to video frequencies, and where the speed of flash converters is not required. It features a unique handshaking control system which allows a simple microprocessor interface and simple cascading for interleaved operation.

Performance Characteristics over Recommended Operating Temperature Range

Parameter	54F/74F			Units
	Min	Typ	Max	
Conversion Time		100		ns
Resolution	8			Bits
Input Range	−1.0		+1.0	V
Linearity	−0.5		+0.5	LSB
Differential Linearity			0.2	%
Gain Temperature Coefficient			20	ppm/°C
Common Mode Offset	−1.0		+1.0	V

Interface Specifications Over Recommended Operating Temperature Range

Power Supply

Symbol	Parameter	54F/74F $T_A = +25°C$, V_{CC} (TTL) = +5.0 V, V_{CC} (Analog) = +5.0 V, V_{EE} (Analog) = -5.0 V, C_L = 50 pF			Units
		Min	Typ	Max	
I_{CCD}	Supply Current TTL V_{CC} to TTL Gnd			50	mA
I_{CCA}	Supply Current Analog V_{CC} to Analog Gnd			28	mA
I_{EE}	Supply Current Analog Gnd to Analog V_{EE}			41	mA

Interface Specifications Over Recommended Operating Temperature Range (cont'd)

Analog

Symbol	Parameter	54F/74F $T_A = +25°C$ V_{CC} (TTL) = +5.0 V V_{CC} (Analog) = +5.0 V V_{EE} (Analog) = -5.0 V C_L = 50 pF			Units
		Min	Typ	Max	
Signal Input:					
V_{IN}	Input Voltage	−1.0		+1.0	V
R_{IN}	Input Resistance		20		KΩ
C_{IN}	Input Capacitance			10	pF
I_{BIAS}	Input Bias Current (V_{IN} + = Max)			430	μA
Trim Input:					
V_{TRIM}	Trim Input Range	−0.825		+0.825	V
V_{TRIM} (center) Trim Range	Trim Input Center Voltage Trim Range		3.89 2.00		V %fsd
R_{TRIM}	Input Resistance	5.8			KΩ

AC Characteristics

Symbol	Parameter	54F/74F $T_A = +25°C$ V_{CC} (TTL) = +5.0 V V_{CC} (Analog) = +5.0 V V_{EE} (Analog) = −5.0 V C_L = 50 pF			54F $T_A = -55°C$ to $+125°C$ V_{CC} (TTL) = +5.0 V ± 10% V_{CC} (Analog) = +5.0 V + 10% V_{EE} (Analog) = −5.0 V ± 10% C_L = 50 pF		74F $T_A = 0°C$ to $+70°C$ V_{CC} (TTL) = +5.0 V ± 5% V_{CC} (Analog) = +5.0 V ± 5% V_{EE} (Analog) = −5.0 V ± 5% C_L = 50 pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency		80						MHz
t_{PLH} t_{PHL}	Propagation Delay Digital Output		8.0 8.0						ns

AC Operating Requirements

Symbol	Parameter	54F/74F			54F		74F		Units
		$T_A = +25°C$ V_{CC} (TTL) = +5.0 V V_{CC} (Analog) = +5.0 V V_{EE} (Analog) = −5.0 V C_L = 50 pF			$T_A = -55°C$ to $+125°C$ V_{CC} (TTL) = +5.0 V ± 10% V_{CC} (Analog) = +5.0 V + 10% V_{EE} (Analog) = −5.0 V ± 10% C_L = 50 pF		$T_A = 0°C$ to $+70°C$ V_{CC} (TTL) = +5.0 V ± 5% V_{CC} (Analog) = +5.0 V ± 5% V_{EE} (Analog) = −5.0 V ± 5% C_L = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW CNV to CP		2.0 2.0						ns
$t_h(H)$ $t_h(H)$	Hold Time HIGH or LOW CNV to CP		2.0 2.0						ns
$t_w(H)$ $t_w(L)$	Clock Pulse Width HIGH or LOW		4.4 4.4						ns

4

Fig. 505-a Timing Waveforms

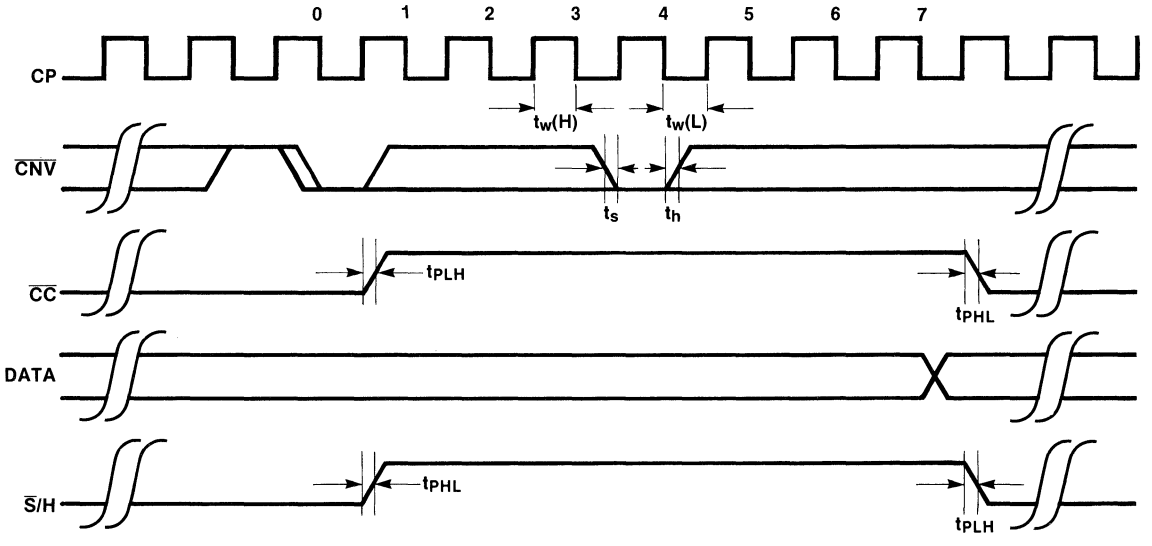
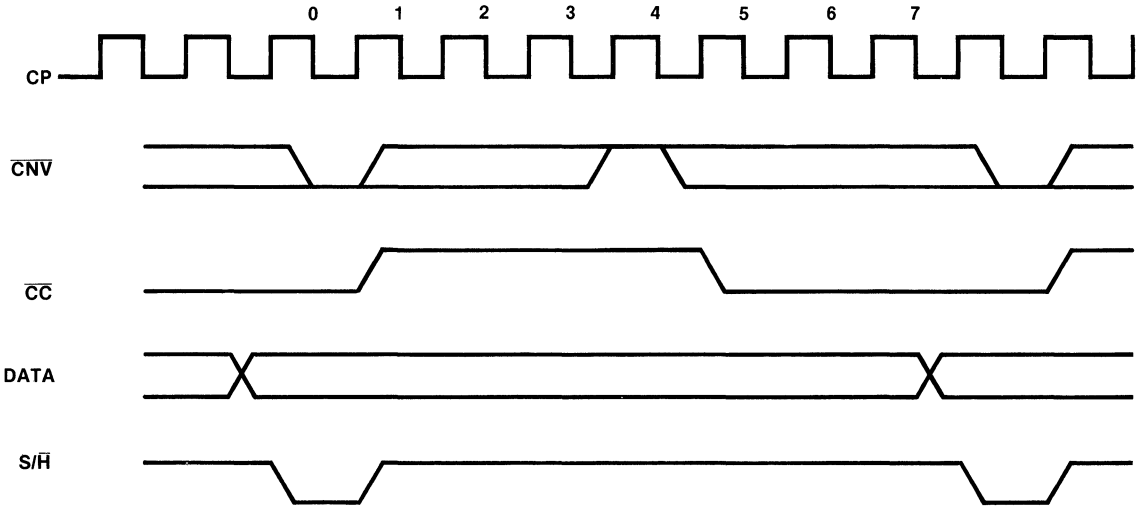


Fig. 505-b Timing Waveforms



54F/74F521

8-Bit Identity Comparator

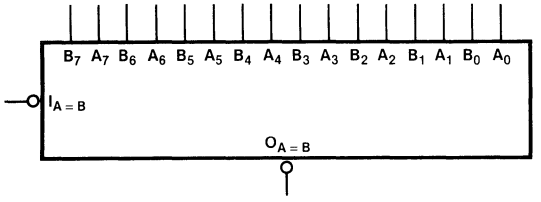
Description

The 'F521 is an expandable 8-bit comparator. It compares two words of up to eight bits each and provides a LOW output when the two words match bit for bit. The expansion input $\overline{I}_{A=B}$ also serves as an active LOW enable input.

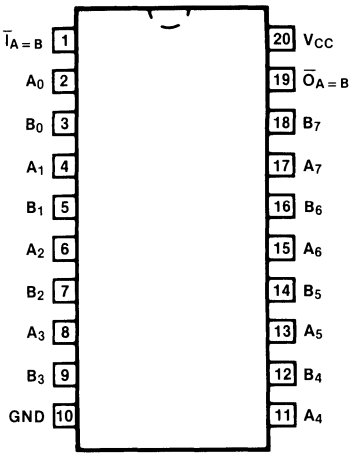
- **Compares Two 8-Bit Words in 6.5 ns Typ**
- **Expandable to Any Word Length**
- **20-Pin Package**

Ordering Code: See Section 5

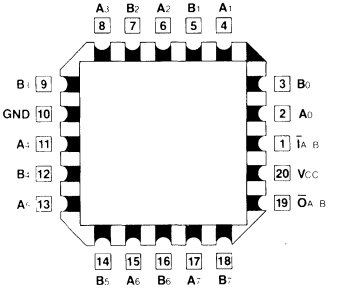
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

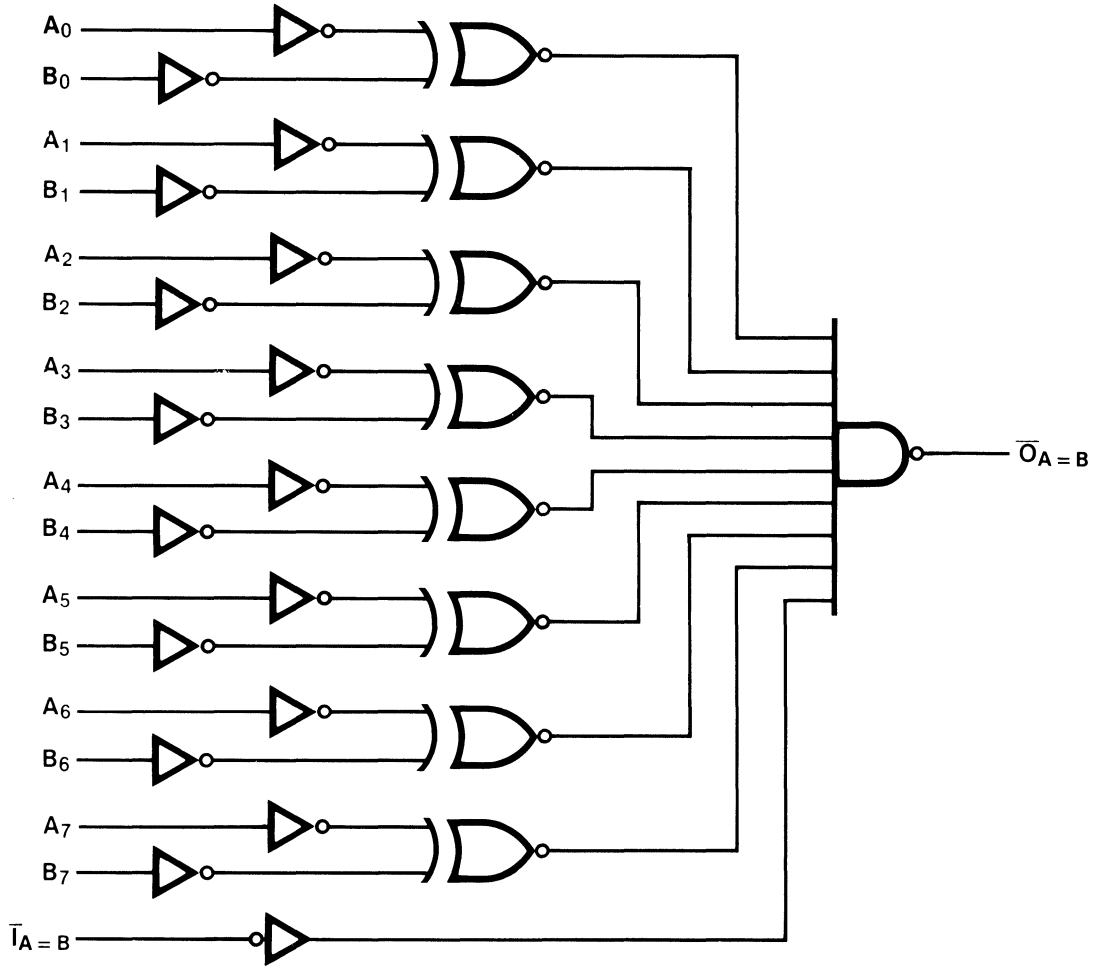
Pin Names	Description	54F/74F(U.L.) HIGH/LOW
A_0-A_7	Word A Inputs	0.5/0.375
B_0-B_7	Word B Inputs	0.5/0.375
$\overline{I}_{A=B}$	Expansion or Enable Input (Active LOW)	0.5/0.375
$\overline{O}_{A=B}$	Identity Output (Active LOW)	25/12.5

Truth Table

Inputs		Output
$\overline{I}_{A=B}$	A, B	$\overline{O}_{A=B}$
L	A = B*	L
L	A ≠ B	H
H	A = B*	H
H	A ≠ B	H

H = HIGH Voltage Level
L = LOW Voltage Level
*$A_0 = B_0$, $A_1 = B_1$, $A_2 = B_2$, etc.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

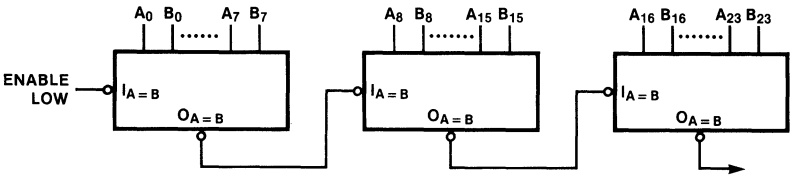
Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		21	32	mA	V_{CC} = Max All inputs HIGH

AC Characteristics: See Section 3 for waveforms and load configurations

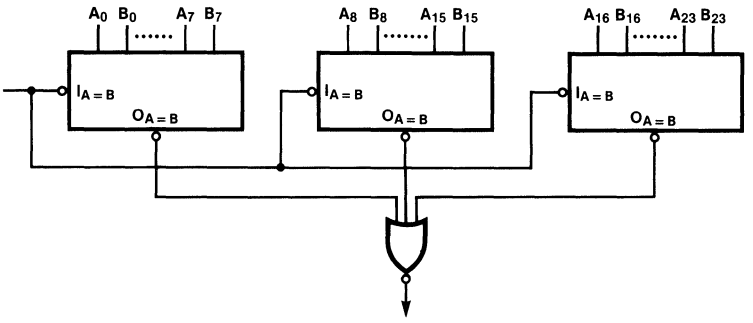
Symbol	Parameter	54F/74F T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			54F T_A, V_{CC} = Mil C_L = 50 pF		74F T_A, V_{CC} = Com C_L = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n or B_n to $\overline{O}_{A=B}$	3.5 4.5	7.0 7.0	10.0 10.0	3.5 4.0	15.0 12.0	3.5 4.0	11.0 11.0	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay $\overline{I}_{A=B}$ to $\overline{O}_{A=B}$	3.0 3.5	5.0 6.5	6.5 9.0	3.0 3.5	8.5 9.0	3.0 3.5	7.5 10.0	ns	3-1 3-10

Applications

Ripple Expansion



Parallel Expansion



54F/74F524

8-Bit Registered Comparator

Description

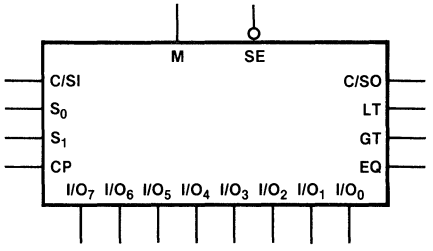
The 'F524 is an 8-bit bidirectional register with parallel input and output plus serial input and output progressing from LSB to MSB. All data inputs, serial and parallel, are loaded by the rising edge of the input clock. The device functions are controlled by two control lines (S_0, S_1) to execute shift, load, hold and read out.

An 8-bit comparator examines the data stored in the registers and on the data bus. Three true-HIGH, open-collector outputs representing 'register equal to bus', 'register greater than bus' and 'register less than bus' are provided. These outputs can be disabled to the OFF state by the use of Status Enable ($\overline{SE}$). A mode control has also been provided to allow twos complement as well as magnitude compare. Linking inputs are provided for expansion to longer words.

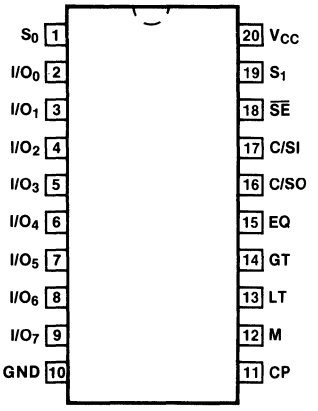
- **8-Bit Bidirectional Register with Bus-Oriented Input-Output**
- **Independent Serial Input-Output to Register**
- **Register Bus Comparator with 'Equal to', 'Greater then' and 'Less than' Outputs**
- **Cascadable in Groups of Eight Bits**
- **Open-Collector Comparator Outputs for AND-Wired Expansion**
- **Twos Complement or Magnitude Compare**

Ordering Code: See Section 5

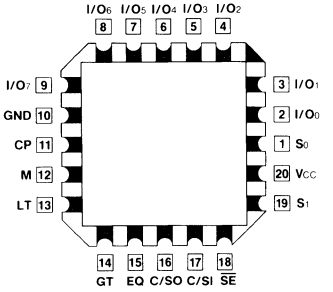
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
S_0, S_1	Mode Select Inputs	0.5/0.375
C/SI	Status Priority or Serial Data Input	0.5/0.375
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
$\overline{SE}$	Status Enable Input (Active LOW)	0.5/0.375
M	Compare Mode Select Input	0.5/0.375
I/O_0-I/O_7	Parallel Data Inputs or	1.75/0.406
	3-State Parallel Data Outputs	75/15 (12.5)
C/SO	Status Priority or Serial Data Output	25/12.5
LT	Register Less Than Bus Output	OC*/12.5
EQ	Register Equal Bus Output	OC*/12.5
GT	Register Greater Than Bus Output	OC*/12.5

*OC = Open Collector

Functional Description

The 'F524 contains eight D-type flip-flops connected as a shift register with provision for either parallel or serial loading. Parallel data may be read from or loaded into the registers via the data bus I/O_0-I/O_7. Serial data is entered from the C/SI input and may be shifted into the register and out through the C/SO output. Both parallel and serial data entry occur on the rising edge of the input clock (CP). The operation of the shift register is controlled by two signals S_0 and S_1 according to the Select Truth Table. The 3-state parallel output buffers are enabled only in the Read mode.

One port of an 8-bit comparator is attached to the data bus while the other port is tied to the outputs of the internal register. Three active-OFF, open-collector outputs indicate whether the contents held in the shift register are 'greater than', (GT), 'less than' (LT), or 'equal to' (EQ) the data on the input bus. A HIGH signal on the Status Enable ($\overline{SE}$) input disables these outputs to the OFF state. A mode control input (M) allows selection between a straightforward magnitude compare or a comparison between twos complement numbers.

For 'greater than' or 'less than' detection, the C/SI input must be held HIGH, as indicated in the Status Truth Table. The internal logic is arranged such that a LOW signal on the C/SI input disables the 'greater than' and 'less than' outputs. The C/SO output will be forced HIGH if the 'equal to' status condition exists, otherwise C/SO will be held LOW. These facilities enable the 'F524 to be cascaded for word length greater than eight bits.

Word length expansion (in groups of eight bits) can be achieved by connecting the C/SO output of the more significant byte to the C/SI input of the next less significant byte and also to its own $\overline{SE}$ input (see Figure a). The C/SI input of the most significant device is held HIGH while the $\overline{SE}$ input of the least significant device is held LOW. The corresponding status outputs are AND-wired together. In the case of twos complement number compare, only the Mode input to the most significant device should be HIGH. The Mode inputs to all other cascaded devices are held LOW.

Suppose that an inequality condition is detected in the most significant device. Assuming that the byte stored in the register is greater than the byte on the data bus, the EQ and LT outputs will be pulled LOW and the GT output will float HIGH. Also the C/SO output of the most significant device will be forced LOW, disabling the subsequent devices but enabling its own status outputs. The correct status condition is thus indicated. The same applies if the registered byte is less than the data byte, only in this case the EQ and GT outputs go LOW and LT output floats HIGH.

If an equality condition is detected in the most significant device, its C/SO output is forced HIGH. This enables the next less significant device and also disables its own status outputs. In this way, the status output priority is handed down to the next less significant device which now effectively becomes the most significant byte. The worst case

propagation delay for a compare operation involving 'n' cascaded 'F524s will be when an equality condition is detected in all but the least significant byte. In this case, the status priority has to ripple all the way down the chain before the correct status output is established. Typically, this will take 35 + 6(n-2) ns.

Select Truth Table

S_0	S_1	Operation
L	L	Hold—Retains data in shift register
L	H	Read—Read contents in register onto data bus
H	L	Shift—Allows serial shifting on next rising clock edge
H	H	Load—Load data on bus into register

Number Representation Select Table

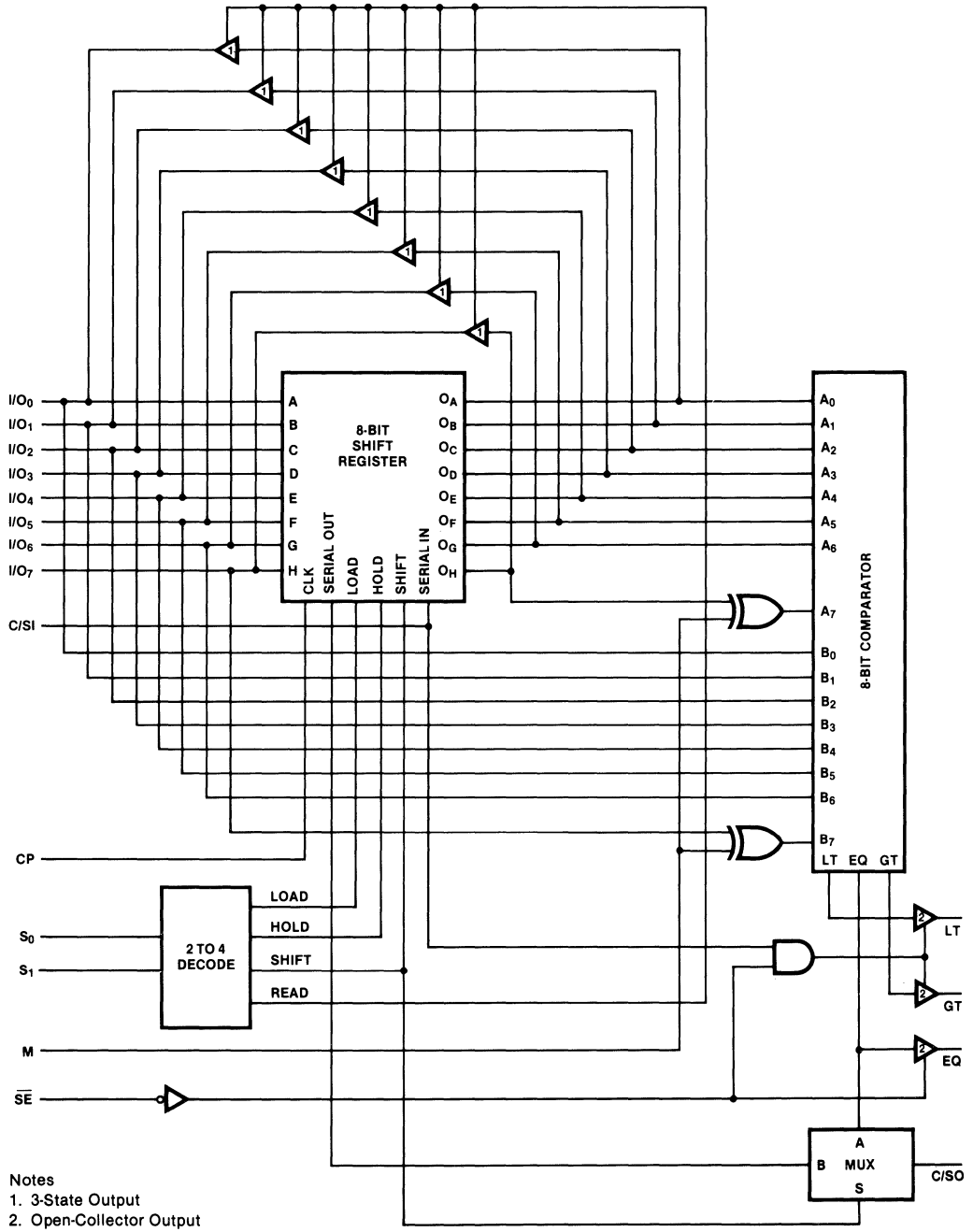
M	Operation
L	Magnitude compare
H	Twos complement compare

Status Truth Table (Hold Mode)

Inputs			Outputs			
$\overline{SE}$	C/SI	Data Comparison	EQ	GT	LT	C/SO
H	X	X	H	H	H	1
L	L	O_A-O_H > I/O_0-I/O_7	L	H	H	L
L	L	O_A-O_H = I/O_0-I/O_7	H	H	H	L
L	L	O_A-O_H < I/O_0-I/O_7	L	H	H	L
L	H	O_A-O_H > I/O_0-I/O_7	L	H	L	L
L	H	O_A-O_H = I/O_0-I/O_7	H	L	L	H
L	H	O_A-O_H < I/O_0-I/O_7	L	L	H	L

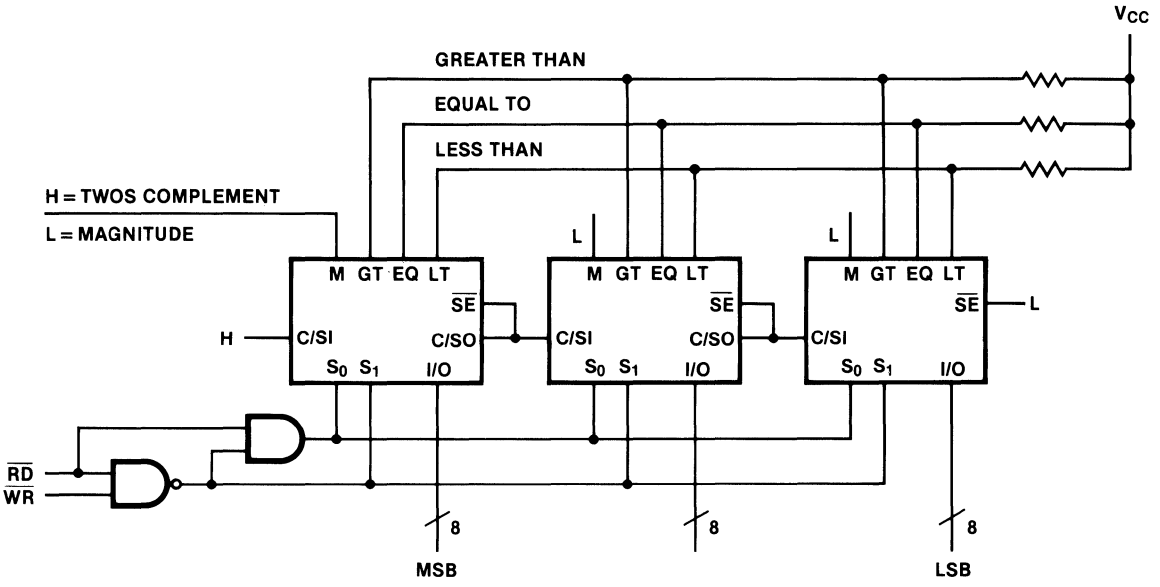
1 = HIGH if data are equal, otherwise LOW
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Block Diagram



Notes
1. 3-State Output
2. Open-Collector Output

Fig. a Cascading 'F524s for Comparing Longer Words



DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		128	180	mA	S_0, S_1, $\overline{SE}$, C/SI = HIGH CP, I/O_0-I/O_7, Register = LOW

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F $T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$			54F T_A, V_{CC} = Mil $C_L = 50\ pF$		74F T_A, V_{CC} = Com $C_L = 50\ pF$		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Shift Frequency	50	75				50		MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay I/O_n to EQ	9.0 5.0	16.5 9.5	20.0 12.0			9.0 5.0	21.0 13.0	ns	3-1, 3-10
t_{PLH} t_{PHL}	Propagation Delay I/O_n to GT	8.5 6.5	14.1 13.0	19.0 16.5			8.5 6.5	20.0 17.5		
t_{PLH} t_{PHL}	Propagation Delay I/O_n to LT	7.0 4.5	15.5 10.0	20.0 14.0			7.0 4.5	21.0 15.0		
t_{PLH} t_{PHL}	Propagation Delay I/O_n to C/SO	8.0 6.0	15.2 12.5	19.5 16.0			8.0 6.0	20.5 17.0	ns	3-1, 3-10
t_{PLH} t_{PHL}	Propagation Delay CP to EQ	10.0 4.0	20.0 8.5	25.0 16.5			10.0 4.0	26.0 17.5	ns	3-1, 3-7
t_{PLH} t_{PHL}	Propagation Delay CP to GT	10.0 8.5	16.5 17.0	21.0 22.0			10.0 8.5	22.0 23.0		
t_{PLH} t_{PHL}	Propagation Delay CP to LT	9.0 5.5	20.0 13.5	25.0 17.0			9.0 5.5	26.0 18.0		
t_{PLH}	Propagation Delay CP to C/SO (Compare)	8.5	16.5	21.0			8.5	22.0	ns	3-1, 3-7
t_{PLH} t_{PHL}	Propagation Delay CP to C/SO (Serial Shift)	5.0 4.5	10.0 9.0	13.0 11.5			5.0 4.5	14.0 12.5		
t_{PLH} t_{PHL}	Propagation Delay C/SI to GT	9.0 3.0	15.0 6.5	19.0 8.5			9.0 3.0	20.0 9.5	ns	3-1, 3-3
t_{PLH} t_{PHL}	Propagation Delay C/SI to LT	8.0 3.5	15.5 6.5	20.0 8.5			8.0 3.5	21.0 9.5		

AC Characteristics (Cont'd)

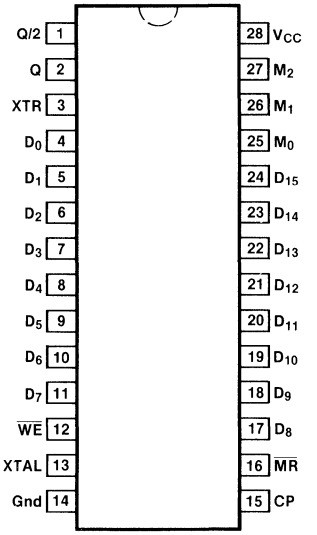
Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$			T_A, V_{CC} = Mil $C_L = 50\ pF$		T_A, V_{CC} = Com $C_L = 50\ pF$			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay S_0, S_1 to EQ	15.0 9.0	25.0 15.0	33.0 19.0			15.0 9.0	35.0 20.0	ns	3-1, 3-10
t_{PLH} t_{PHL}	Propagation Delay S_0, S_1 to GT	10.5 10.5	18.0 18.0	23.0 23.0			10.5 10.5	24.0 24.0		
t_{PLH} t_{PHL}	Propagation Delay S_0, S_1 to LT	13.0 12.0	22.0 19.0	28.0 24.0			13.0 12.0	30.0 25.0		
t_{PLH} t_{PHL}	Propagation Delay S_0, S_1 to C/SO	6.5 5.5	11.5 14.0	14.5 18.0			6.5 5.5	15.5 19.0	ns	3-1, 3-10
t_{PLH} t_{PHL}	Propagation Delay $\overline{SE}$ to EQ	3.5 2.5	8.0 6.0	10.5 8.0			3.5 2.5	11.5 9.0	ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay $\overline{SE}$ to GT	6.5 3.5	12.5 6.5	16.0 8.0			6.5 3.5	17.0 9.0		
t_{PLH} t_{PHL}	Propagation Delay $\overline{SE}$ to LT	5.0 3.5	10.5 6.0	13.5 8.0			5.0 3.5	14.5 9.0		
t_{PLH} t_{PHL}	Propagation Delay C/SI to C/SO	4.0 4.0	8.5 8.5	11.0 11.0			4.0 4.0	12.0 12.0	ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay M to GT	8.0 6.0	15.0 12.0	19.5 15.5			8.0 6.0	20.5 16.5	ns	3-1, 3-10
t_{PLH} t_{PHL}	Propagation Delay M to LT	8.0 5.5	17.0 9.5	22.0 12.0			8.0 4.5	23.0 13.0		
t_{PZH} t_{PZL}	Output Enable Time S_0, S_1 to I/O_n	4.5 5.5	10.0 11.0	13.0 15.0			4.5 5.5	14.0 16.0	ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time S_0, S_1 to I/O_n	3.5 4.5	8.0 9.6	12.0 12.5			3.5 4.5	13.0 13.5		

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW I/O_n to CP	6.0 6.0		6.0 6.0	ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW I/O_n to CP	0 0		0 0		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW S_0 or S_1 to CP	10.0 10.0		10.0 10.0	ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW S_0 or S_1 to CP	0 0		0 0		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW C/SI to CP	7.0 7.0		7.0 7.0	ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW C/SI to CP	0 0		0 0		
$t_w(H)$	Clock Pulse Width, HIGH	5.0		5.0	ns	3-7

54F/74F525

Programmable Counter



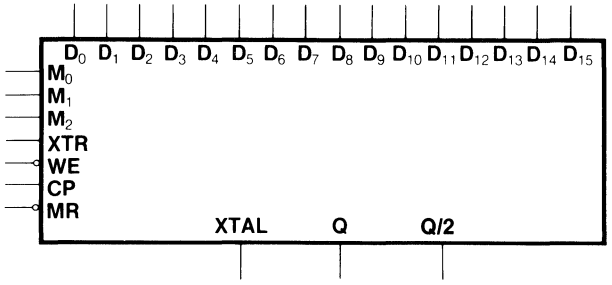
Description

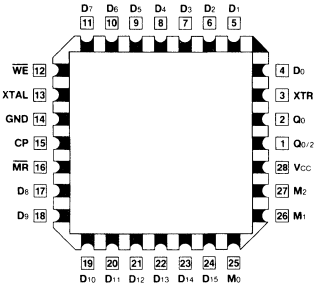
The 'F525 is a multi-function 28-pin device. It consists of a 16-bit count-down counter, logic to control the counter, logic to control the state of the outputs and a PLA to decode the particular function selected by the user. The list of high-speed timing applications include:

- Baud Rate Generator
- Digitally Programmed Monostable
- Variable System Frequency Generator
- Digital Filter Variable Sampling Rate

Ordering Code: See Section 5

Logic Symbol





Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
Q	Output (Primarily indicates when the counter has reached zero)	25/12.5
Q/2	Output (Divides Q by 2)	25/12.5
M_0-M_2	Status Inputs	0.5/0.375
$\overline{MR}$	Master Reset	0.5/0.375
CP	Clock Pulse	0.5/0.375
D_0-D_{15}	Data Inputs	0.5/0.375
$\overline{WE}$	Write Enable	0.5/0.375
XTR	External Trigger	0.5/0.375
XTAL	Crystal	0.5/0.375

Functional Description

The multi-function aspect of the device consists of eight different modes of operation. An explanation of the operation of the device in each of the modes follows. However, there is one operation that is independent of the selected mode, the loading of data. Data is latched into a set of data latches when $\overline{WE}$ is brought from a LOW to a HIGH state. The latches are transparent when $\overline{WE}$ is held LOW.

MODE 0
While XTR is HIGH, the data in the data latches is loaded into the counter upon the next positive-edge of CP. The negative-edge of XTR enables the count-down to begin with the next positive-edge of CP. When the count reaches zero, Q is brought HIGH and Q/2 toggles state. Taking XTR HIGH at any time causes the data in the latches to be loaded into the counter and the Q output to be cleared.

MODE 1
The operation is exactly the same as in mode 0 except that Q is normally HIGH and goes LOW on a count of zero. Q/2 toggles on the negative-edge of Q.

MODE 2
While XTR is HIGH, the data in the data latches is loaded into the counter upon the next positive-edge of CP. The negative-edge of XTR enables the count-down to begin with the next positive-edge of CP. When the count reaches zero, Q is brought HIGH for a single period of CP. Q/2 toggles state on the positive-edge of Q. Taking XTR HIGH at any time causes the data in the latches to be loaded into the counter and the Q output to be cleared.

MODE 3
The operation is exactly the same as in mode 2 except that Q is normally HIGH and goes LOW on a count of zero for a single period of CP. Q/2 toggles on the negative-edge of Q.

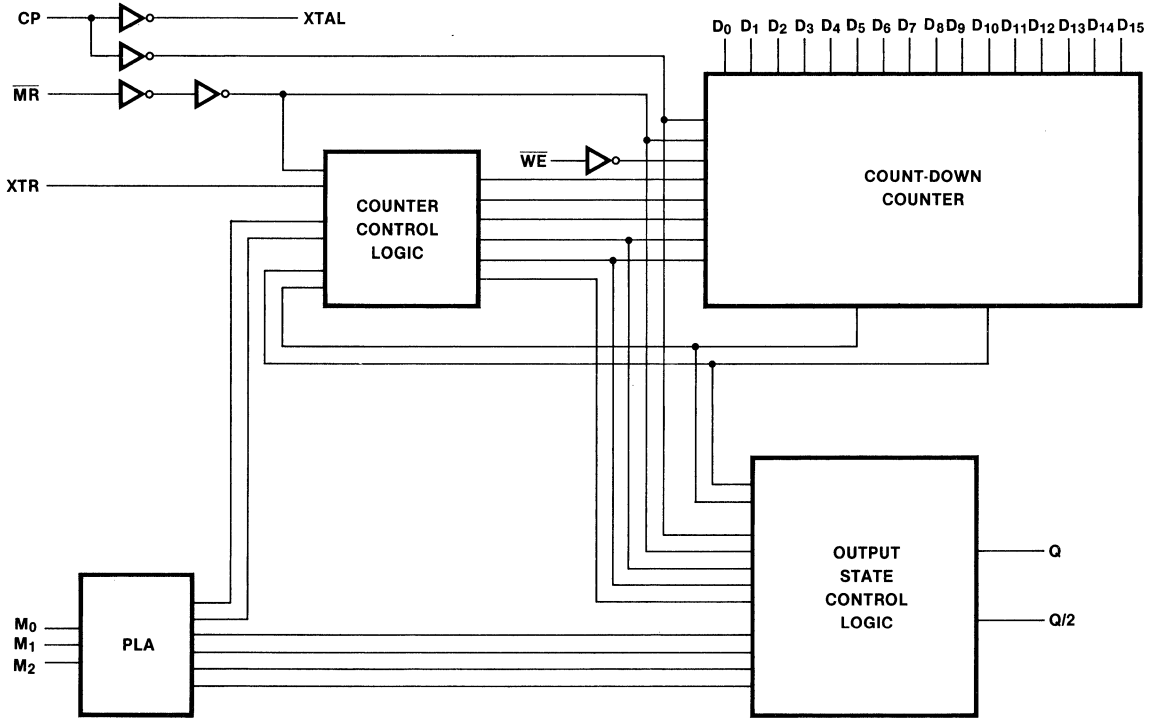
MODE 4
While XTR is HIGH, the data in the data latches is loaded into the counter upon the next positive-edge of CP. The negative-edge of XTR enables the count-down to begin with the next positive-edge of CP. When the count reaches zero, Q is brought HIGH for a single period of CP. Q/2 toggles state on the positive-edge of Q. Taking XTR HIGH before the counters reach zero causes the data currently in the counters to be held.

MODE 5
The operation is exactly the same as in Mode 4 except that Q is normally HIGH and goes LOW on a count of zero. Q/2 toggles on the negative-edge of Q.

MODE 6
While XTR is HIGH, the data in the data latches is loaded into the counter upon the next positive-edge of CP. The negative-edge of XTR enables both the count-down to begin and Q to go HIGH with the next positive-edge of CP. Q is brought LOW when the count reaches zero. Q/2 toggles on the positive-edge of CP. Bringing XTR HIGH during a count-down will reload the latched data into the counter, but will not affect Q.

MODE 7
The negative-edge of XTR enables the count-down to begin with the next positive-edge of CP. When the count reaches zero, Q is brought HIGH for a single period of CP. Q/2 toggles state on the positive-edge of Q. The positive-edge of CP upon which Q goes low also causes the data in the data latches to be reloaded into the counters. Taking XTR HIGH at any time causes the data in the data latches to be loaded into the counter and the Q output to be cleared. However, after an initial XTR this mode can run continuously until stopped by MR.

Block Diagram



DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		90	135	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F $T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$			54F T_A, V_{CC} = Mil $C_L = 50\ pF$		74F T_A, V_{CC} = Com $C_L = 50\ pF$		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	50	60						MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay CP to Q	9.0 8.0	16.0 12.0	20.5 15.5			8.0 7.0	22.5 17.5	ns	3-1 3-7
t_{PLH} t_{PHL}	Propagation Delay CP to Q/2	9.0 10.0	15.5 15.5	20.0 20.0			8.0 9.0	22.0 22.0	ns	3-1 3-7
t_{PLH} t_{PHL}	Propagation Delay XTR to Q	8.5 6.0	12.0 10.5	15.5 13.5			7.5 5.0	17.5 15.0	ns	3-1 3-7
t_{PLH} t_{PHL}	Propagation Delay $\overline{MR}$ to Q	11.5 9.0	16.5 12.5	21.0 16.0			10.0 8.0	23.0 18.0	ns	3-1 3-11
t_{PLH} t_{PHL}	Propagation Delay $\overline{MR}$ to Q/2	8.0 7.0	14.0 10.5	17.5 13.5			7.0 6.0	19.5 15.0	ns	3-1 3-11
t_{PLH} t_{PHL}	Propagation Delay M_n to Q	10.0 10.5	15.0 17.0	19.0 21.5			9.0 9.0	21.0 23.5	ns	3-1 3-10

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW D_n to $\overline{WE}$	2.0 4.0		2.5 4.5	ns	3-15
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D_n to $\overline{WE}$	0 2.0		0 2.5	ns	3-15
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW D_n to CP	9.0 10.5		10.0 12.0	ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D_n to CP	0 0		0 0	ns	3-5
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW XTR to CP	7.0 8.0		8.0 9.0	ns	3-5
$t_h(H)$	Hold Time, HIGH, XTR to CP	0		0	ns	3-5
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW Mode to CP	33.5 33.5		35.5 35.5	ns	3-5
$t_w(H)$	XTR Pulse Width, HIGH	11.5		13.0	ns	3-7
$t_w(L)$	MR Pulse Width, LOW	7.0		8.0	ns	3-11
$t_w(L)$	$\overline{WE}$ Pulse Width, LOW	4.5		5.0	ns	3-11
$t_w(H)$ $t_w(L)$	CP Pulse Width HIGH or LOW	3.5 9.5		4.0 10.5	ns	3-8
t_{rec}	Recovery Time $\overline{MR}$ to CP	5.0		6.0	ns	3-11
t_{rec}	Recovery Time Mode to CP	30.0		32.0	ns	3-11

54F/74F533

Octal Transparent Latch With 3-State Outputs

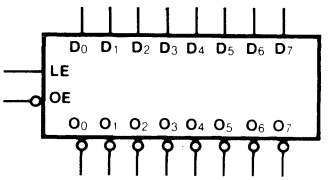
Description

The 'F533 consists of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH the bus output is in the high impedance state. The 'F533 is the same as the 'F373, except that the outputs are inverted. For description and logic diagram please see the 'F373 data sheet.

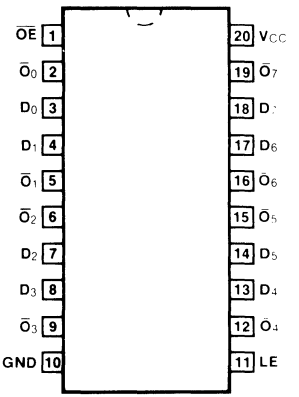
- **Eight Latches in a Single Package**
- **3-State Outputs for Bus Interfacing**

Ordering Code: See Section 5

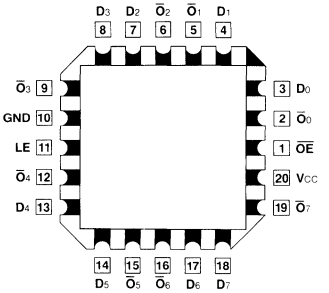
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
D_0-D_7	Data Inputs	0.5/0.375
LE	Latch Enable Input (Active HIGH)	0.5/0.375
$\overline{OE}$	Output Enable Input (Active LOW)	0.5/0.375
$\overline{O}_0$-$\overline{O}_7$	Complementary 3-State Outputs	75/15 (12.5)

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CCZ}	Power Supply Current		41	61	mA	V_{CC} = Max, $\overline{OE}$ = HIGH D_n, LE = Gnd

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			54F T_A, V_{CC} = Mil C_L = 50 pF		74F T_A, V_{CC} = Com C_L = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to $\overline{O}_n$	4.0 3.0	6.9 5.2	9.0 7.0	4.0 3.0	12.0 9.0	4.0 3.0	10.0 8.0	ns	3-1 3-3
t_{PLH} t_{PHL}	Propagation Delay LE to $\overline{O}_n$	5.0 3.0	8.5 5.6	11.0 7.0	5.0 3.0	14.0 9.0	5.0 3.0	13.0 8.0	ns	3-1 3-7
t_{PZH} t_{PZL}	Output Enable Time	2.0 2.0	7.7 5.1	10.0 6.5	2.0 2.0	12.5 9.0	2.0 2.0	11.0 7.5	ns	3-1, 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time	2.0 2.0	4.7 4.1	6.0 5.5	2.0 2.0	8.5 7.5	2.0 2.0	7.0 6.5	ns	3-1, 3-12 3-13

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F T_A = +25°C V_{CC} = +5.0 V			54F T_A, V_{CC} = Mil		74F T_A, V_{CC} = Com		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_s(H) t_s(L)	Setup Time, HIGH or LOW D_n to LE	2.0 2.0			2.0 2.0		2.0 2.0		ns	3-15
t_h(H) t_h(L)	Hold Time, HIGH or LOW D_n to LE	3.0 3.0			3.0 3.0		3.0 3.0		ns	3-15
t_w(H)	LE Pulse Width, HIGH	6.0			6.0		6.0		ns	3-7

54F/74F534

Octal D-Type Flip-Flop With 3-State Outputs

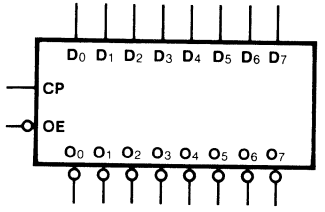
Description

The 'F534 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops. The 'F534 is the same as the 'F374 except that the outputs are inverted.

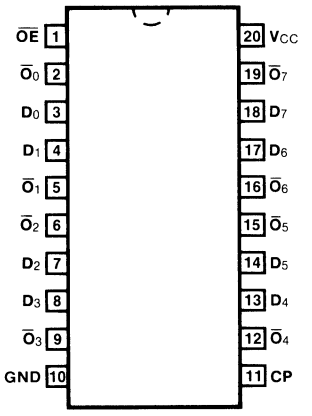
- **Edge-Triggered D-Type Inputs**
- **Buffered Positive Edge-Triggered Clock**
- **3-State Outputs for Bus-Oriented Applications**

Ordering Code: See Section 5

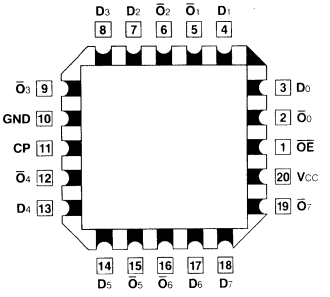
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

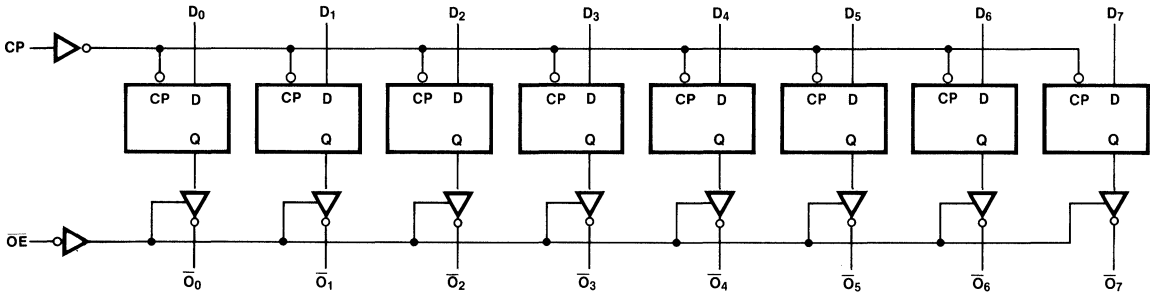
Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
D_0-D_7	Data Inputs	0.5/0.375
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
$\overline{OE}$	3-State Output Enable Input (Active LOW)	0.5/0.375
$\overline{O}_0$-$\overline{O}_7$	Complementary 3-State Outputs	75/15(12.5)

Functional Description

The 'F534 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-state true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CCZ}	Power Supply Current (All Outputs OFF)		55	86	mA	V_{CC} = Max, D_n = Gnd $\overline{OE}$ = HIGH

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F $T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$			54F T_A, V_{CC} = Mil $C_L = 50\ pF$		74F T_A, V_{CC} = Com $C_L = 50\ pF$		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	100			60		70		MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{O}_n$	4.0 4.0	6.5 6.5	8.5 8.5	4.0 4.0	10.5 11.0	4.0 4.0	10.0 10.0	ns	3-1 3-7
t_{PZH} t_{PZL}	Output Enable Time	2.0 2.0	9.0 5.8	11.5 7.5	2.0 2.0	14.0 10.0	2.0 2.0	12.5 8.5	ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time	2.0 2.0	5.3 4.3	7.0 5.5	2.0 2.0	8.0 7.5	2.0 2.0	8.0 6.5		

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F $T_A = +25°C$ $V_{CC} = +5.0\ V$			54F T_A, V_{CC} = Mil		74F T_A, V_{CC} = Com		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW D_n to CP	2.0 2.0			2.5 2.0		2.0 2.0		ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D_n to CP	2.0 2.0			2.0 2.5		2.0 2.0			
$t_w(H)$ $t_w(L)$	CP Pulse Width HIGH or LOW	7.0 6.0			7.0 6.0		7.0 6.0		ns	3-7

54F/74F537

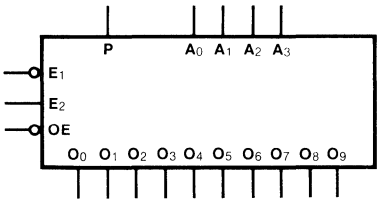
1-of-10 Decoder
With 3-State Outputs

Description

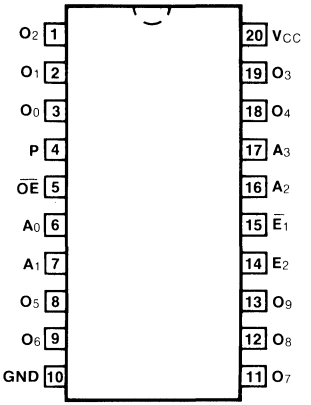
The 'F537 is one-of-ten decoder/demultiplexer with four active HIGH BCD inputs and ten mutually exclusive outputs. A polarity control input determines whether the outputs are active LOW or active HIGH. The 'F537 has 3-state outputs, and a HIGH signal on the Output Enable ($\overline{OE}$) input forces all outputs to the high impedance state. Two input enables, active HIGH E_2 and active LOW $\overline{E}_1$, are available for demultiplexing data to the selected output in either non-inverted or inverted form. Input codes greater than BCD nine cause all outputs to go to the inactive state (i.e., same polarity as the P input).

Ordering Code: See Section 5

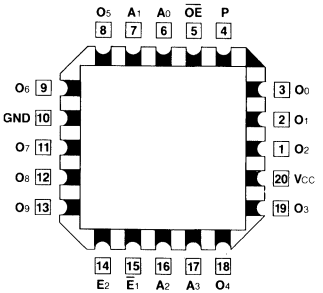
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

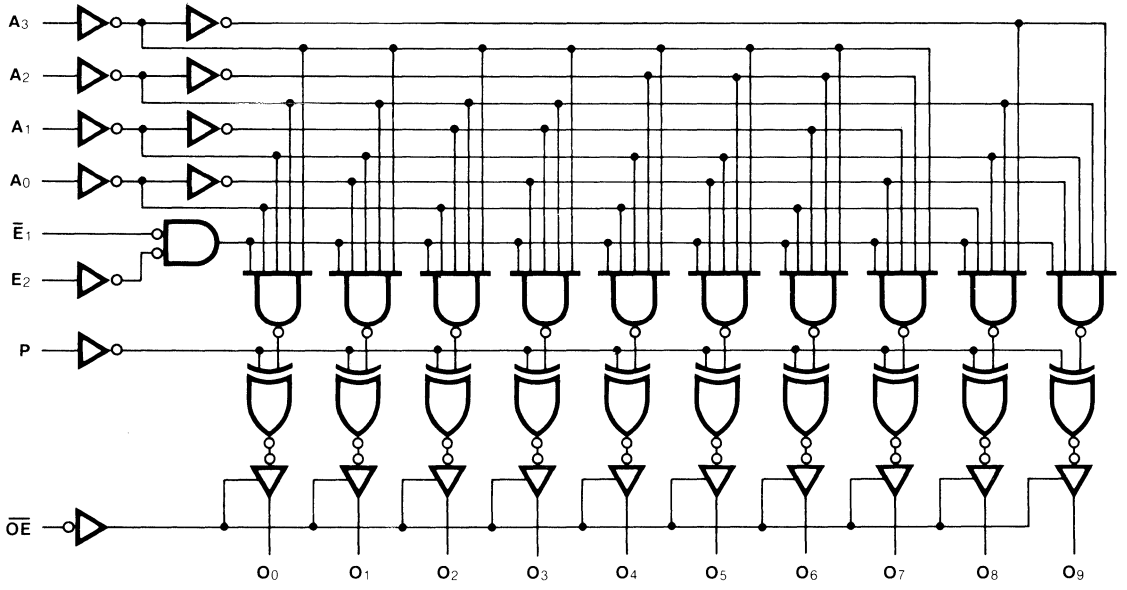
Pin Names	Description	54F/74F(U.L.) HIGH/LOW
A_0-A_3	Address Inputs	0.5/0.375
$\overline{E}_1$	Enable Input (Active LOW)	0.5/0.375
E_2	Enable Input (Active HIGH)	0.5/0.375
$\overline{OE}$	Output Enable Input (Active LOW)	0.5/0.375
P	Polarity Control Input	0.5/0.375
O_0-O_9	3-State Outputs	75/15 (12.5)

Truth Table

Function	Inputs							Outputs									
	$\overline{OE}$	$\overline{E}_1$	E_2	A_3	A_2	A_1	A_0	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7	O_8	O_9
High Impedance	H	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
Disable	L	H	X	X	X	X	X	Outputs Equal P Input									
	L	X	L	X	X	X	X										
Active HIGH Output (P = L)	L	L	H	L	L	L	L	H	L	L	L	L	L	L	L	L	L
	L	L	H	L	L	L	H	L	H	L	L	L	L	L	L	L	L
	L	L	H	L	L	H	L	L	L	H	L	L	L	L	L	L	L
	L	L	H	L	L	H	H	L	L	L	H	L	L	L	L	L	L
	L	L	H	L	H	L	L	L	L	L	L	H	L	L	L	L	L
	L	L	H	L	H	L	H	L	L	L	L	L	H	L	L	L	L
	L	L	H	L	H	H	L	L	L	L	L	L	L	H	L	L	L
	L	L	H	L	H	H	H	L	L	L	L	L	L	L	H	L	L
	L	L	H	H	L	L	L	L	L	L	L	L	L	L	L	H	L
	L	L	H	H	L	L	H	L	L	L	L	L	L	L	L	L	H
	L	L	H	H	X	H	X	L	L	L	L	L	L	L	L	L	L
	L	L	H	H	H	X	X	L	L	L	L	L	L	L	L	L	L
Active LOW Output (P = H)	L	L	H	L	L	L	L	H	H	H	H	H	H	H	H	H	H
	L	L	H	L	L	L	H	H	L	H	H	H	H	H	H	H	H
	L	L	H	L	L	H	L	H	H	L	H	H	H	H	H	H	H
	L	L	H	L	L	H	H	H	H	H	L	H	H	H	H	H	H
	L	L	H	L	H	L	L	H	H	H	H	L	H	H	H	H	H
	L	L	H	L	H	L	H	H	H	H	H	H	L	H	H	H	H
	L	L	H	L	H	H	L	H	H	H	H	H	H	L	H	H	H
	L	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H
	L	L	H	H	L	L	L	H	H	H	H	H	H	H	H	L	H
	L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	L
	L	L	H	H	X	H	X	H	H	H	H	H	H	H	H	H	H
	L	L	H	H	H	X	X	H	H	H	H	H	H	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CCZ}	Power Supply Current		44	66	mA	A_0-A_3, $\overline{E}_1$ = Gnd $\overline{OE}$, E_2, P = HIGH

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$			T_A, V_{CC} = Mil $C_L = 50\ pF$		T_A, V_{CC} = Com $C_L = 50\ pF$			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	6.0	11.0	16.0			6.0	17.0	ns	3-1, 3-10
t_{PHL}	A_n to O_n	4.0	7.5	11.0			4.0	12.0		
t_{PLH}	Propagation Delay	5.0	8.5	14.5			5.0	15.5		
t_{PHL}	$\overline{E}_1$ to O_n	4.0	6.5	9.0			4.0	10.0		
t_{PLH}	Propagation Delay	6.0	11.0	16.0			6.0	17.0	ns	3-1, 3-10
t_{PHL}	E_2 to O_n	5.0	10.0	14.0			5.0	15.0		
t_{PLH}	Propagation Delay	6.0	11.5	18.0			6.0	20.0		
t_{PHL}	P to O_n	6.0	11.0	16.0			6.0	17.0		
t_{PZH}	Output Enable Time	3.0	5.5	10.5			3.0	11.5	ns	3-1, 3-12, 3-13
t_{PLZ}	$\overline{OE}$ to O_n	5.0	9.0	13.0			5.0	14.0		
t_{PHZ}	Output Disable Time	2.0	4.0	6.0			2.0	7.0		
t_{PLZ}	$\overline{OE}$ to O_n	3.0	5.0	7.0			3.0	8.0		

54F/74F538

1-of-8 Decoder
With 3-State Outputs

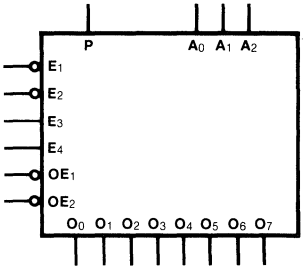
Description

The 'F538 decoder/demultiplexer accepts three Address (A_0-A_2) input signals and decodes them to select one of eight mutually exclusive outputs. A polarity control input (P) determines whether the outputs are active LOW or active HIGH. A HIGH Signal on either of the active LOW Output Enable ($\overline{OE}$) inputs forces all outputs to the high impedance state. Two active HIGH and two active LOW input enables are available for easy expansion to 1-of 32 decoding with four packages, or for data demultiplexing to 1-of-8 or 1-of-16 destinations.

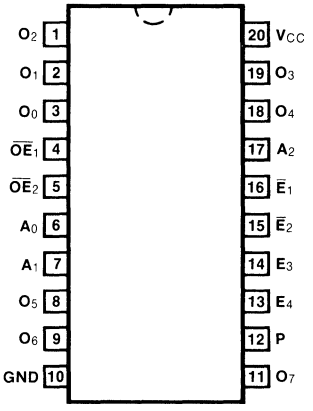
- **Output Polarity Control**
- **Data Demultiplexing Capability**
- **Multiple Enables for Expansion**
- **3-State Outputs**

Ordering Code: See Section 5

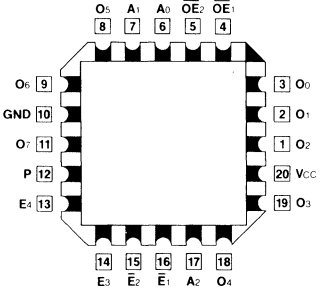
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC

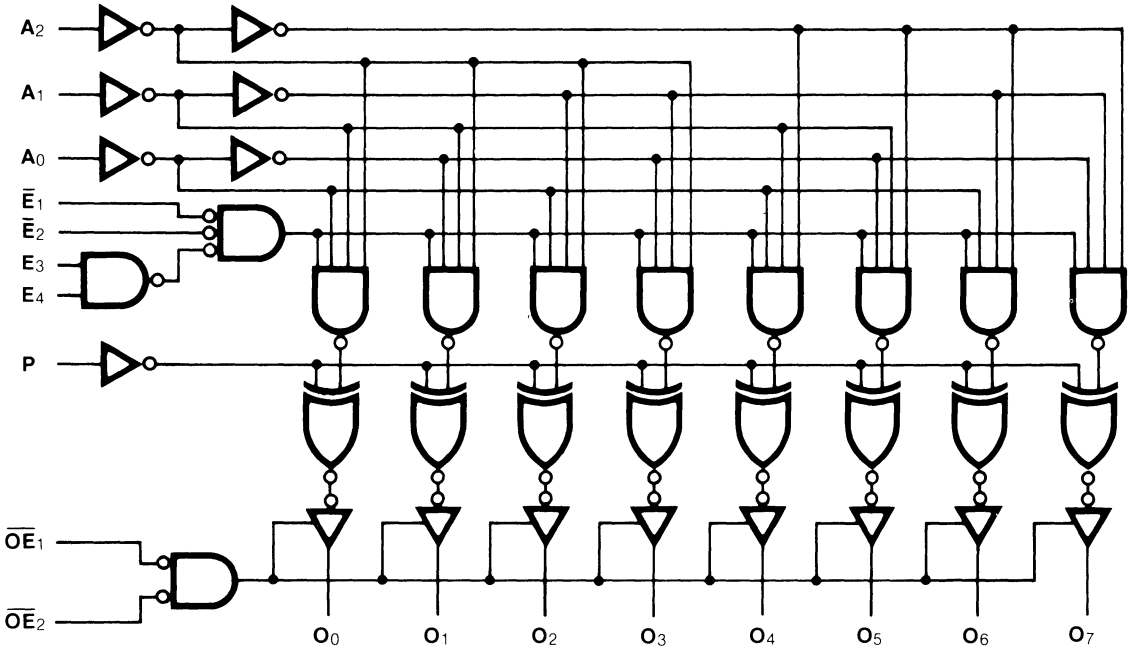


Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
A_0-A_2	Address Inputs	0.5/0.375
$\overline{E}_1$, $\overline{E}_2$	Enable Inputs (Active LOW)	0.5/0.375
E_3, E_4	Enable Inputs (Active HIGH)	0.5/0.375
P	Polarity Control Input	0.5/0.375
$\overline{OE}_1$, $\overline{OE}_2$	Output Enable Inputs (Active LOW)	0.5/0.375
O_0-O_7	3-State Outputs	75/15 (12.5)

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Truth Table

Function	Inputs									Outputs							
	$\overline{OE}_1$	$\overline{OE}_2$	$\overline{E}_1$	$\overline{E}_2$	E_3	E_4	A_2	A_1	A_0	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7
High Impedance	H	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z
	X	H	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z
Disable	L	L	H	X	X	X	X	X	X	Outputs Equal P Input							
	L	L	X	H	X	X	X	X	X								
	L	L	X	X	L	X	X	X	X								
	L	L	X	X	X	L	X	X	X								
Active HIGH Output (P = L)	L	L	L	L	H	H	L	L	L	H	L	L	L	L	L	L	L
	L	L	L	L	H	H	L	L	H	L	H	L	L	L	L	L	L
	L	L	L	L	H	H	L	H	L	L	L	H	L	L	L	L	L
	L	L	L	L	H	H	L	H	H	L	L	L	H	L	L	L	L
	L	L	L	L	H	H	H	L	L	L	L	L	L	H	L	L	L
	L	L	L	L	H	H	H	L	H	L	L	L	L	L	H	L	L
	L	L	L	L	H	H	H	H	L	L	L	L	L	L	L	H	L
	L	L	L	L	H	H	H	H	H	L	L	L	L	L	L	L	H
Active LOW Output (P = H)	L	L	L	L	H	H	L	L	L	L	H	H	H	H	H	H	H
	L	L	L	L	H	H	L	L	H	H	L	H	H	H	H	H	H
	L	L	L	L	H	H	L	H	L	H	H	L	H	H	H	H	H
	L	L	L	L	H	H	L	H	H	H	H	H	L	H	H	H	H
	L	L	L	L	H	H	H	L	L	H	H	H	H	L	H	H	H
	L	L	L	L	H	H	H	L	H	H	H	H	H	H	L	H	H
	L	L	L	L	H	H	H	H	L	H	H	H	H	H	H	L	H
	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		37	56	mA	A_0-A_2, $\overline{E}_1$, $\overline{E}_2$ = Gnd $\overline{OE}_1$, $\overline{OE}_2$, E_3, E_4, P = HIGH

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			54F T_A, V_{CC} = Mil C_L = 50 pF		74F T_A, V_{CC} = Com C_L = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n to O_n	6.0 4.0	11.0 7.5	16.0 11.0			6.0 4.0	17.0 12.0	ns	3-1, 3-10
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to O_n	5.0 4.0	8.5 6.5	15.0 9.0			5.0 4.0	16.0 10.0		
t_{PLH} t_{PHL}	Propagation Delay E_3 or E_4 to O_n	6.0 5.0	11.0 10.0	16.0 14.0			6.0 5.0	17.0 15.0	ns	3-1, 3-10
t_{PLH} t_{PHL}	Propagation Delay P to O_n	6.0 6.0	11.5 11.0	18.0 16.0			6.0 6.0	20.0 17.0		
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}_1$ or $\overline{OE}_2$ to O_n	3.0 5.0	5.5 9.0	10.0 13.0			3.0 5.0	11.0 14.0	ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}_1$ or $\overline{OE}_2$ to O_n	2.0 3.0	4.0 5.0	6.0 8.0			2.0 3.0	7.0 9.0		

54F/74F539

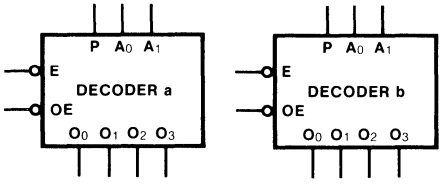
Dual 1-of-4 Decoder With 3-State Outputs

Description

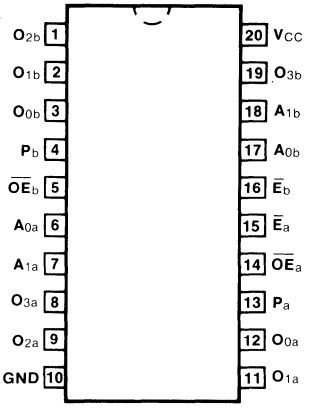
The 'F539 contains two independent decoders. Each accepts two Address (A_0, A_1) input signals and decodes them to select one of four mutually exclusive outputs. A polarity control input (P) determines whether the outputs are active HIGH (P = L) or active LOW (P = H). An active LOW input Enable ($\overline{E}$) is available for data demultiplexing; data is routed to the selected output in non-inverted form in the active LOW mode or in inverted form in the active HIGH mode. A HIGH signal on the active LOW Output Enable ($\overline{OE}$) input forces the 3-state outputs to the high impedance state.

Ordering Code: See Section 5

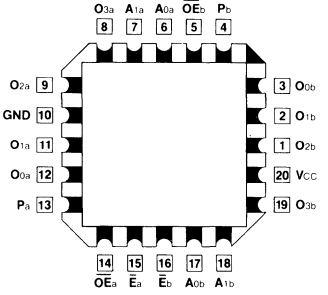
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
A_{0a}-A_{1a}	Side A Address Inputs	0.5/0.375
A_{0b}-A_{1b}	Side B Address Inputs	0.5/0.375
$\overline{E}_a$, $\overline{E}_b$	Enable Inputs (Active LOW)	0.5/0.375
$\overline{OE}_a$, $\overline{OE}_b$	Output Enable Inputs (Active LOW)	0.5/0.375
P_a, P_b	Polarity Control Inputs	0.5/0.375
O_{0a}-O_{3a}	Side A 3-State Outputs	75/15 (12.5)
O_{0b}-O_{3b}	Side B 3-State Outputs	75/15 (12.5)

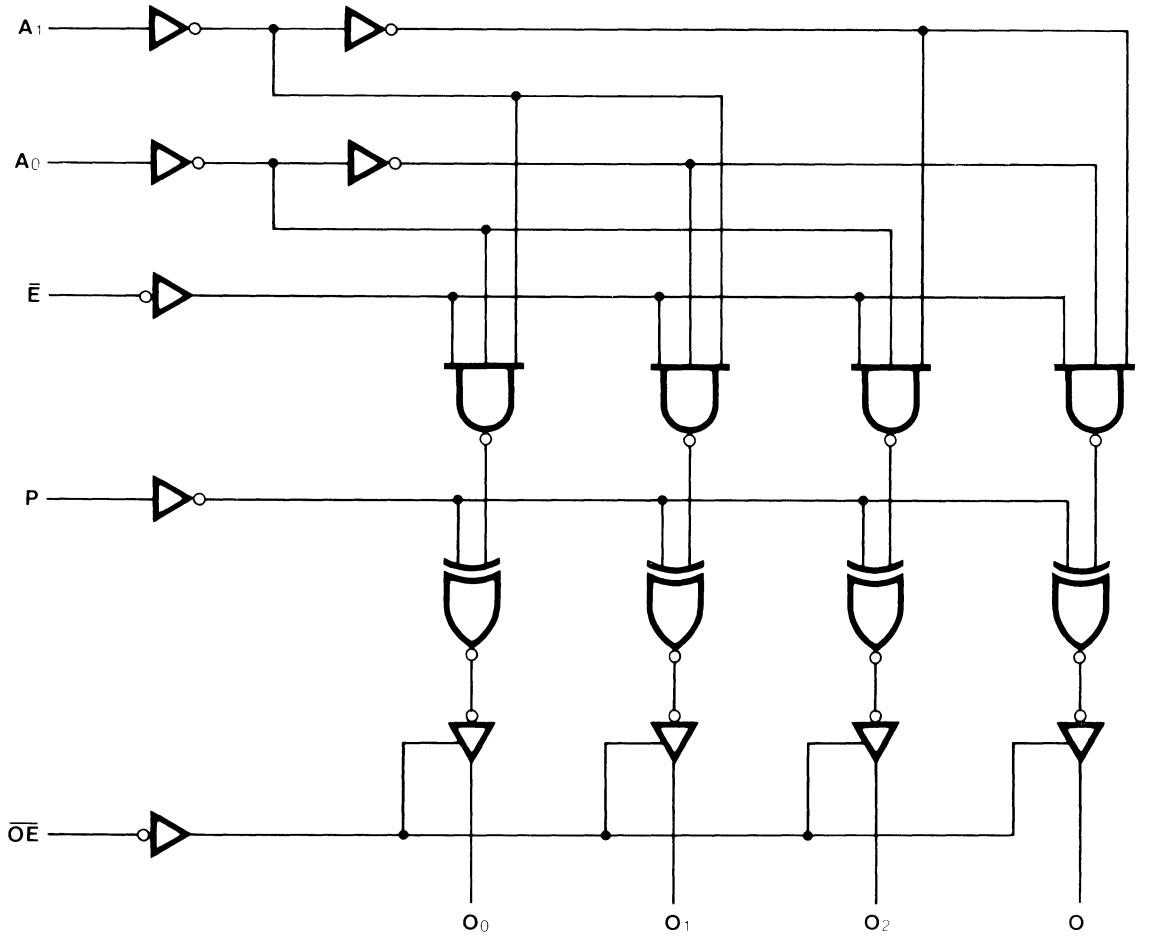
Truth Table (each half)

Function	Inputs				Outputs			
	$\overline{OE}$	$\overline{E}$	A_1	A_0	O_0	O_1	O_2	O_3
High Impedance	H	X	X	X	Z	Z	Z	Z
Disable	L	H	X	X	$O_n = P$			
Active HIGH Output (P = L)	L	L	L	L	H	L	L	L
	L	L	L	H	L	H	L	L
	L	L	H	L	L	L	H	L
	L	L	H	H	L	L	L	H
Active LOW Output (P = H)	L	L	L	L	L	H	H	H
	L	L	L	H	H	L	H	H
	L	L	H	L	H	H	L	H
	L	L	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

4

Logic Diagram (one half shown)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CCZ}	Power Supply Current (All Outputs OFF)		40	60	mA	A_0, A_1, $\overline{E}$ = Gnd $\overline{OE}$, P = HIGH

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\,V$ $C_L = 50\,pF$			T_A, V_{CC} = Mil $C_L = 50\,pF$		T_A, V_{CC} = Com $C_L = 50\,pF$			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n to O_n	9.0 4.0	14.5 9.5	18.5 12.0			9.0 4.0	19.5 13.0	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to O_n	5.5 4.0	12.0 7.5	16.0 9.5			5.5 4.0	17.0 10.5	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay P to O_n	7.5 5.0	14.5 11.0	21.5 16.5			7.5 5.0	22.5 17.5	ns	3-1 3-10
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	4.5 5.5	8.0 10.0	10.5 13.0			4.5 5.5	11.5 14.0	ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n	2.0 3.0	4.5 6.5	6.0 8.5			2.0 3.0	7.0 9.5		

54F/74F540 • 54F/74F541

Octal Buffer/Line Driver With 3-State Outputs

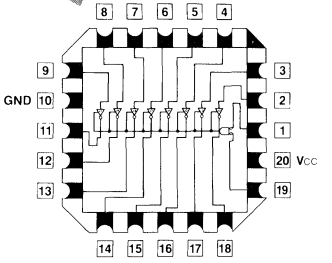
Description

The 'F540 and 'F541 are similar in function to the 'F240 and 'F244 respectively, except that the inputs and outputs are on opposite sides of the package (see Connection Diagrams). This pinout arrangement makes these devices especially useful as output ports for microprocessors, allowing ease of layout and greater PC board density.

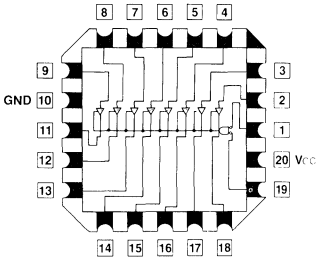
- **3-State Outputs Drive Bus Lines**
- **Inputs and Outputs Opposite Side of Package, Allowing Easier Interface to Microprocessors**

Ordering Code: See Section 5

Connection Diagrams

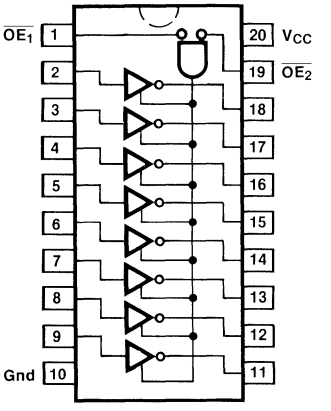


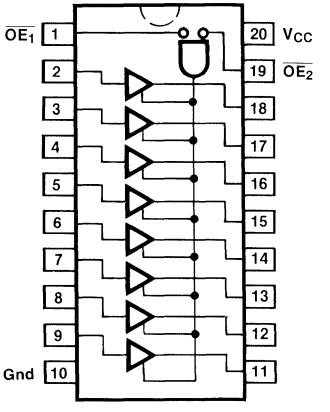
'F540



'F541

Pin Assignment for LCC and PCC





Pin Assignment for DIP and SOIC

Truth Table

Inputs			Outputs	
$\overline{OE}_1$	$\overline{OE}_2$	D	'F540	'F541
L	L	H	L	H
H	X	X	Z	Z
X	H	X	Z	Z
L	L	L	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
$\overline{OE}_1$, $\overline{OE}_2$	3-State Output Enable Input (Active LOW)	0.5/0.375
OE_2	3-State Output Enable Input (Active HIGH)	0.5/0.375
	Inputs	0.5/0.375
	Outputs	75/40 (30)

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter		54F/74F Min	54F/74F Typ	54F/74F Max	Units	Conditions	
I_{CCH}	Power Supply Current	'F540		20	30	mA	Outputs HIGH	V_{CC} = Max
		'F541		40	60			
I_{CCL}		'F540		50	75	mA	Outputs LOW	
		'F541		60	90			
I_{CCZ}		'F540		40	60	mA	Outputs OFF	
		'F541		60	90			

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF Min	Typ	Max	54F T_A, V_{CC} = Mil C_L = 50 pF Min	Max	74F T_A, V_{CC} = Com C_L = 50 pF Min	Max	Units	Fig. No.
t_{PLH} t_{PHL}	Propagation Delay Data to Output ('F540)			5.0 5.0					ns	3-1 3-3
t_{PZH} t_{PZL}	Output Enable Time ('F540)			7.0 8.0					ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time ('F540)			7.0 8.0						
t_{PLH} t_{PHL}	Propagation Delay Data to Output ('F541)			6.0 5.0					ns	3-1 3-4
t_{PZH} t_{PZL}	Output Enable Time ('F541)			7.0 8.0					ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time ('F541)			7.0 8.0						

54F/74F543

Octal Registered Transceiver

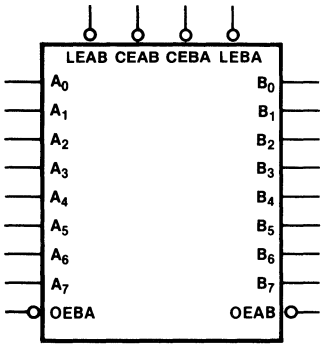
Description

The 'F543 octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable and Output Enable inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow. The A outputs are guaranteed to sink 20 mA while the B outputs are rated for 64 mA.

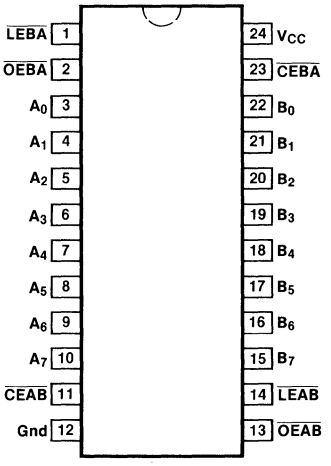
- **8-Bit Octal Transceiver**
- **Back-to-Back Registers for Storage**
- **Separate Controls for Data Flow in Each Direction**
- **B Outputs Sink 64 mA**
- **300 mil Slim Package**

Ordering Code: See Section 5

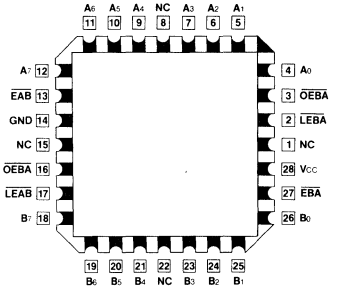
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)	0.5/0.375
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)	0.5/0.375
$\overline{CEAB}$	A-to-B Enable Input (Active LOW)	0.5/0.75
$\overline{CEBA}$	B-to-A Enable Input (Active LOW)	0.5/0.75
$\overline{LEAB}$	A-to-B Latch Enable Input (Active LOW)	0.5/0.375
$\overline{LEBA}$	B-to-A Latch Enable Input (Active LOW)	0.5/0.375
A_0-A_7	A-to-B Data Inputs or	1.75/0.406
	B-to-A 3-State Outputs	25/12
B_0-B_7	B-to-A Data Inputs or	1.75/0.406
	A-to-B 3-State Outputs	75/40 (30)

Functional Description

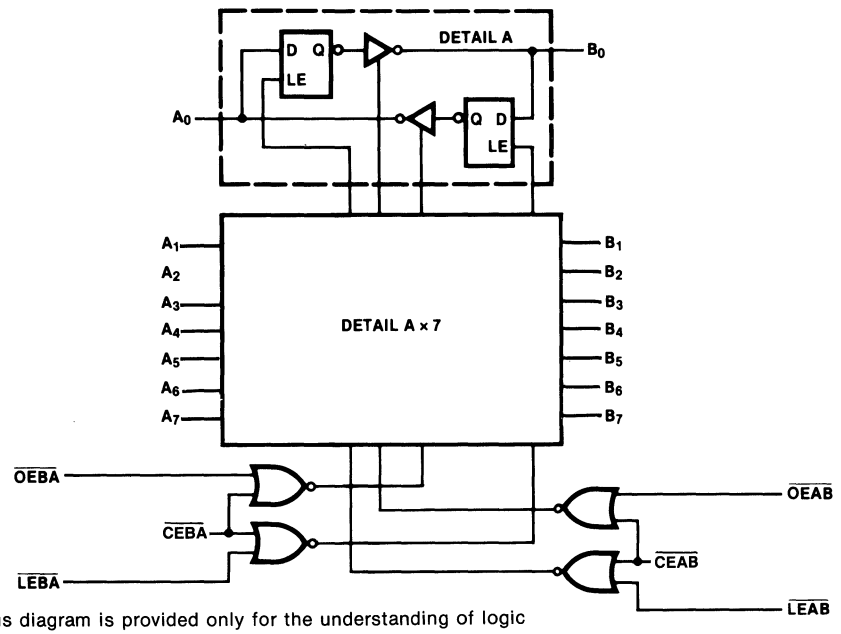
The 'F543 contains two sets of eight D-type latches, with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable ($\overline{CEAB}$) input must be LOW in order to enter data from A_0-A_7 or take data from B_0-B_7, as indicated in the Data I/O Control Table. With $\overline{CEAB}$ LOW, a LOW signal on the A-to-B Latch Enable ($\overline{LEAB}$) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $\overline{LEAB}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{CEAB}$ and $\overline{OEAB}$ both LOW, the 3-state B output buffers are active and reflect the data present at the output of the A latches. Control of data flow from B to A is similar, but using the $\overline{CEAB}$, $\overline{LEBA}$ and $\overline{OEBA}$ inputs.

Data I/O Control Table

Inputs			Latch Status	Output Buffers
$\overline{EAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A-to-B	B_0-B_7
H	X	X	Storing	High Z
X	H		Storing	—
X		H	—	High Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous* A Inputs

* Before $\overline{LEAB}$ LOW-to-HIGH Transition
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
A-to-B data flow shown; B-to-A flow control is the same, except using $\overline{CEBA}$, $\overline{LEBA}$ and $\overline{OEBA}$

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CCH} I_{CCL} I_{CCZ}	Power Supply Current		67 83 83	100 125 125	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			54F T_A, V_{CC} = Mil, C_L = 50 pF		74F T_A, V_{CC} = Com, C_L = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay, Transparent Mode A_n to B_n or B_n to A_n	3.0 3.0	5.5 5.0	7.5 6.5			3.0 3.0	8.5 7.5	ns	3-1, 3-3 3-4
t_{PLH} t_{PHL}	Propagation Delay $\overline{LEBA}$ to A_n	4.5 4.5	8.5 8.5	11.0 11.0			4.5 4.5	12.5 12.5	ns	3-1 3-8
t_{PLH} t_{PHL}	Propagation Delay $\overline{LEAB}$ to B_n	4.5 4.5	8.5 8.5	11.0 11.0			4.5 4.5	12.5 12.5	ns	3-1 3-8
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n $\overline{CEBA}$ or $\overline{CEAB}$ to A_n or B_n	3.0 4.0	7.0 7.5	9.0 10.5			3.0 4.0	10.0 12.0	ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n $\overline{CEBA}$ or $\overline{CEAB}$ to A_n or B_n	2.5 2.5	6.0 5.5	8.0 7.5			2.5 2.5	9.0 8.5		

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F T_A = +25°C, V_{CC} = +5.0 V			54F T_A, V_{CC} = Mil		74F T_A, V_{CC} = Com		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW A_n or B_n to $\overline{LEBA}$ or $\overline{LEAB}$	3.0 3.0					3.5 3.5		ns	3-14
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW A_n or B_n to $\overline{LEBA}$ or $\overline{LEAB}$	3.0 3.0					3.5 3.5			
$t_w(L)$	Latch Enable, B to A Pulse Width, LOW	8.0					9.0		ns	3-7

54F/74F544

Octal Registered Transceiver

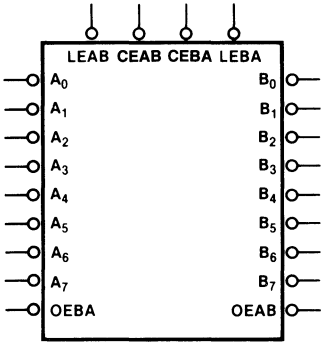
Description

The 'F544 octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable and Output Enable inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow. The A outputs are guaranteed to sink 20 mA while the B outputs are rated for 64 mA. The 'F544 inverts data in both directions.

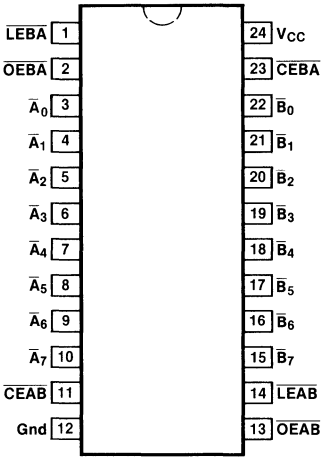
- **8-Bit Octal Transceiver**
- **Back-to-Back Registers for Storage**
- **Separate Controls for Data Flow in Each Direction**
- **A Outputs Sink 20 mA, B Outputs Sink 64 mA**
- **300 mil Slim Package**

Ordering Code: See Section 5

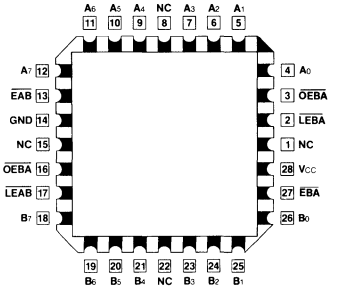
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)	0.5/0.375
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)	0.5/0.375
$\overline{CEAB}$	A-to-B Enable Input (Active LOW)	0.5/0.75
$\overline{CEBA}$	B-to-A Enable Input (Active LOW)	0.5/0.75
$\overline{LEAB}$	A-to-B Latch Enable Input (Active LOW)	0.5/0.375
$\overline{LEBA}$	B-to-A Latch Enable Input (Active LOW)	0.5/0.375
$\overline{A}_0$-$\overline{A}_7$	A-to-B Data Inputs or	1.75/0.406
	B-to-A 3-State Outputs	75/15 (12.5)
$\overline{B}_0$-$\overline{B}_7$	B-to-A Data Inputs or	1.75/0.406
	A-to-B 3-State Outputs	75/40 (30)

Functional Description

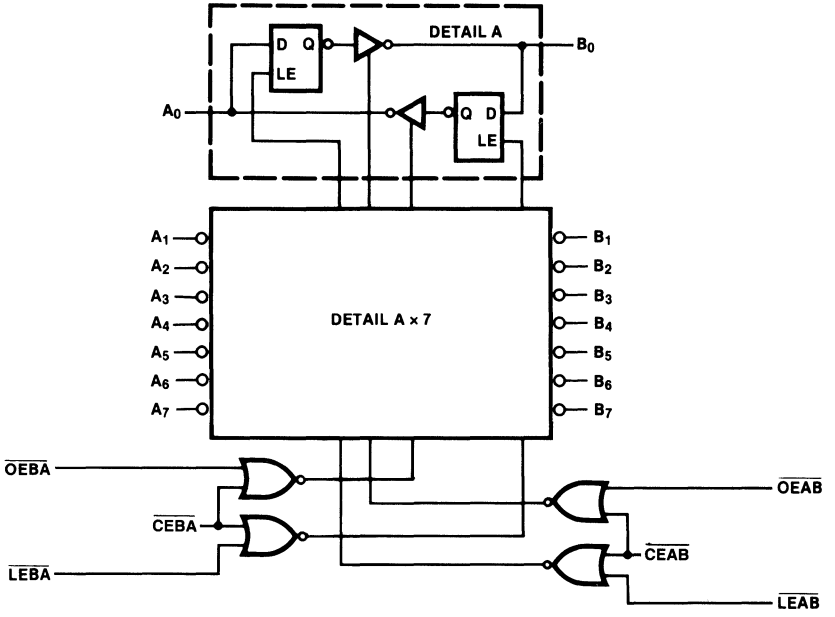
The 'F544 contains two sets of eight D-type latches, with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable ($\overline{CEAB}$) input must be LOW in order to enter data from $\overline{A}_0$-$\overline{A}_7$ or take data from $\overline{B}_0$-$\overline{B}_7$, as indicated in the Data I/O Control Table. With $\overline{CEAB}$ LOW, a LOW signal on the A-to-B Latch Enable ($\overline{LEAB}$) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $\overline{LEAB}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{CEAB}$ and $\overline{OEAB}$ both LOW, the 3-state B output buffers are active and reflect the data present at the output of the A latches. Control of data flow from B to A is similar, but using the $\overline{CEBA}$, $\overline{LEBA}$ and $\overline{OEBA}$ inputs.

Data I/O Control Table

Inputs			Latch Status	Output Buffers
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A-to-B	$\overline{B}_0$-$\overline{B}_7$
H	X	X	Storing	High Z
X	H		Storing	——
X		H	——	High Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous* A Inputs

* Before $\overline{LEAB}$ LOW-to-HIGH Transition
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
A-to-B data flow shown; B-to-A flow control is the same, except using $\overline{CEBA}$, $\overline{LEBA}$ and $\overline{OEBA}$

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CCH} I_{CCL} I_{CCZ}	Power Supply Current		70 85 83	105 130 125	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			54F T_A, V_{CC} = Mil C_L = 50 pF		74F T_A, V_{CC} = Com C_L = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay, Transparent Mode $\overline{A}_n$ to $\overline{B}_n$ or $\overline{B}_n$ to $\overline{A}_n$	3.0 3.0	7.0 5.0	9.5 6.5			3.0 3.0	10.5 7.5	ns	3-1, 3-3 3-4
t_{PLH} t_{PHL}	Propagation Delay $\overline{LEBA}$ to $\overline{A}_n$	6.0 4.0	10.0 7.0	13.0 9.5			6.0 4.0	14.5 10.5	ns	3-1 3-8
t_{PLH} t_{PHL}	Propagation Delay $\overline{LEAB}$ to $\overline{B}_n$	6.0 4.0	10.0 7.0	13.0 9.5			6.0 4.0	14.5 10.5	ns	3-1 3-8
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEBA}$ or $\overline{OEAB}$ to $\overline{A}_n$ or $\overline{B}_n$ $\overline{CEBA}$ or $\overline{CEAB}$ to $\overline{A}_n$ or $\overline{B}_n$	3.0 4.0	7.0 7.5	9.0 10.5			3.0 4.0	10.0 12.0	ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEBA}$ or $\overline{OEAB}$ to $\overline{A}_n$ or $\overline{B}_n$ $\overline{CEBA}$ or $\overline{CEAB}$ to $\overline{A}_n$ or $\overline{B}_n$	2.5 2.5	6.0 5.5	8.0 7.5			2.5 2.5	9.0 8.5		

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F T_A = +25°C V_{CC} = +5.0 V			54F T_A, V_{CC} = Mil		74F T_A, V_{CC} = Com		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_s(H) t_s(L)	Setup Time, HIGH or LOW $\overline{A}_n$ or $\overline{B}_n$ to $\overline{LEBA}$ or $\overline{LEAB}$	3.0 3.0					3.0 3.0		ns	3-14
t_h(H) t_h(L)	Hold Time, HIGH or LOW $\overline{A}_n$ or $\overline{B}_n$ to $\overline{LEBA}$ or $\overline{LEAB}$	3.0 3.0					3.0 3.0			
t_w(L)	Latch Enable, B to A Pulse Width, LOW	6.0					7.5		ns	3-7

54F/74F545

Octal Bidirectional Transceiver With 3-State Inputs/Outputs

Description

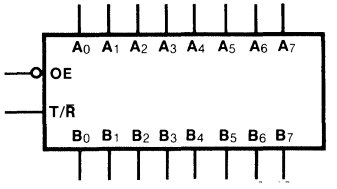
The 'F545 is an 8-bit, 3-state, high-speed transceiver. It provides bidirectional drive for bus-oriented microprocessor and digital communications systems. Straight through bidirectional transceivers are featured, with 20 mA bus drive capability on the A ports and 64 mA bus drive capability on the B ports.

One input, Transmit/Receive ($T/\overline{R}$) determines the direction of logic signals through the bidirectional transceiver. Transmit enables data from A ports to B ports; Receive enables data from B ports to A ports. The Output Enable input disables both A and B ports by placing them in a 3-state condition.

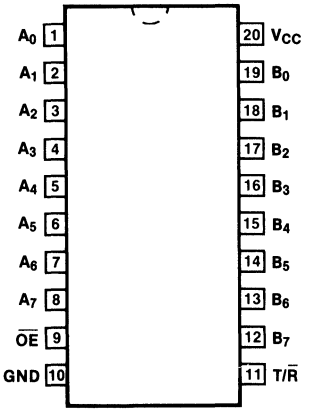
- **Higher Drive than 8304**
- **8-Bit Bidirectional Data Flow Reduces System Package Count**
- **3-State Inputs/Outputs for Interfacing with Bus-Oriented Systems**
- **20 mA and 64 mA Bus Drive Capability on A and B Ports, Respectively**
- **Transmit/Receive and Output Enable Simplify Control Logic**

Ordering Code: See Section 5

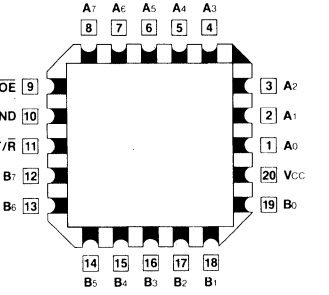
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

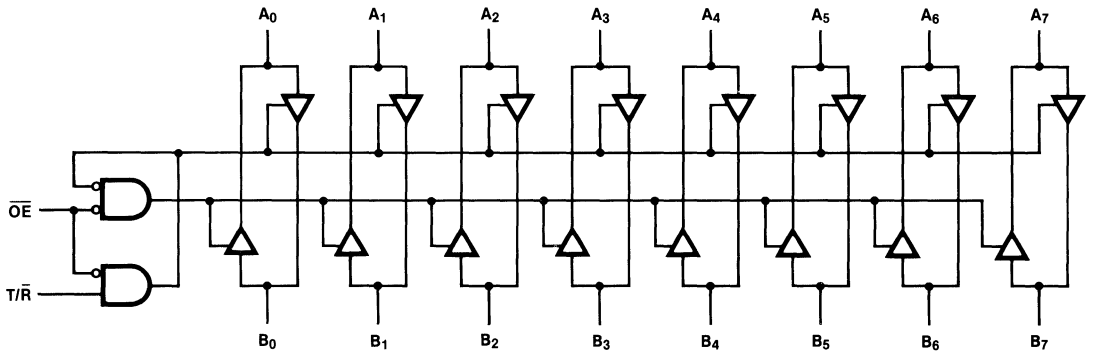
Pin Names	Description	54F/74F(U.L.) HIGH/LOW
$\overline{OE}$	Output Enable Input (Active LOW)	0.5/0.75
$T/\overline{R}$	Transmit/Receive Input	0.5/0.75
A_0-A_7	Side A 3-State Inputs or	1.75/0.406
	3-State Outputs	75/15(12.5)
B_0-B_7	Side B 3-State Inputs or	1.75/0.406
	3-State Outputs	75/40 (30)

Truth Table

Inputs		Outputs
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CCH}	Power Supply Current		70	90	mA	V_{CC} = Max
I_{CCL}			95	120		
I_{CCZ}			85	110		

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$			T_A, V_{CC} = Mil $C_L = 50\ pF$		T_A, V_{CC} = Com $C_L = 50\ pF$			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	2.5	4.2	6.0	2.0	7.5	2.5	7.0	ns	3-1
t_{PHL}	A_n to B_n or B_n to A_n	2.5	4.6	6.0	2.0	7.5	2.5	7.0		3-4
t_{PZH}	Output Enable Time	3.0	5.3	7.0	2.5	9.0	3.0	8.0	ns	3-1 3-12 3-13
t_{PZL}		3.5	6.0	8.0	3.0	10.0	3.5	9.0		
t_{PHZ}	Output Disable Time	3.0	5.0	6.5	2.5	9.0	3.0	7.5		
t_{PLZ}		2.0	5.0	6.5	2.0	10.0	2.0	7.5		

54F/74F547

Octal Decoder/Demultiplexer With Address Latches and Acknowledge

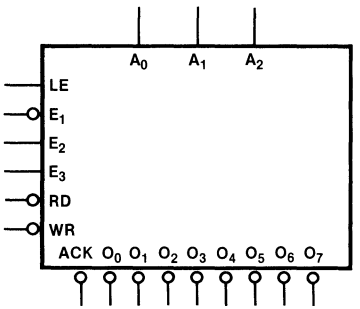
Description

The 'F547 is a 3-to-8 line address decoder with latches for address storage. Designed primarily to simplify multiple chip selection in a microprocessor system, it contains one active LOW and two active HIGH Enables to conserve address space. Also included is an active LOW Acknowledge output that responds to either a Read or Write input signal when the Enables are active.

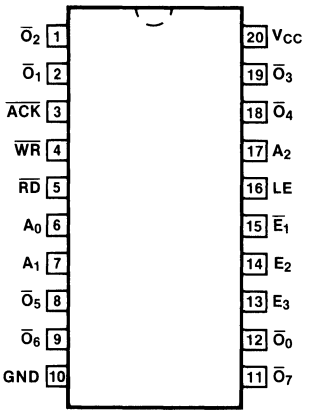
- **3-to-8 Line Address Decoder**
- **Address Storage Latches**
- **Multiple Enables for Address Extension**
- **Open Collector Acknowledge Output**

Ordering Code: See Section 5

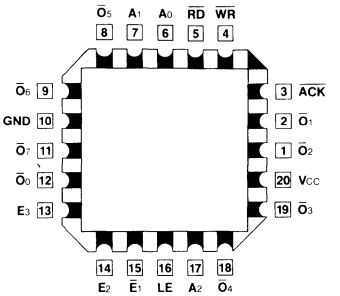
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
A_0-A_2	Output Select Address Inputs	0.5/0.375
$\overline{E}_1$	Chip Enable Input (Active LOW)	0.5/0.375
E_2, E_3	Chip Enable Inputs	0.5/0.375
LE	Latch Enable Input	0.5/0.375
$\overline{RD}$	Read Acknowledge Input (Active LOW)	0.5/0.375
$\overline{WR}$	Write Acknowledge Input (Active LOW)	0.5/0.375
$\overline{ACK}$	Open Collector Acknowledge Output (Active LOW)	OC*/12.5
$\overline{O}_0$-$\overline{O}_7$	Decoded Outputs (Active LOW)	25/12.5

*OC = Open Collector

Functional Description

When enabled, the 'F547 accepts the A_0-A_2 Address inputs and decodes them to select one of eight active LOW, mutually exclusive outputs, as shown in the Decoder Truth Table. With LE HIGH, the Address latches are transparent and the output selection changes each time the A_0-A_2 address changes. When LE is LOW, the latches store the last valid address preceding the HIGH-to-LOW transition of the LE input signal. For applications in which the separation of latch enable and chip enable functions is not required, LE and $\overline{E}_1$ can be tied together, such that when HIGH the outputs are OFF and the latches are transparent, and when LOW the latches are storing and the selected output is enabled.

The open collector Acknowledge ($\overline{ACK}$) output is normally HIGH (i.e. OFF) and goes LOW when $\overline{E}_1$, E_2 and E_3 are all active and either the Read ($\overline{RD}$) or Write ($\overline{WR}$) input is LOW, as indicated in the Acknowledge Truth Table.

Acknowledge Truth Table

Inputs					Output
$\overline{E}_1$	E_2	E_3	$\overline{RD}$	$\overline{WR}$	$\overline{ACK}$
H	X	X	X	X	H
X	L	X	X	X	H
X	X	L	X	X	H
L	H	H	H	H	H
L	H	H	L	X	L
L	H	H	X	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Latch and Output Status Table

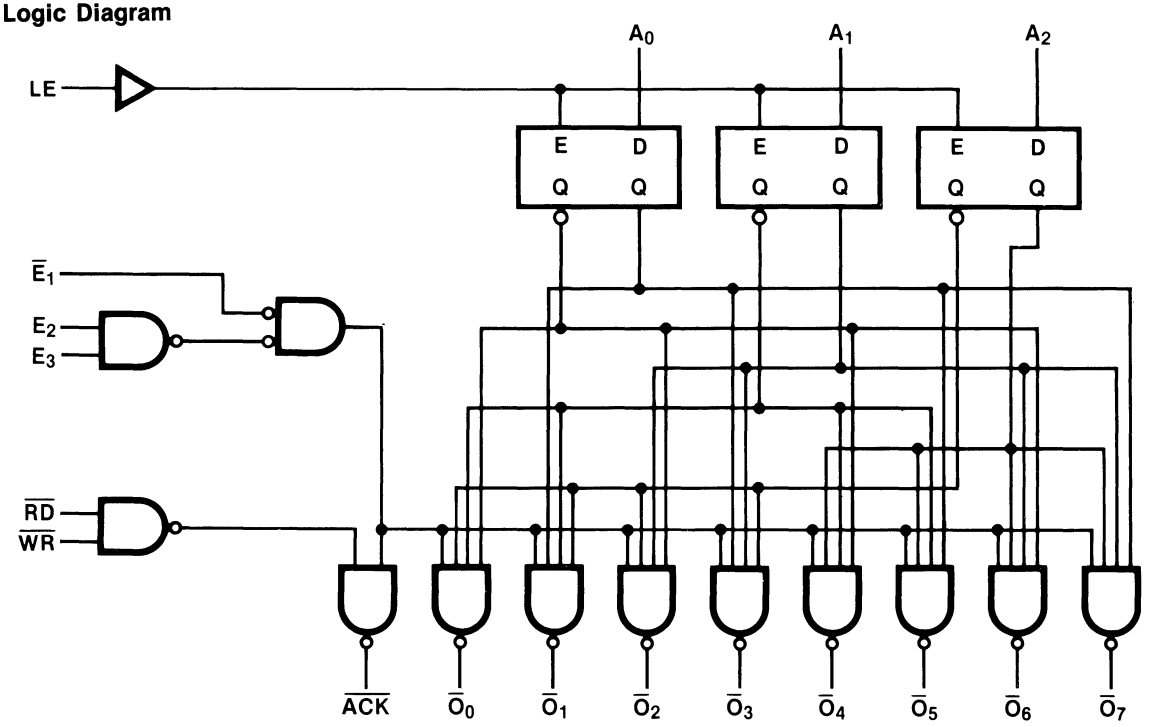
Inputs				Latch	Decoder
$\overline{E}_1$	E_2	E_3	LE	Status	Outputs
L	H	H	H	Transparent	—
L	H	H	L	Storing	Selected Output LOW
H	X	X	X	Storing	All Outputs HIGH
X	L	X	X	Storing	All Outputs HIGH
X	X	L	X	Storing	All Outputs HIGH

Decoder Truth Table*

Inputs			Outputs							
A_2	A_1	A_0	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H
L	H	L	H	H	L	H	H	H	H	H
L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	H	H	H	L	H	H	H
H	L	H	H	H	H	H	H	L	H	H
H	H	L	H	H	H	H	H	H	L	H
H	H	H	H	H	H	H	H	H	H	L

*Assuming $\overline{E}_1$, LOW; E_2 and E_3, HIGH

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		17	25	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F $T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$			54F $T_A, V_{CC} =$ Mil $C_L = 50\ pF$		74F $T_A, V_{CC} =$ Com $C_L = 50\ pF$		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n to $\overline{O}_n$	4.0 5.0	7.0 9.0	9.0 12.0	3.0 5.0	10.5 13.0	4.0 5.0	10.0 13.0	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_1$ to $\overline{O}_n$	4.0 4.0	6.5 6.5	8.5 8.5	3.0 3.5	10.0 10.0	4.0 4.0	9.5 9.5	ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay LE to $\overline{O}_n$	4.0 5.0	7.5 14.5	9.5 18.0	4.0 5.0	11.5 20.0	4.0 5.0	10.5 19.0	ns	3-1 3-3
t_{PLH} t_{PHL}	Propagation Delay E_2 or E_3 to $\overline{O}_n$	5.0 5.0	8.5 8.5	11.0 11.0	4.5 4.5	12.5 12.5	5.0 5.0	12.0 12.0	ns	3-1 3-3
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_1$, $\overline{RD}$ or $\overline{WR}$ to $\overline{ACK}$	6.5 4.0	11.0 7.5	14.0 9.5	6.5 3.5	16.0 11.0	6.5 4.0	15.0 10.5	ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay E_2 or E_3 to $\overline{ACK}$	8.0 5.0	13.0 8.5	16.5 11.0	8.0 5.0	18.5 12.5	8.0 5.0	17.5 12.0	ns	3-1 3-3

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F $T_A = +25°C$ $V_{CC} = +5.0\ V$			54F $T_A, V_{CC} =$ Mil		74F $T_A, V_{CC} =$ Com		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW A_n to LE	5.0 5.0			5.0 5.0		5.0 5.0		ns	3-15
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW A_n to LE	6.0 6.0			6.0 6.0		6.0 6.0			
$t_w(H)$	LE Pulse Width, HIGH	6.0			6.0		6.0		ns	3-7

54F/74F548

Octal Decoder/Demultiplexer With Acknowledge

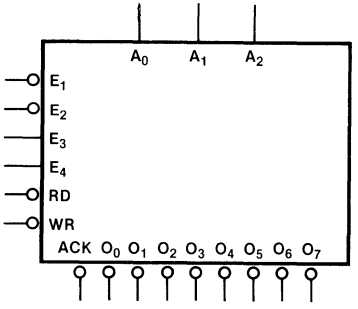
Description

The 'F548 is a 3-to-8 line address decoder with four Enable inputs. Two of the Enables are Active LOW and two are Active HIGH for maximum addressing versatility. Also provided is an Active LOW Acknowledge output that responds to either a Read or Write input signal when the Enables are active.

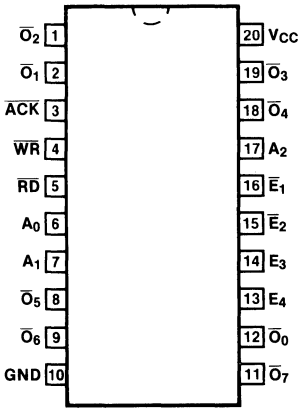
- **3-to-8 Line Address Decoder**
- **Multiple Enables for Address Extension**
- **Open Collector Acknowledge Output**
- **Active LOW Decoder Outputs**

Ordering Code: See Section 5

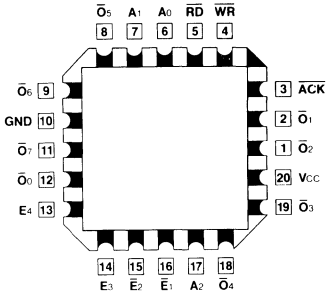
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



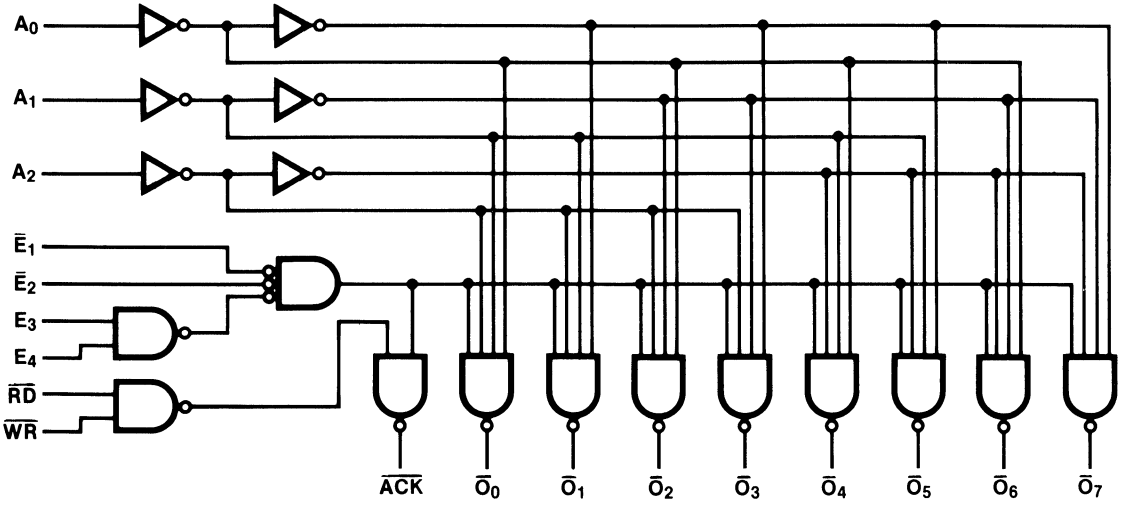
Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
A_0-A_2	Output Select Address Inputs	0.5/0.375
$\overline{E}_1$, $\overline{E}_2$	Chip Enable Inputs (Active LOW)	0.5/0.375
E_3, E_4	Chip Enable Inputs	0.5/0.375
$\overline{RD}$	Read Acknowledge Input (Active LOW)	0.5/0.375
$\overline{WR}$	Write Acknowledge Input (Active LOW)	0.5/0.375
$\overline{ACK}$	Open Collector Acknowledge Output (Active LOW)	OC*/12.5
$\overline{O}_0$-$\overline{O}_7$	Decoded Outputs (Active LOW)	25/12.5

*OC = Open Collector

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Functional Description

When enabled, the 'F548 accepts the A_0-A_2 Address inputs and decodes them to select one of eight active LOW, mutually exclusive outputs, as shown in the Decoder Truth Table. When one or more Enables is inactive, all decoder outputs are HIGH. Thus, the 'F548 can be used as a demultiplexer by applying data to one of the Enables.

The open collector Acknowledge ($\overline{ACK}$) output is normally HIGH (i.e. OFF) and goes LOW when the Enables are all active and either the Read ($\overline{RD}$) or Write ($\overline{WR}$) input is LOW, as indicated in the Acknowledge Truth Table.

Acknowledge Truth Table

Inputs						Output
$\overline{E_1}$	$\overline{E_2}$	E_3	E_4	$\overline{RD}$	$\overline{WR}$	$\overline{ACK}$
H	X	X	X	X	X	H
X	H	X	X	X	X	H
X	X	L	X	X	X	H
X	X	X	L	X	X	H
L	L	H	H	H	H	H
L	L	H	H	L	X	L
L	L	H	H	X	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Decoder Truth Table

Inputs							Outputs							
$\overline{E_1}$	$\overline{E_2}$	E_3	E_4	A_2	A_1	A_0	$\overline{O_0}$	$\overline{O_1}$	$\overline{O_2}$	$\overline{O_3}$	$\overline{O_4}$	$\overline{O_5}$	$\overline{O_6}$	$\overline{O_7}$
H	X	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	X	H	H	H	H	H	H	H	H
X	X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	H	L	H	H	H	H	H	H
L	L	H	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	L	H	H	H	H
L	L	H	H	H	L	L	H	H	H	H	L	H	H	H
L	L	H	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	H	H	H	L	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	L

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		14	21	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n to $\overline{O}_n$	3.0 4.0	5.5 8.0	7.5 10.5	3.0 4.0	10.0 12.0	3.0 4.0	8.5 11.5	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$	3.0 3.5	6.5 6.5	8.5 8.5	3.0 3.5	10.0 10.0	3.0 3.5	9.5 9.5	ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay E_3 or E_4 to $\overline{O}_n$	5.0 4.0	8.5 8.5	11.0 11.0	5.0 4.0	13.0 12.5	5.0 4.0	12.0 12.0	ns	3-1 3-3
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{ACK}$	6.5 3.0	11.0 7.5	14.0 9.5	6.5 3.0	16.5 11.0	6.5 3.0	15.0 10.5	ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay E_3 or E_4 to $\overline{ACK}$	8.0 4.0	13.0 8.5	16.5 11.0	8.0 4.0	19.5 13.0	8.0 4.0	17.5 12.5	ns	3-1 3-3
t_{PLH} t_{PHL}	Propagation Delay $\overline{RD}$ or $\overline{WR}$ to $\overline{ACK}$	5.5 2.5	10.0 5.0	12.5 6.5	5.5 2.5	16.5 8.5	5.5 2.5	13.5 7.5	ns	3-1 3-4

54F/74F550 • 54F/74F551

Octal Registered Transceiver With Status Flags

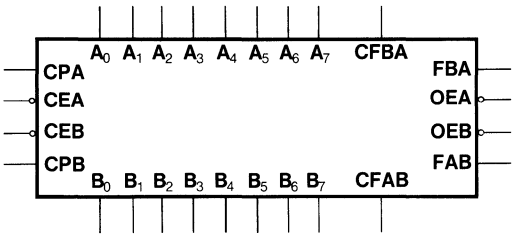
Description

The 'F550 and 'F551 octal transceivers each contain two 8-bit registers for temporary storage of data flowing in either direction. Each register has its own clock pulse and clock enable inputs, as well as a flag flip-flop that is set automatically as the register is loaded. Each flag flip-flop is provided with a clear input, and each register has a separate output enable control for its 3-state buffers. The separate clocks, flags and enables provide considerable flexibility as I/O ports for demand-response data transfer. The 'F550 is non-inverting; the 'F551 inverts data in both directions.

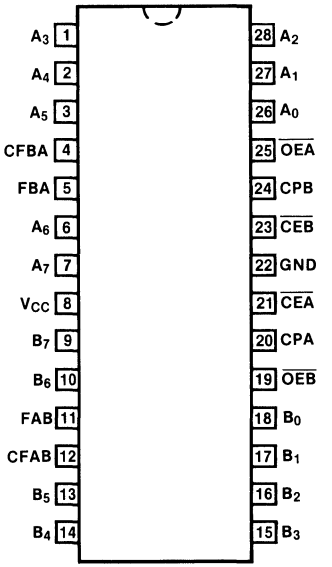
- **8-Bit Bidirectional I/O Port with Handshake**
- **Back-to-Back Registers for Storage**
- **Register Status Flag Flip-Flops**
- **Separate Edge-Detecting Clears for Flags**
- **Inverting and Non-Inverting Versions**
- **B Outputs Sink 64 mA**

Ordering Code: See Section 5

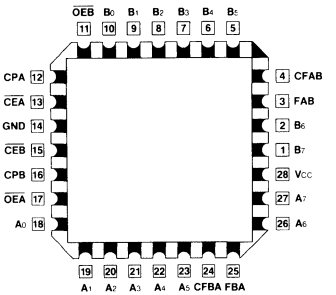
Logic Symbol



Connection Diagrams ('F550 shown*)



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

*'F551 has inverting outputs

Input Loading/Fan-Out: See Section 3 for U.L. definitions

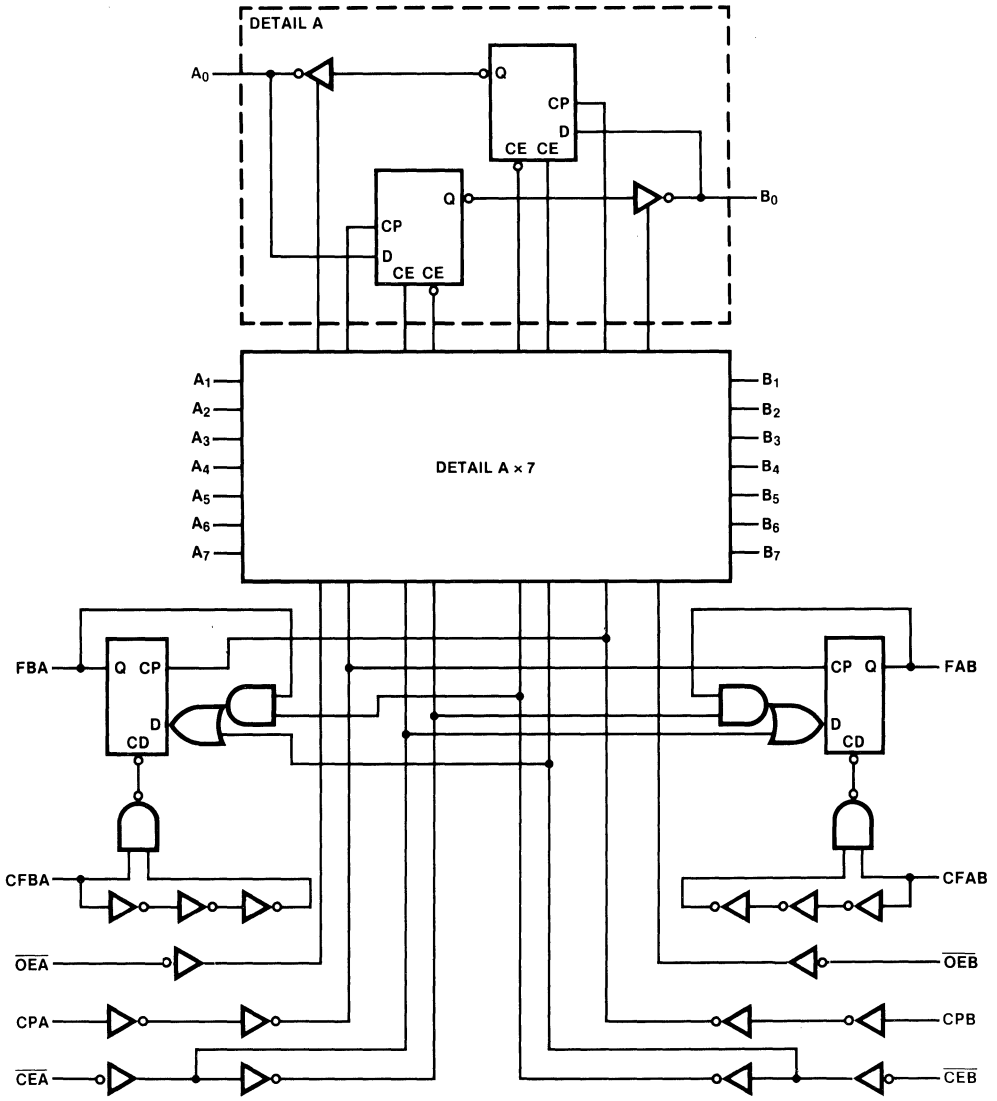
Pin Names	Description	54F/74F(U.L.) HIGH/LOW
CPA	A-to-B Clock Pulse Input (Active Rising Edge)	0.5/0.375
CPB	B-to-A Clock Pulse Input (Active Rising Edge)	0.5/0.375
$\overline{CEA}$	A-to-B Clock Enable Input (Active LOW)	0.5/0.375
$\overline{CEB}$	B-to-A Clock Enable Input (Active LOW)	0.5/0.375
$\overline{OEA}$	A Output Enable Input (Active LOW)	0.5/0.375
$\overline{OEB}$	B Output Enable Input (Active LOW)	0.5/0.375
CFAB	A-to-B Flag Clear Input (Active Rising Edge)	0.5/0.5
CFBA	B-to-A Flag Clear Input (Active Rising Edge)	0.5/0.5
A_0-A_7	A-to-B Data Inputs or	1.75/0.406
	3-State B-to-A Outputs	75/15 (12.5)
B_0-B_7	B-to-A Data Inputs or	1.75/0.406
	3-State B-to-A Outputs	75/40 (30)
FAB	A-to-B Status Flag Output (Active HIGH)	25/12.5
FBA	B-to-A Status Flag Output (Active HIGH)	25/12.5

Functional Description

Data applied to the A inputs is entered and stored on the rising edge of the A Clock Pulse (CPA), provided that the A Clock Enable ($\overline{CEA}$) is LOW; simultaneously, the status flip-flop is set and the A-to-B flag (FAB) output goes HIGH. Data thus entered from the A inputs is present at the inputs to the B output buffers, but only appears on the B I/O pins when the B Output Enable ($\overline{OEB}$) signal is made LOW. After the B output data is assimilated, the receiving system clears the A-to-B flag flip-flop by applying a LOW-to-HIGH transition to the CFAB input. Optionally, the $\overline{OEA}$ and CFAB pins can be tied together and operated by one function from the receiving system.

Data flow from B-to-A proceeds in the same manner described for A-to-B flow. Inputs $\overline{CEB}$ and CPB enter the B input data and set the B-to-A flag (FBA) output HIGH. A LOW signal on $\overline{OEA}$ enables the A output buffers and a LOW-to-HIGH transition on CFBA clears the FBA flag.

Logic Diagram ('F550 shown)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		130	190	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay CPA, CPB to B_n, A_n	3.0 4.0	5.5 7.0	7.5 9.0			2.5 3.5	8.5 10.0	ns	3-1 3-7
t_{PLH}	Propagation Delay CPA, CPB to FBA	3.5	6.0	8.0			3.0	9.0	ns	3-1 3-7
t_{PHL}	Propagation Delay CFAB, CFBA to FAB, FBA	5.0	9.0	11.5			4.5	13.0	ns	3-1 3-11
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEA}$ or $\overline{OEB}$ to A_n or B_n	2.5 3.5	5.5 7.0	7.5 9.5			2.0 3.0	8.5 10.5	ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEA}$ or $\overline{OEB}$ to A_n or B_n	3.0 2.5	6.5 5.5	9.0 7.5			2.5 2.0	10.0 8.5		

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW A_n, B_n to CPA, CPB	4.0 4.0		4.5 4.5	ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW A_n, B_n to CPA, CPB	2.0 2.0		2.5 2.5		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{CEA}$, $\overline{CEB}$ to CPA, CPB	4.0 4.0		4.5 4.5	ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{CEA}$, $\overline{CEB}$ to CPA, CPB	2.0 2.0		2.5 2.5		
$t_w(H)$ $t_w(L)$	Pulse Width, HIGH or LOW CPA or CPB	3.0 3.0		3.5 3.5	ns	3-7
$t_w(H)$	Pulse Width, HIGH CFAB or CFBA	3.0		3.5	ns	3-11
t_{rec}	Recovery Time CFAB, CFBA to CPA, CPB	9.0		10.0	ns	3-11

4

54F/74F552

Octal Registered Transceiver With Parity and Flags

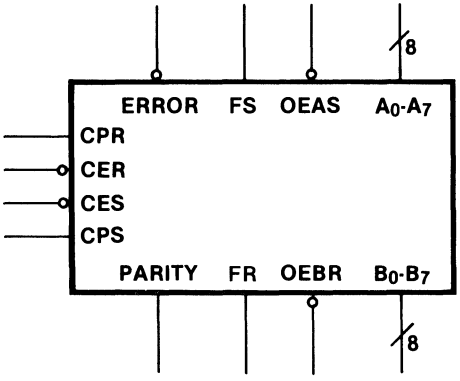
Description

The 'F552 octal transceiver contains two 8-bit registers for temporary storage of data flowing in either direction. Each register has its own clock pulse and clock enable input as well as a flag flip-flop that is set automatically as the register is loaded. The flag output will be reset when the output enable returns to HIGH after reading the output port. Each register has a separate output enable control for its 3-state buffer. The separate Clocks, Flags, and Enables provide considerable flexibility as I/O ports for demand-response data transfer. When data are transferred from the A-port to the B-port, a parity bit is generated. On the other hand, when data are transferred from the B-port to the A-port, the parity of input data on B_0-B_7 is checked.

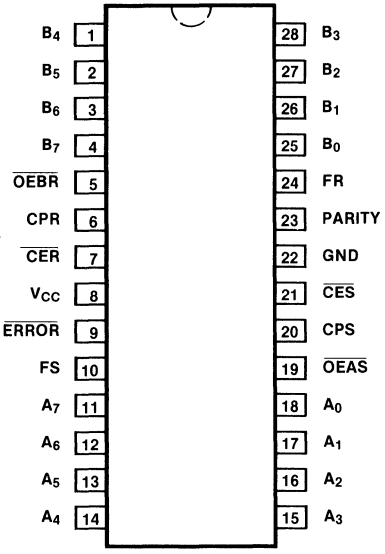
- **8-Bit Bidirectional I/O Port with Handshake**
- **Register Status Flag Flip-Flops**
- **Separate Clock Enable and Output Enable**
- **Parity Generation and Parity Check**
- **B-Outputs Sink 64 mA**

Ordering Code: See Section 5

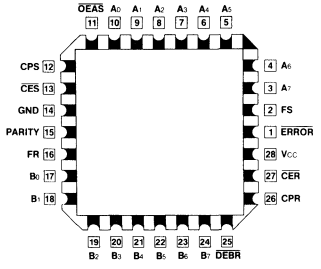
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
A_0-A_7	A Port Data Transceiver Input	1.75/0.406
	Output	75/15 (12.5)
B_0-B_7	B Port Data Transceiver Input	1.75/0.406
	Output	75/40 (30)
FR	B Port Flag Output	25/12.5
FS	A Port Flag Output	25/12.5
PARITY	Parity Bit Transceiver Input	1.75/0.406
	Output	75/40 (30)
$\overline{ERROR}$	Parity Check Output (Active LOW)	25/12.5
$\overline{CER}$	R Registers Clock Enable Input (Active LOW)	0.5/0.375
$\overline{CES}$	S Registers Clock Enable Input (Active LOW)	0.5/0.375
CPR	R Registers Clock Pulse Input (Active Rising Edge)	0.5/0.375
CPS	S Registers Clock Pulse Input (Active Rising Edge)	0.5/0.375
$\overline{OEBR}$	B Port and PARITY Output Enable (Active LOW) and Clear FR input (Active Rising Edge)	0.5/0.75
$\overline{OEAS}$	A Port Output Enable (Active LOW) and Clear FS input (Active Rising Edge)	0.5/0.75

4

Functional Description

Data applied to the A-inputs are entered and stored in the R register on the rising edge of the CPR Clock Pulse, provided that the Clock Enable ($\overline{CER}$) is LOW; simultaneously, the status flip-flop is set and the flag (FR) output goes HIGH. As the Clock Enable ($\overline{CER}$) returns to HIGH, the data will be held in the R register. These data entered from the A-inputs will appear at the B-port I/O pins after the Output Enable ($\overline{OEBR}$) has gone LOW. When $\overline{OEBR}$ is LOW, a parity bit appears at the PARITY pin, which will be set HIGH when there is an even number of 1s or all 0s at the Q outputs of the R register. After the data are assimilated, the receiving system clears the flag FR by changing the signal at the $\overline{OEBR}$ pin from LOW to HIGH.

Data flow from B-to-A flow proceeds in the same manner described for A-to-B flow. A LOW at the $\overline{CES}$ pin and a LOW-to-HIGH transition at CPS pin enter the B-input data and the parity-input data into the S register and the parity register respectively and set the flag output FS to HIGH. A LOW signal at the $\overline{OEAS}$ pin enables the A-port I/O pins and a LOW-to-HIGH transition of the $\overline{OEAS}$ signal clears the FS flag. When $\overline{OEAS}$ is LOW, the parity check output $\overline{ERROR}$ will be HIGH if there is an odd number of 1s at the Q outputs of the S registers and the parity register. The flag FS can be cleared by a LOW-to-HIGH transition of the $\overline{OEAS}$ signal.

Register Function Table

(Applies to R or S Register)

Inputs			Internal Q	Function
D	CP	$\overline{CE}$		
X	X	H	NC	Hold Data
L	↑	L	L	Load Data
H	↑	L	H	
M	↓	L	NC	Keep Old Data

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↑ = LOW-to-HIGH Transition
↓ = Not LOW-to-HIGH Transition
NC = No Change

Output Control

$\overline{OE}$	Internal Q	A or B Outputs	Function
H	X	Z	Disable Output
L	L	L	Enable Output
L	H	H	

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Flag Flip-Flop Function Table
(Applies to R or S Flag Flip-Flop)

Inputs			Flag Output	Function
$\overline{CE}$	CP	$\overline{OE}$		
H	X	‡	NC	Hold Flag
L	↑	‡	H	Set Flag
X	X	‡	L	Clear Flag

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↑ = LOW-to-HIGH Transition
‡ = Not LOW-to-HIGH Transition
NC = No Change

Parity Generation Function

$\overline{OEBR}$	Number of HIGHs in the Q Outputs of the R Register	Parity Output
H	X	Z
L	0,2,4,6,8	H
L	1,3,5,7	L

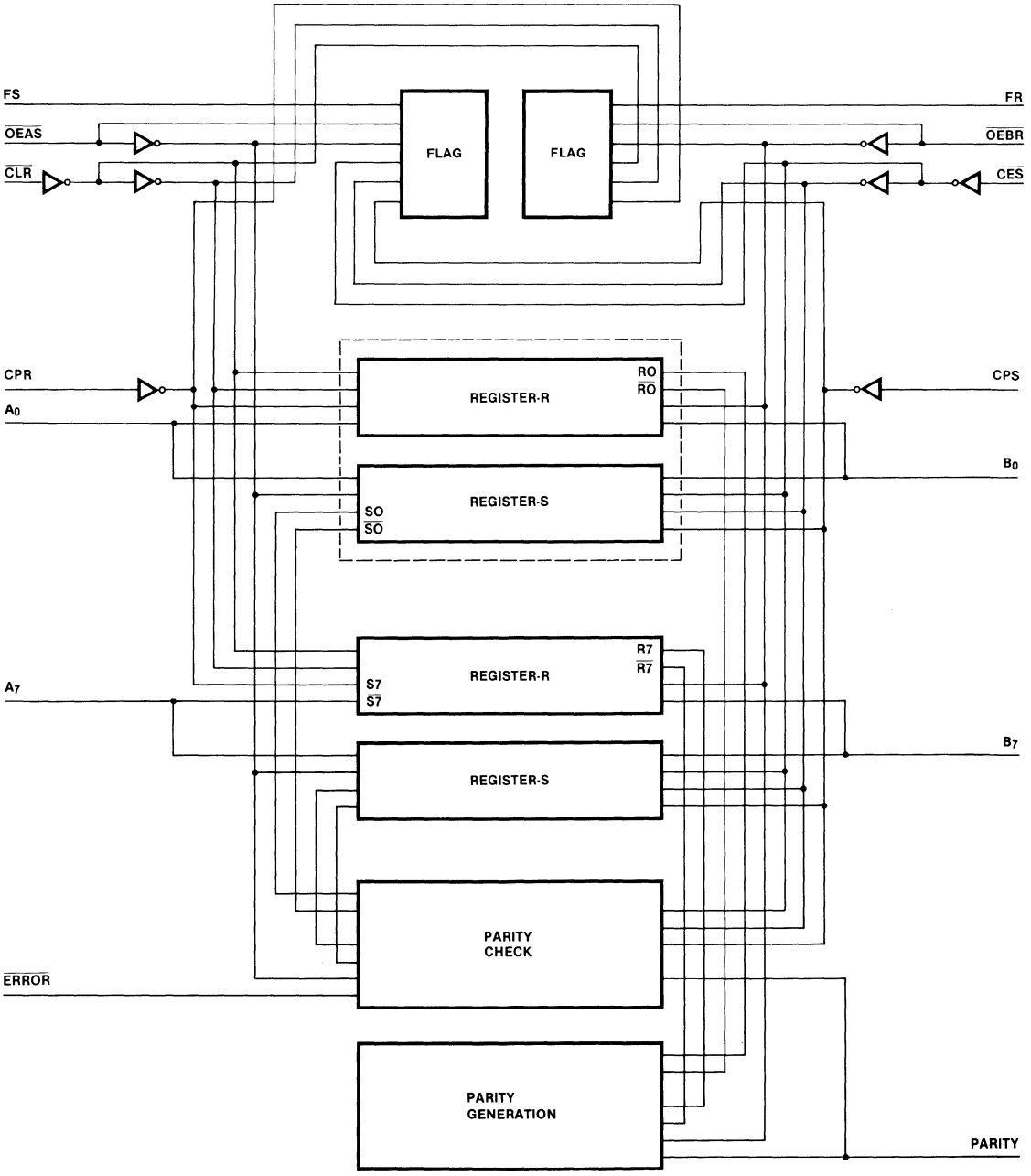
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Parity Check Function

$\overline{OEAS}$	Number of HIGHs in the Q Outputs of the S Register	Parity Input	$\overline{ERROR}$ Output
H	X	X	H
L	0,2,4,6,8	L	L
L	1,3,5,7	L	H
L	0,2,4,6,8	H	H
L	1,3,5,7	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Block Diagram



DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CCZ} I_{CCL} I_{CCH}	Power Supply Current		110 100 100	165 150 150	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			54F T_A, V_{CC} = Mil C_L = 50 pF		74F T_A, V_{CC} = Com C_L = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay CPS or CPR to A_n or B_n	3.5 4.0	6.0 7.0	8.0 9.5			3.0 3.5	9.0 10.5	ns	3-1 3-7
t_{PLH}	Propagation Delay CPS or CPR to FS or FR	3.0	5.5	7.5			2.5	8.5	ns	3-1 3-7
t_{PHL}	Propagation Delay $\overline{OEAS}$ to FS	3.5	6.0	8.0			3.0	9.0	ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay CPS to Parity	8.0 8.5	14.0 14.5	18.0 18.5			7.0 7.5	20.0 20.5	ns	3-1 3-11
t_{PLH} t_{PHL}	Propagation Delay CPR to $\overline{ERROR}$	8.0 7.5	13.5 13.0	17.5 16.5			7.0 6.5	19.5 18.5	ns	3-1 3-11
t_{PLH} t_{PHL}	Propagation Delay $\overline{OEAS}$ to $\overline{ERROR}$	3.5 3.0	6.0 5.0	8.0 7.0			3.0 2.5	9.0 8.0	ns	3-1 3-11
t_{PZH} t_{PZL}	Enable Time $\overline{OEAS}$ or $\overline{OEBR}$ to B_n or A_n	3.0 3.5	5.5 7.0	7.5 9.5			2.5 3.0	8.5 10.5	ns	3-1 3-12 3-3
t_{PHZ} t_{PLZ}	Disable Time $\overline{OEAS}$ or $\overline{OEBR}$ to B_n or A_n	3.0 3.0	6.5 5.5	8.5 7.5			2.5 2.5	9.5 8.5		
t_{PZH} t_{PZL}	Enable Time $\overline{OEBR}$ to Parity	2.5 3.5	4.5 6.0	6.0 8.0			2.0 3.0	7.0 9.0	ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Disable Time $\overline{OEBR}$ to Parity	3.5 3.0	5.5 6.5	7.0 8.5			2.5 2.5	8.0 9.5		

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW A_n or B_n or Parity to CPS or CPR	7.5 4.5		8.5 5.0	ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW A_n or B_n or Parity to CPS or CPR	0 0		0 0		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{CES}$ or $\overline{CER}$ to CPS or CPR	6.0 10.0		7.0 11.5	ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{CES}$ or $\overline{CER}$ to CPS or CPR	0 0		0 0		
$t_w(H)$ $t_w(L)$	Pulse Width, HIGH or LOW CPS or CPR	4.0 6.0		4.5 7.0	ns	3-7

4

54F/74F557 • 54F/74F558

8-Bit By 8-Bit Multipliers With 3-State Outputs

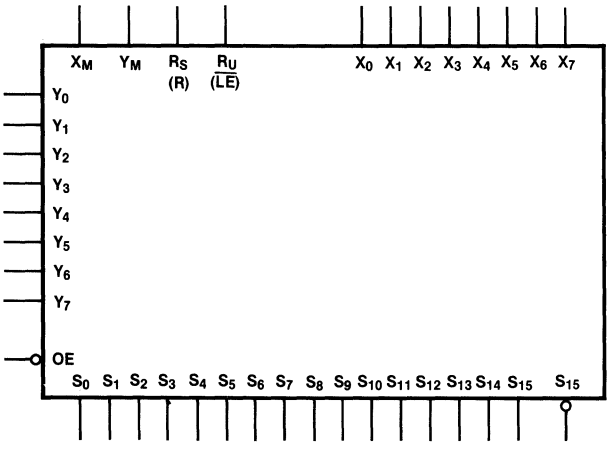
Description

The 'F557 and 'F558 are high-speed combinatorial arrays that multiply two 8-bit unsigned or signed twos complement numbers and provide the 16-bit unsigned or signed product. Each input operand X and Y has a mode control input that determines whether the number is treated as signed or unsigned. Additional inputs, R_S and R_U for the 'F558 or R for the 'F557, allow the addition of a bit for rounding to the best signed or unsigned fractional 8-bit result. For expansion during signed or mixed multiplication, both the true and complement outputs of the most significant bit are available. The 'F557 has output latches that store the results when $\overline{LE}$ is HIGH. Both devices have 3-state outputs for bus applications.

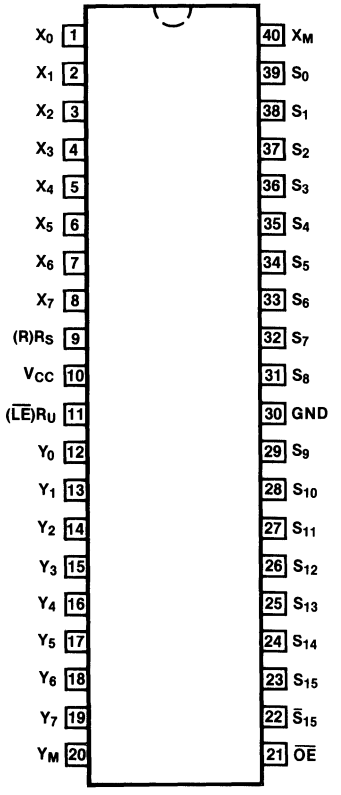
- **Unsigned, Signed or Mixed Multiplication**
- **Full 16-Bit Product Outputs**
- **MSB Complement Output for Signed Expansion**
- **Rounding Inputs for Fractional 8-Bit Product**

Ordering Code: See Section 5

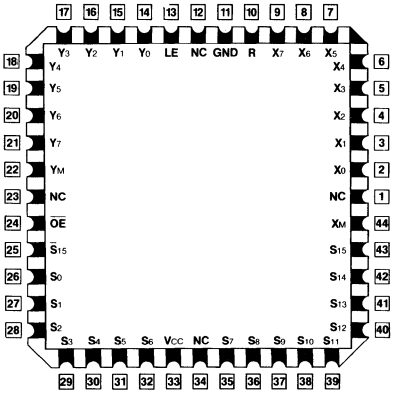
Logic Symbol



Connection Diagrams



Pin Assignment for DIP



Pin Assignment for LCC and PCC

Pin assignments shown are for 'F558. $\overline{LE}$ and R shown in parentheses are pin assignments for 'F557.

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
X_0-X_7	Multiplicand Inputs	0.5/0.5
Y_0-Y_7	Multiplier Inputs	0.5/0.5
X_M	Multiplicand Sign Control Input	0.5/0.5
Y_M	Multiplier Sign Control Input	0.5/0.5
R	Rounding Input ('F557)	0.5/0.5
R_S	Signed Number Rounding Input ('F558)	0.5/0.5
R_U	Unsigned Number Rounding Input ('F558)	0.5/0.5
$\overline{LE}$	Latch Enable Input (Active LOW) ('F557)	0.5/0.5
$\overline{OE}$	3-State Output Enable Input (Active LOW)	0.5/0.5
S_0-S_{15}	Product Outputs	50/12.5
$\overline{S}_{15}$	MSB Complement Output	50/12.5

Functional Description

The 'F557 and 'F558 multipliers are 8x8 combinatorial logic arrays capable of multiplying numbers in unsigned, signed twos complement or mixed notation. Each 8-bit input operand X and Y has an associated mode control which determines whether the array treats the number as signed or unsigned. If the mode control X_M or Y_M is HIGH, the operand is treated as a twos complement number with the most significant bit having a negative weight; if the mode control is LOW, the operand is treated as an unsigned number.

The multipliers provide all sixteen product bits generated by the multiplication. For expansion during signed or mixed multiplication, the most significant product bit has both true and complement available. Therefore, an adder may be used as a subtractor in many applications and the need for SSI circuits is eliminated.

The 'F557 has latches that store the product for pipelined operations. When $\overline{LE}$ is HIGH the latches are transparent and their outputs change with their inputs. When $\overline{LE}$ is LOW the latches are in the storage mode and new data cannot enter.

The 3-state output buffers are controlled by the active LOW Output Enable $\overline{OE}$ input. When $\overline{OE}$ is LOW, the outputs are active; when $\overline{OE}$ is HIGH, the outputs are in a high impedance (High Z) state. Several multipliers can be connected on a common bus or used in a pipeline system for multiplications in higher speed systems.

Rounding

The 16-bit product can be truncated to eight bits by using the rounding input(s) to add one in either the 2^7 adder for unsigned numbers or in the 2^6 adder for signed numbers. The 'F558 has separate rounding inputs R_S and R_U for signed or unsigned numbers, respectively. The 'F557 has a single rounding input R and develops the proper rounding by internally combining R with X_M and Y_M as follows:

$R_U = \overline{X}_M \bullet \overline{Y}_M \bullet R$ = unsigned rounding input to 2^7 adder

$R_S = (X_M \pm Y_M)R$ = signed rounding input to 2^6 adder

Rounding input levels and results for the various modes are shown in Tables 1 and 2. Figure a shows how R_S and R_U would normally be used for rounding signed and unsigned fractional multipliers.

Signed Expansion

The most significant product bit has both true and complement outputs available. When building larger signed multipliers the partial products, except at the lower stages, are signed numbers. These unsigned and signed partial products must be added to give the correct signed product. For example, to obtain the correct signed product when using MSI adders, the carry from the previous adder stage must be added to the sum of the two negative most significant partial product bits. The result of this addition must be a positive sum and a negative carry (borrow). The equations are:

$$S = A + B + C$$
$$C_0 = A \bullet B + B \bullet \overline{C} + \overline{C} \bullet A$$

where C is the Carry In and A and B the sign bits of the two partial products.

An adder produces the equations:

$$S = A + B + C$$
$$C_0 = A \bullet B + B \bullet C + C \bullet A$$

Therefore, if the inversion of A and B is used, then the adder produces the inversion of the negative carry since

$$A \bullet B + B \bullet \overline{C} + \overline{C} \bullet A = \overline{\overline{A} \bullet \overline{B} + \overline{B} \bullet C + \overline{A} \bullet C}$$

and the sum remains the same.

Table 1 'F557 Rounding Inputs

Inputs			Adds	
X_M	Y_M	R	2^7	2^6
L	L	H	Yes	No
L	H	H	No	Yes
H	L	H	No	Yes
H	H	H	No	Yes
X	X	L	No	No

Table 2 'F558 Rounding Inputs

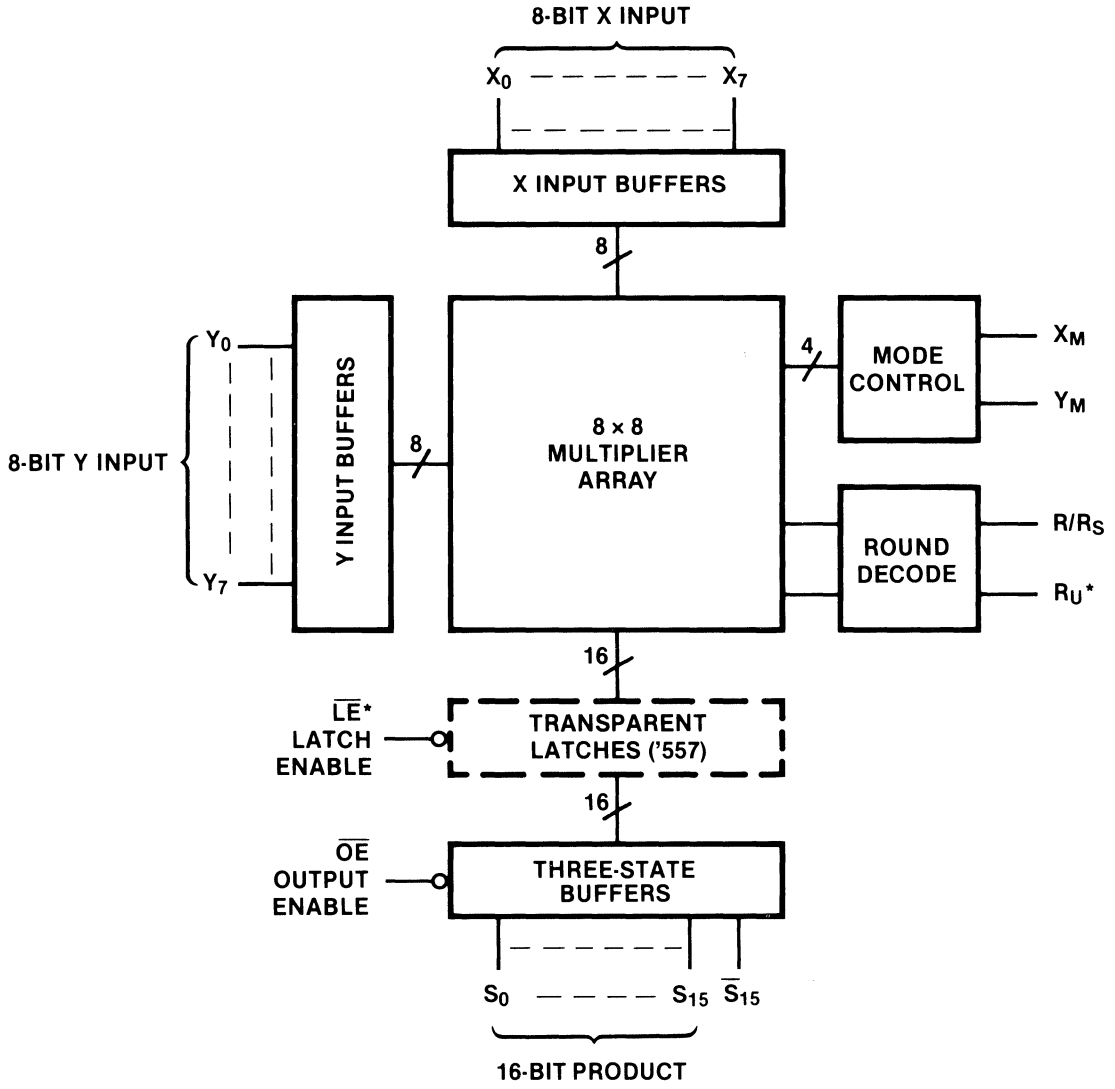
Inputs		Adds		Normally Used With	
R_U	R_S	2^7	2^6	X_M	Y_M
L	L	No	No	X	X
L	H	No	Yes	$X_M + Y_M = H$	
H	L	Yes	No	L	L
H	H	Yes	Yes	*	*

*Most rounding applications require a HIGH level for R_U or R_S, but not both.
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Mode Select Table

Operating Mode	Input Data		Mode Control Inputs	
	X_0-X_7	Y_0-Y_7	X_M	Y_M
Unsigned	Unsigned	Unsigned	L	L
Mixed	Unsigned	Twos Complement	L	H
	Twos Complement	Unsigned	H	L
Signed	Twos Complement	Twos Complement	H	H

Block Diagram



$\overline{LE}$ for 'F557 and R_U for 'F558.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		200	280	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay X_n or Y_n to S_n, $\overline{S}_{15}$			70.0 70.0					ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay $\overline{LE}$ to S_n, $\overline{S}_{15}$ ('F557)			20.0 2.0					ns	3-1 3-8
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to S_n or $\overline{S}_{15}$			14.0 14.0					ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to S_n or $\overline{S}_{15}$			21.0 14.0						

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
t_s(H) t_s(L)	Setup Time, HIGH or LOW X_n or Y_n to $\overline{LE}$	65.0 65.0							ns	3-14
t_h(H) t_h(L)	Hold Time, HIGH or LOW X_n or Y_n to $\overline{LE}$	0 0								
t_w(L)	$\overline{LE}$ Pulse Width, LOW	10.0							ns	3-8

Applications

16x16 Twos Complement Multiplier

The 'F558 8x8 multiplier can be used with standard MSI adder circuits to build larger multipliers. Figure b illustrates the use of four 'F558 multipliers and ten 16-pin 4-bit 'F283 adders to form a 16x16-bit twos complement multiplier with a typical multiplication time of 90 ns. The 16-bit operands are split up into 8-bit sections:

$$X \bullet Y = (X_{0\text{-}7} + X_{8\text{-}15}2^8) \bullet (Y_{0\text{-}7} + Y_{8\text{-}15}2^8)$$
$$= X_{0\text{-}7} \bullet Y_{0\text{-}7} + 2^8(X_{0\text{-}7} \bullet Y_{8\text{-}15} + X_{8\text{-}15} \bullet Y_{0\text{-}7})$$
$$= + 2^{16}(X_{8\text{-}15} \bullet Y_{8\text{-}15})$$

Since X_8-X_{15} and Y_8-Y_{15} are signed numbers, the most significant bit of all the partial products (except the first) carries a negative weight. Therefore, at these negative bit positions the partial product bits must be subtracted rather than added. This subtraction is done in the middle of the network at the 2^{15} bit position by using the inverted output of the most significant product bits from the multipliers to obtain a borrow signal from the last sum output of the appropriate 'F283. This borrow is then used to either add zero or minus 1 to the remaining 8-bit adder section. The mode control inputs of the four 'F558 devices are tied to the logic levels required to produce the correctly signed partial products. Rounding to the best 16-bit fractional product is made by tying the R_S input of one of the middle multipliers to V_{CC}. Appropriate connection of the adders and mode control logic levels will yield 16x16 unsigned multiplication.

4

Fig. a Rounded Products

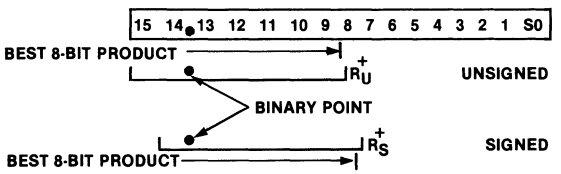
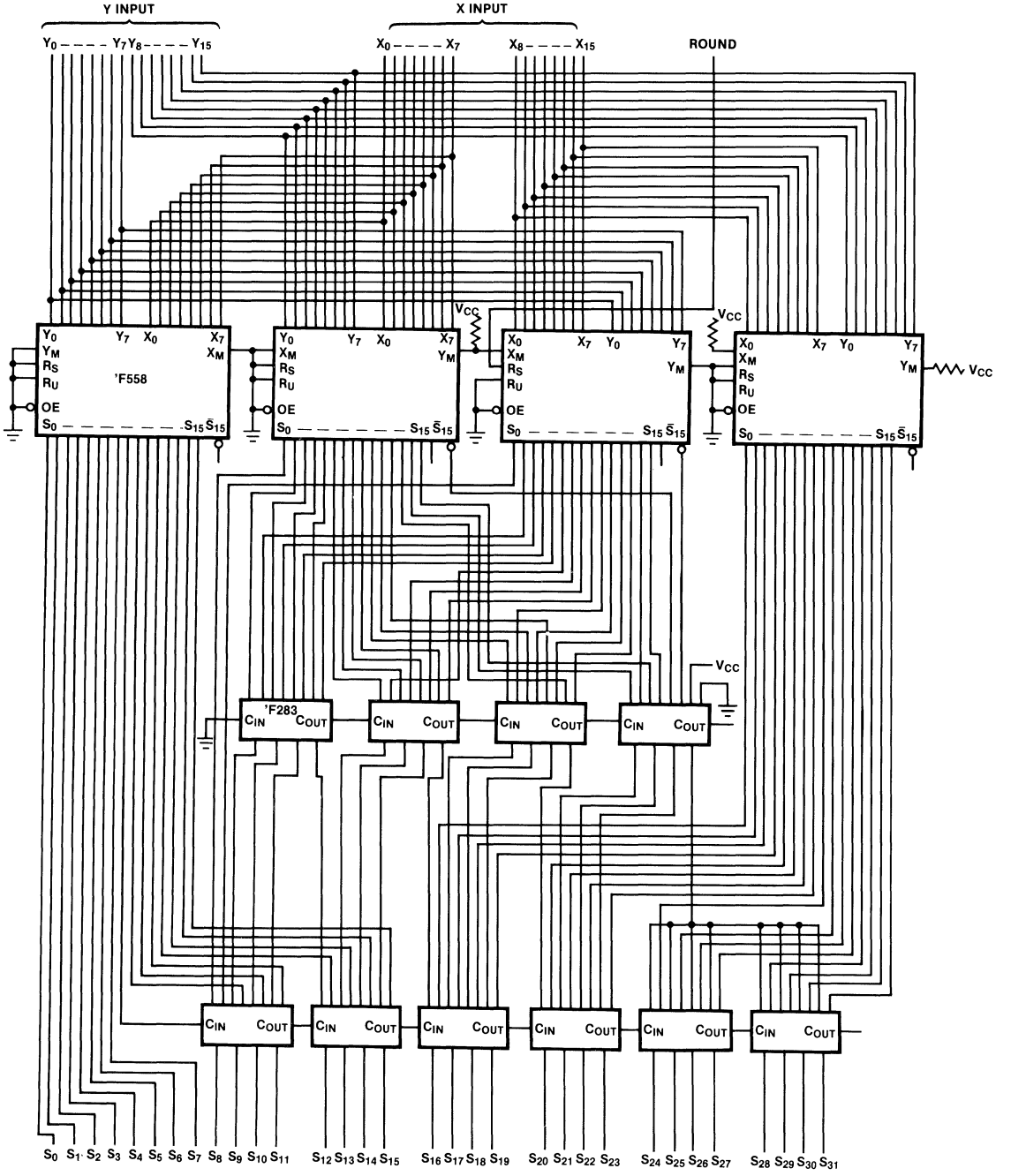
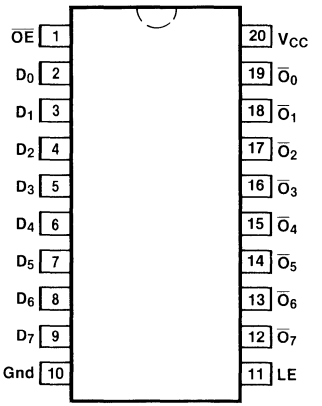


Fig. b High-Speed 16x16 Twos Complement Multiplication



54F/74F563

Octal D-Type Latch
With 3-State Outputs



Pin Assignment for DIP and SOIC

Description

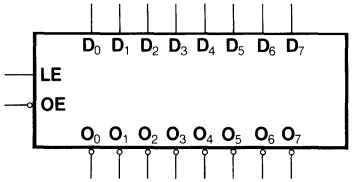
The 'F563 is a high speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ($\overline{OE}$) inputs.

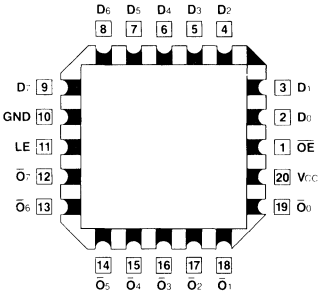
This device is functionally identical to the 'F573, but has inverted outputs.

- **Inputs and Outputs on Opposite Sides of Package Allowing Easy Interface with Microprocessors**
- **Useful as Input or Output Port for Microprocessors**
- **Functionally Identical to 'F573**

Ordering Code: See Section 5

Logic Symbol





Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
D_0-D_7	Data Inputs	0.5/0.375
LE	Latch Enable Input (Active HIGH)	0.5/0.375
$\overline{OE}$	3-State Output Enable Input (Active LOW)	0.5/0.375
$\overline{O_0}$-$\overline{O_7}$	3-State Latch Outputs	75/15 (12.5)

Functional Description

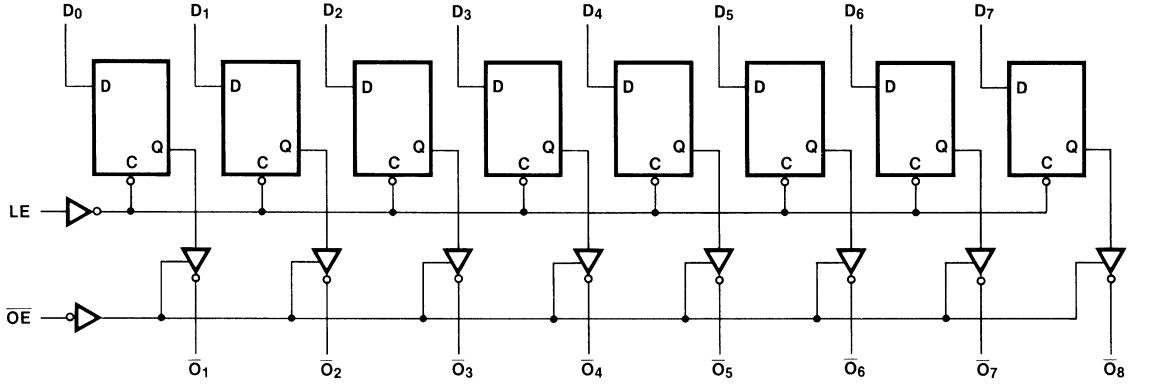
The 'F563 contains eight D-type latches with 3-state output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-state buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are in the bi-state mode. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Function Table

Inputs			Internal	Output	Function
$\overline{OE}$	LE	D	Q	O	
H	X	X	X	Z	High Z
H	H	L	H	Z	High Z
H	H	H	L	Z	High Z
H	L	X	NC	Z	Latched
L	H	L	H	H	Transparent
L	H	H	L	L	Transparent
L	L	X	NC	NC	Latched

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
NC = No Change

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		35	55	mA	V_{CC} = Max, $\overline{OE}$ = HIGH D_n, LE = Gnd (All outputs OFF)

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			54F T_A, V_{CC} = Mil C_L = 50 pF		74F T_A, V_{CC} = Com C_L = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to $\overline{O}_n$	4.0 3.0	6.9 5.2	9.0 7.0			3.5 2.5	10.0 8.0	ns	3-1 3-3
t_{PLH} t_{PHL}	Propagation Delay LE to $\overline{O}_n$	5.0 3.0	8.5 5.6	11.0 7.0			4.5 2.5	12.5 8.0	ns	3-1 3-7
t_{PZH} t_{PZL}	Output Enable Time	2.0 2.0	7.7 5.1	10.0 6.5			1.5 1.5	11.5 7.5	ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time	2.0 2.0	4.7 4.1	6.0 5.5			1.5 1.5	7.0 6.5		

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F T_A = +25°C V_{CC} = +5.0 V			54F T_A, V_{CC} = Mil		74F T_A, V_{CC} = Com		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_s(H) t_s(L)	Setup Time, HIGH or LOW D_n to LE	2.0 2.0					2.5 2.5		ns	3-5
t_h(H) t_h(L)	Hold Time, HIGH or LOW D_n to LE	3.0 3.0					3.5 3.5		ns	3-5
t_w(H)	LE Pulse Width, HIGH	6.0					7.0		ns	3-7

54F/74F564

Octal D-Type Flip-Flop With 3-State Outputs

Description

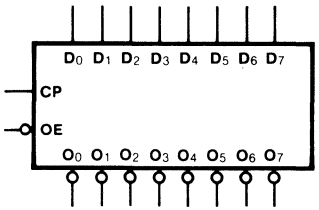
The 'F564 is a high speed low power octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable ($\overline{OE}$). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

This device is functionally identical to the 'F574, but has inverted outputs.

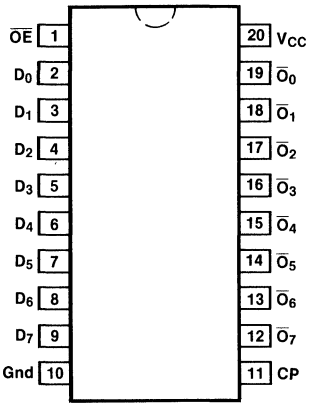
- **Inputs and Outputs on Opposite Sides of Package Allowing Easy Interface with Microprocessors**
- **Useful as Input or Output Port for Microprocessors**
- **Functionally Identical to 'F574**
- **3-State Outputs for Bus-Oriented Applications**

Ordering Code: See Section 5

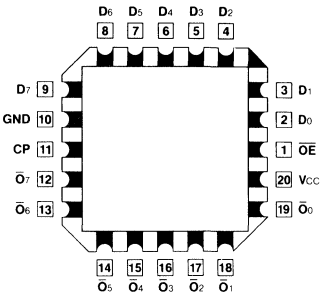
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
D_0-D_7	Data Inputs	0.5/0.375
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
$\overline{OE}$	3-State Output Enable Input (Active LOW)	0.5/0.375
$\overline{O_0}$-$\overline{O_7}$	3-State Outputs	75/15 (12.5)

Functional Description

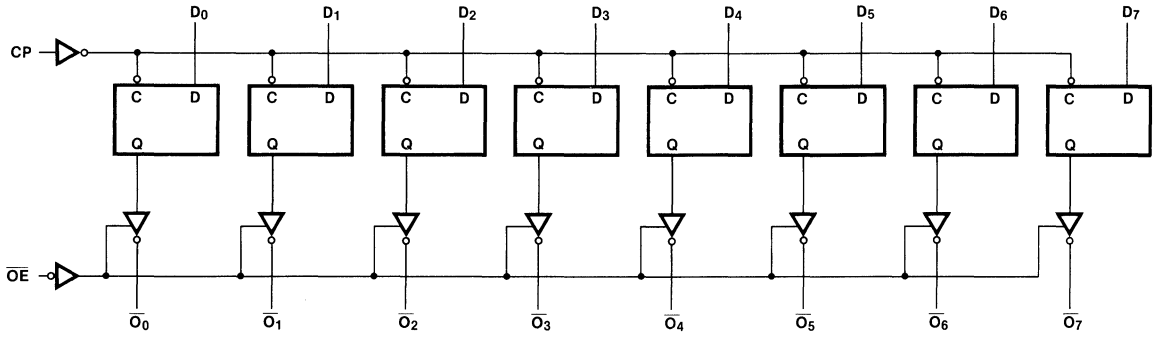
The 'F564 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-state true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Function Table

Inputs			Internal	Outputs	Function
$\overline{OE}$	CP	D	Q	O	
H	H	L	NC	Z	Hold
H	H	H	NC	Z	Hold
H	↑	L	H	Z	Load
H	↑	H	L	Z	Load
L	↑	L	H	H	Data Available
L	↑	H	L	L	Data Available
L	H	L	NC	NC	No Change in Data
L	H	H	NC	NC	No Change in Data

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
↑ = LOW-to-HIGH Transition
NC = No Change

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		55	86	mA	V_{CC} = Max, D_n = Gnd, $\overline{OE}$ = HIGH

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$	T_A, V_{CC} = Mil $C_L = 50\ pF$	T_A, V_{CC} = Com $C_L = 50\ pF$		
		Min Typ Max	Min Max	Min Max		
f_{max}	Maximum Clock Frequency	100			MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{O}_n$	7.5 9.5			ns	3-1 3-7
t_{PZH} t_{PZL}	Output Enable Time	11.5 7.5			ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time	7.0 5.5				

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW D_n to CP	2.0 2.0			ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D_n to CP	2.0 2.0				
$t_w(H)$ $t_w(L)$	CP Pulse Width HIGH or LOW	5.0 5.0			ns	3-7

54F/74F568 • 54F/74F569

4-Bit Bidirectional Counters With 3-State Outputs

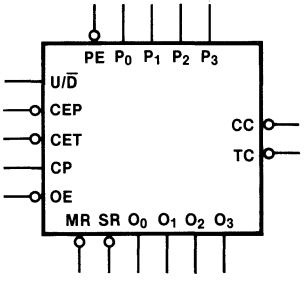
Description

The 'F568 and 'F569 are fully synchronous, reversible counters with 3-state outputs. The 'F568 is a BCD decade counter; the 'F569 is a binary counter. They feature preset capability for programmable operation, carry lookahead for easy cascading, and a U/$\overline{D}$ input to control the direction of counting. For maximum flexibility there are both synchronous and master asynchronous reset inputs as well as both Clocked Carry ($\overline{CC}$) and Terminal Count ($\overline{TC}$) outputs. All state changes except Master Reset are initiated by the rising edge of the clock. A HIGH signal on the Output Enable ($\overline{OE}$) input forces the output buffers into the high impedance state but does not prevent counting, resetting or parallel loading.

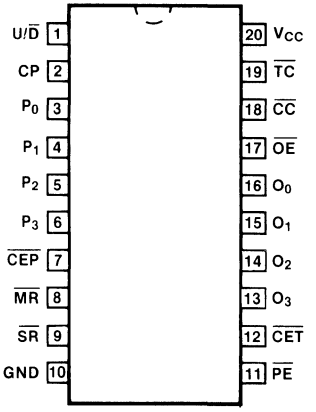
- **Synchronous Counting and Loading**
- **Lookahead Carry Capability for Easy Cascading**
- **Preset Capability for Programmable Operation**
- **3-State Outputs for Bus Organized Systems**

Ordering Code: See Section 5

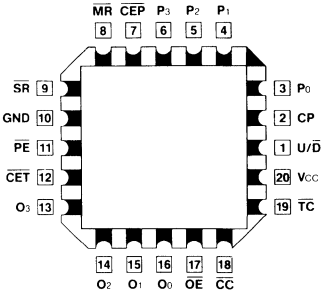
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
P_0-P_3	Parallel Data Inputs	0.5/0.375
$\overline{CEP}$	Count Enable Parallel Input (Active LOW)	0.5/0.375
$\overline{CET}$	Count Enable Trickle Input (Active LOW)	0.5/0.75
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
$\overline{PE}$	Parallel Enable Input (Active LOW)	0.5/0.75
U/$\overline{D}$	Up/Down Count Control Input	0.5/0.375
$\overline{OE}$	Output Enable Input (Active LOW)	0.5/0.375
$\overline{MR}$	Master Reset Input (Active LOW)	0.5/0.375
$\overline{SR}$	Synchronous Reset Input (Active LOW)	0.5/0.375
O_0-O_3	3-State Parallel Data Outputs	75/25 (12.5)
$\overline{TC}$	Terminal Count Output (Active LOW)	25/12.5
$\overline{CC}$	Clocked Carry Output (Active LOW)	25/12.5

Functional Description

The 'F568 counts modulo-10 in the BCD (8421) sequence. From state 9 (HLLH) it will increment to 0 (LLLL) in the Up mode; in Down mode it will decrement from 0 to 9. The 'F569 counts in the modulo-16 binary sequence. From state 15 it will increment to state 0 in the Up mode; in the Down mode it will decrement from 0 to 15. The clock inputs of all flip-flops are driven in parallel through a clock buffer. All state changes (except due to Master Reset) occur synchronously with the LOW-to-HIGH transition of the Clock Pulse (CP) input signal.

The circuits have five fundamental modes of operation, in order of precedence: asynchronous reset, synchronous reset, parallel load, count and hold. Five control inputs—Master Reset ($\overline{MR}$), Synchronous Reset ($\overline{SR}$), Parallel Enable ($\overline{PE}$), Count Enable Parallel ($\overline{CEP}$) and Count Enable Trickle ($\overline{CET}$)—plus the Up/Down (U/$\overline{D}$) input, determine the mode of operation, as shown in the Mode Select Table. A LOW signal on $\overline{MR}$ overrides all other inputs and asynchronously forces the flip-flop Q outputs LOW. A LOW signal on $\overline{SR}$ overrides counting and parallel loading and allows the Q outputs to go LOW on the next rising edge of CP. A LOW signal on $\overline{PE}$ overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With $\overline{MR}$, $\overline{SR}$ and $\overline{PE}$ HIGH, $\overline{CEP}$ and $\overline{CET}$ permit counting when both are LOW. Conversely, a HIGH signal on either $\overline{CEP}$ or $\overline{CET}$ inhibits counting.

The 'F568 and 'F569 use edge-triggered flip-flops and changing the $\overline{SR}$, $\overline{PE}$, $\overline{CEP}$, $\overline{CET}$ or U/$\overline{D}$ inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

Two types of outputs are provided as overflow/underflow indicators. The Terminal Count ($\overline{TC}$) output is normally HIGH and goes LOW providing $\overline{CET}$ is LOW, when the counter reaches zero in the Down mode, or reaches maximum (9 for the 'F568, 15 for the 'F569) in the Up mode. $\overline{TC}$ will then remain LOW until a state change occurs, whether by counting or presetting, or until U/$\overline{D}$ or $\overline{CET}$ is changed. To implement synchronous multistage counters, the connections between the $\overline{TC}$ output and the $\overline{CEP}$ and $\overline{CET}$ inputs can provide either slow or fast carry propagation. Figure a shows the connections for simple ripple carry, in which the clock period must be longer than the CP to $\overline{TC}$ delay of the first stage, plus the cumulative $\overline{CET}$ to $\overline{TC}$ delays of the intermediate stages, plus the $\overline{CET}$ to CP setup time of the last stage. This total delay plus setup time sets the upper limit on clock frequency. For faster clock rates, the carry lookahead connections shown in Figure b are recommended. In this scheme the ripple delay through the intermediate stages commences with the same clock that causes the first stage to tick over from max to min in the Up mode, or min to max in the Down mode, to start its final cycle. Since this final cycle takes 10 ('F568) or 16 ('F569) clocks to complete, there is plenty of time for the ripple to progress through the intermediate stages. The critical timing that limits the clock period is the CP to $\overline{TC}$ delay of the first stage plus the $\overline{CEP}$ to CP setup time of the last stage. The $\overline{TC}$ output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, registers or counters. For such applications, the Clocked Carry ($\overline{CC}$) output is provided. The $\overline{CC}$ output is normally HIGH. When $\overline{CEP}$, $\overline{CET}$, and $\overline{TC}$ are LOW, the $\overline{CC}$ output will go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again, as shown in the $\overline{CC}$ Truth Table. When the Output Enable ($\overline{OE}$) is LOW, the parallel data outputs O_0-O_3 are active and follow the flip-flop Q outputs. A HIGH signal on $\overline{OE}$ forces O_0-O_3 to the High Z state but does not prevent counting, loading or resetting.

Logic Equations:

Count Enable = $\overline{CEP} \bullet \overline{CET} \bullet PE$

Up ('F568): $\overline{TC} = Q_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet Q_3 \bullet (Up) \bullet \overline{CET}$

('F569): $\overline{TC} = Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3 \bullet (Up) \bullet \overline{CET}$

Down (Both): $\overline{TC} = \overline{Q}_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet \overline{Q}_3 \bullet (Down) \bullet \overline{CET}$

$\overline{CC}$ Truth Table

Inputs						Output
$\overline{SR}$	$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	$\overline{TC}$*	CP	$\overline{CC}$
L	X	X	X	X	X	H
X	L	X	X	X	X	H
X	X	H	X	X	X	H
X	X	X	H	X	X	H
X	X	X	X	H	X	H
H	H	L	L	L	⊓	⊓

* = $\overline{TC}$ is generated internally

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Mode Select Table

Inputs						Operating Mode
$\overline{MR}$	$\overline{SR}$	$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	U/$\overline{D}$	
L	X	X	X	X	X	Asynchronous Reset
H	L	X	X	X	X	Synchronous Reset
H	H	L	X	X	X	Parallel Load
H	H	H	H	X	X	Hold
H	H	H	X	H	X	Hold
H	H	H	L	L	H	Count Up
H	H	H	L	L	L	Count Down

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

4

Fig. a Multistage Counter with Ripple Carry

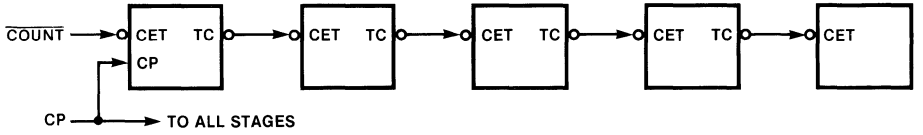
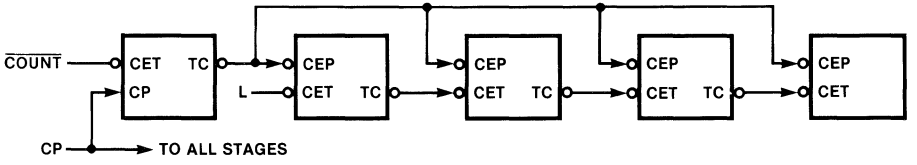
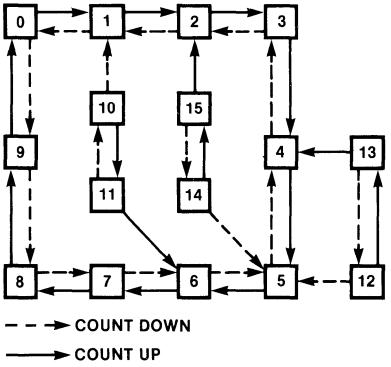


Fig. b Multistage Counter with Lookahead Carry

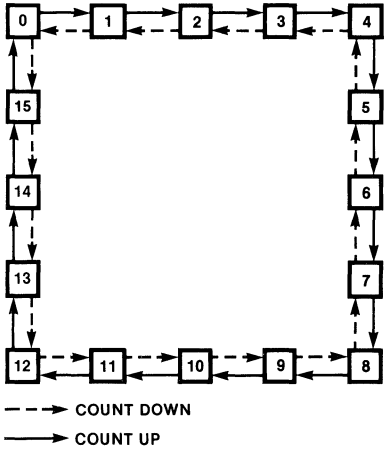


State Diagrams

'F568

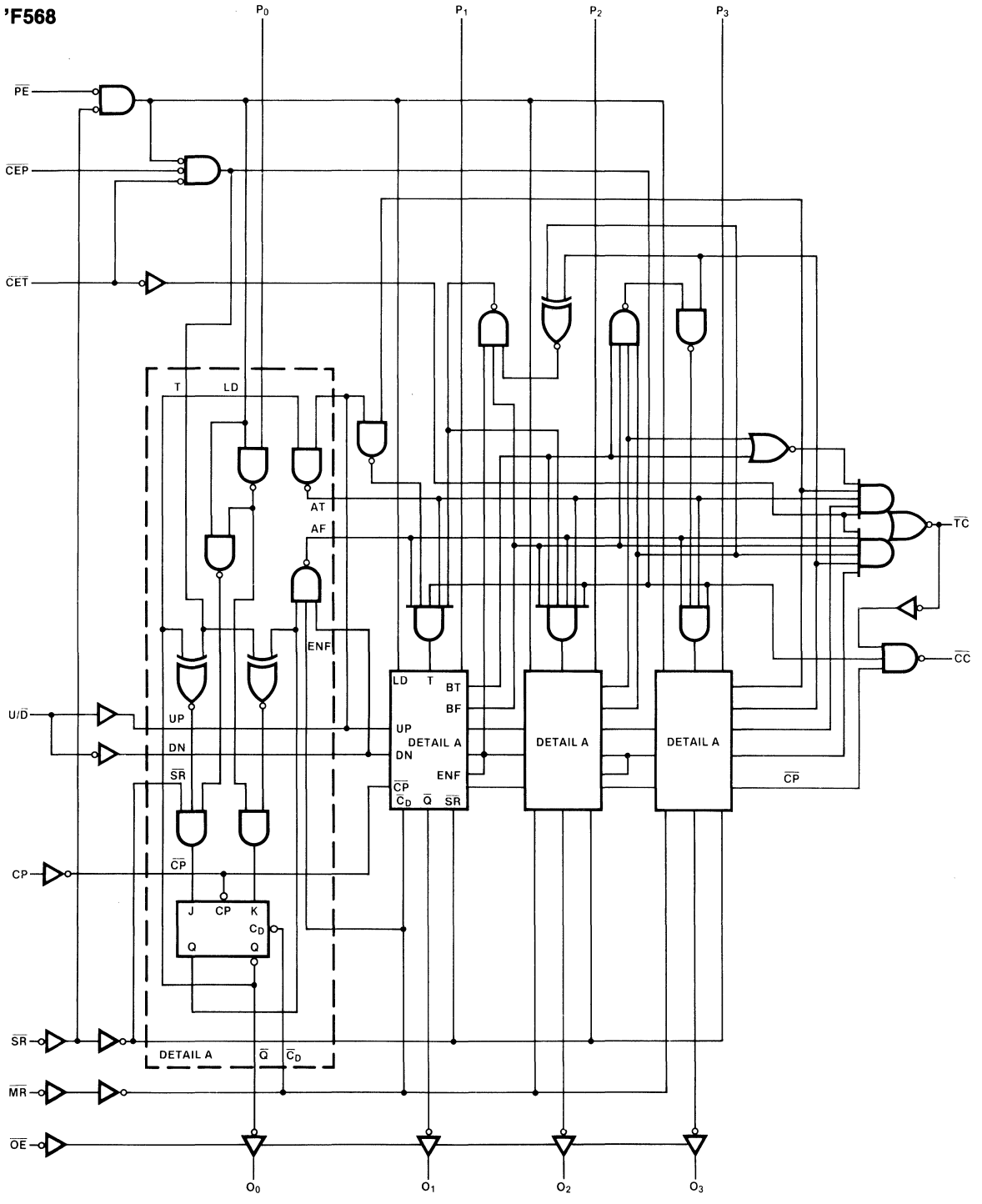


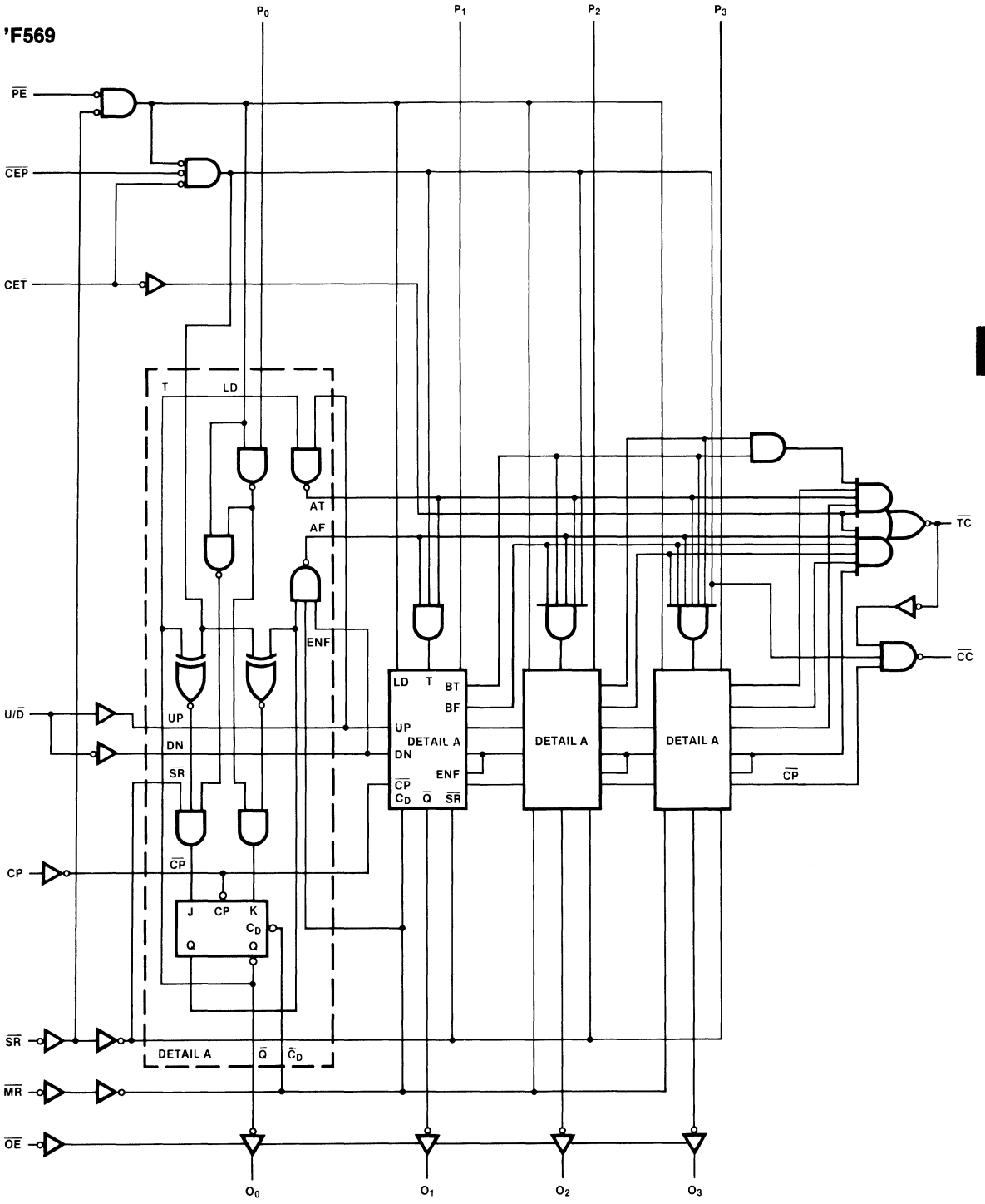
'F569



Logic Diagrams

'F568





Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		45	67	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	100	115				90		MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay CP to O_n ($\overline{PE}$ HIGH or LOW)	3.0 4.0	6.5 9.0	8.5 11.5			3.0 4.0	9.5 13.0	ns	3-1 3-7
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{TC}$	5.5 4.0	12.0 8.5	15.5 11.0			5.5 4.0	17.5 12.5	ns	3-1 3-7
t_{PLH} t_{PHL}	Propagation Delay $\overline{CET}$ to $\overline{TC}$	2.5 2.5	4.5 6.0	6.0 8.0			2.5 2.5	7.0 9.0	ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay U/$\overline{D}$ to $\overline{TC}$ ('F568)	3.5 4.0	8.5 12.5	11.0 16.0			3.5 4.0	12.5 18.0	ns	3-1 3-2
t_{PLH} t_{PHL}	Propagation Delay U/$\overline{D}$ to $\overline{TC}$ ('F569)	3.5 4.0	8.5 8.0	11.0 10.5			3.5 4.0	12.5 12.0	ns	3-1 3-2
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{CC}$	2.5 2.0	5.5 4.5	7.0 6.0			2.5 2.0	8.0 7.0	ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay $\overline{CEP}$, $\overline{CET}$ to $\overline{CC}$	2.5 4.0	5.0 8.5	6.5 11.0			2.5 4.0	7.5 12.5	ns	3-1 3-4
t_{PHL}	Propagation Delay $\overline{MR}$ to O_n	5.0	10.0	13.0			5.0	14.5	ns	3-1 3-11
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	2.5 3.0	5.5 6.0	7.0 3.0			2.5 3.0	8.0 9.0	ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n	1.5 2.0	5.0 4.5	6.5 6.0			1.5 2.0	7.5 7.0		

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\,V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW P_n to CP	4.0 4.0		4.5 4.5	ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW P_n to CP	3.0 3.0		3.5 3.5		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{CEP}$ or $\overline{CET}$ to CP	5.0 5.0		6.0 6.0	ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{CEP}$ or $\overline{CET}$ to CP	0 0		0 0		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{PE}$ to CP	8.0 8.0		9.0 9.0	ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{PE}$ to CP	0 0		0 0		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW U/$\overline{D}$ to CP ('F568)	11.0 16.5		12.5 17.5	ns	3-5
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW U/$\overline{D}$ to CP ('F569)	11.0 7.0		12.5 8.0	ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW U/$\overline{D}$ to CP	0 0		0 0	ns	3-5
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{SR}$ to CP	9.5 8.5		10.5 9.5	ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{SR}$ to CP	0 0		0 0		
$t_w(H)$ $t_w(L)$	CP Pulse Width, HIGH or LOW	4.0 6.0		4.5 6.5	ns	3-7
$t_w(L)$	$\overline{MR}$ Pulse Width, LOW	4.5		5.0	ns	3-11
t_{rec}	$\overline{MR}$ Recovery Time	6.0		7.0	ns	3-11

54F/74F573

Octal D-Type Latch With 3-State Outputs

Description

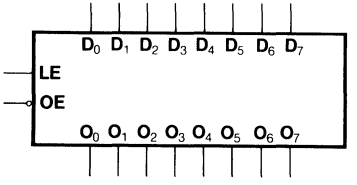
The 'F573 is a high speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ($\overline{OE}$) inputs.

This device is functionally identical to the 'F373 but has different pinouts.

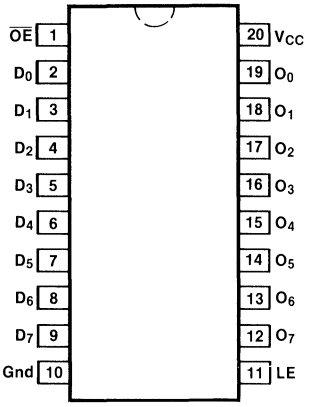
- **Inputs and Outputs on Opposite Sides of Package Allowing Easy Interface with Microprocessors**
- **Useful as Input or Output Port for Microprocessors**
- **Functionally Identical to 'F373**
- **3-State Outputs for Bus Interfacing**

Ordering Code: See Section 5

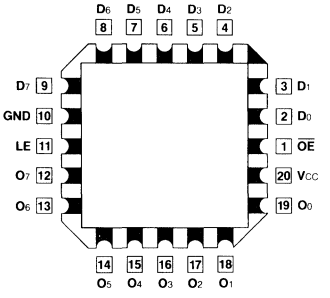
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

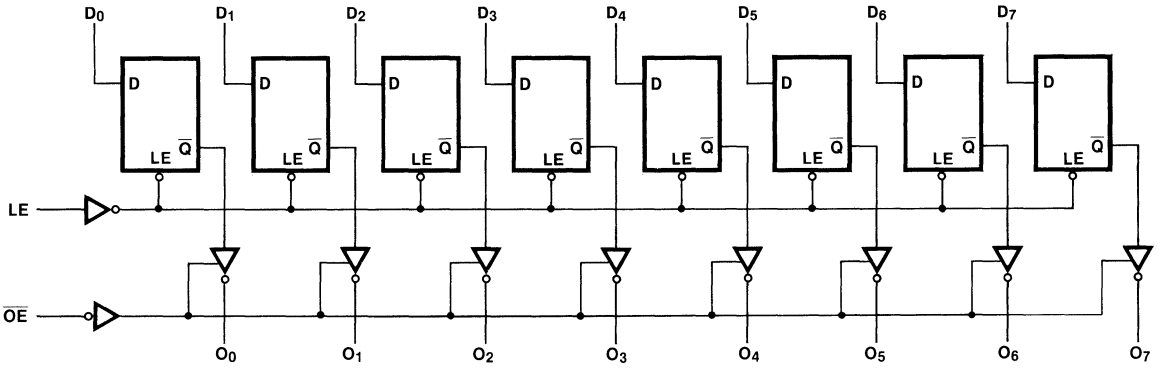
Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
D_0-D_7	Data Inputs	0.5/0.375
LE	Latch Enable Input (Active HIGH)	0.5/0.375
$\overline{OE}$	3-State Output Enable Input (Active LOW)	0.5/0.375
O_0-O_7	3-State Latch Outputs	75/15 (12.5)

Functional Description

The 'F573 contains eight D-type latches with 3-state output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-state buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are in the bi-state mode. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CCZ}	Power Supply Current (All Outputs OFF)		35	55	mA	V_{CC} = Max, $\overline{OE}$ = HIGH D_n, LE = Gnd

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$			T_A, V_{CC} = Mil $C_L = 50\ pF$		T_A, V_{CC} = Com $C_L = 50\ pF$			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to O_n	3.0 2.0	5.3 3.7	7.0 5.0			3.0 2.0	8.0 6.0	ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay LE to O_n	5.0 3.0	9.0 5.2	11.5 7.0			5.0 3.0	13.0 8.0	ns	3-1 3-7
t_{PZH} t_{PZL}	Output Enable Time	2.0 2.0	5.0 5.6	11.0 7.5			2.0 2.0	12.0 8.5	ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time	2.0 2.0	4.5 3.8	6.5 6.0			2.0 2.0	7.5 6.0		

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW D_n to LE	2.0 2.0					2.0 2.0		ns	3-15
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D_n to LE	3.0 3.0					3.0 3.0			
$t_w(H)$	LE Pulse Width, HIGH	6.0					6.0		ns	3-7

54F/74F574

Octal D-Type Flip-Flop With 3-State Outputs

Description

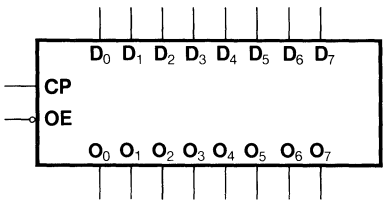
The 'F574 is a high speed low power octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable ($\overline{OE}$). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

This device is functionally identical to the 'F374 except for the pinouts.

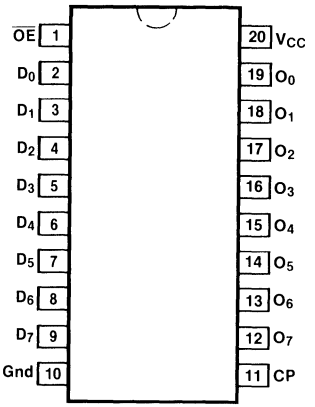
- **Inputs and Outputs on Opposite Sides of Package Allowing Easy Interface with Microprocessors**
- **Useful as Input or Output Port for Microprocessors**
- **Functionally Identical to 'F374**
- **3-State Outputs for Bus Oriented Applications**

Ordering Code: See Section 5

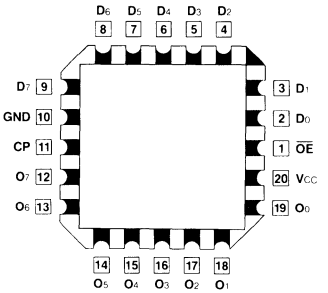
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
D_0-D_7	Data Inputs	0.5/0.375
CP	Clock Pulse Input (Active LOW)	0.5/0.375
$\overline{OE}$	3-State Output Enable Input (Active LOW)	0.5/0.375
O_0-O_7	3-State Outputs	75/15 (12.5)

Functional Description

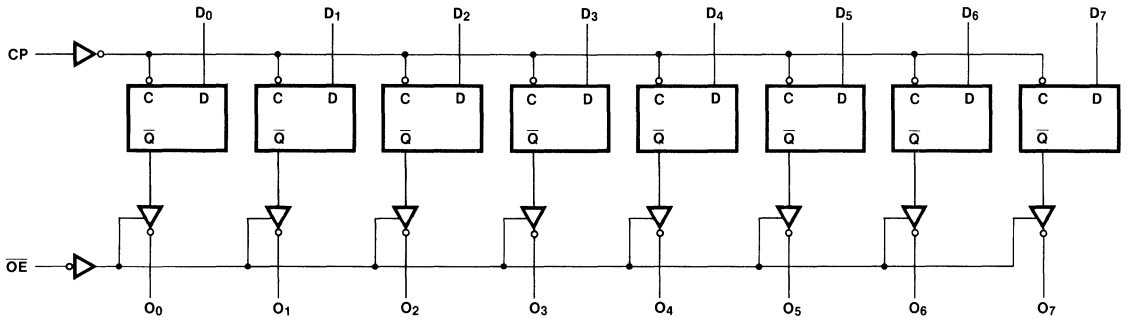
The 'F574 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-state true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Function Table

Inputs			Internal	Outputs	Function
$\overline{OE}$	CP	D	Q	O	
H	H	L	NC	Z	Hold
H	H	H	NC	Z	Hold
H	↑	L	L	Z	Load
H	↑	H	H	Z	Load
L	↑	L	L	L	Data Available
L	↑	H	H	H	Data Available
L	H	L	NC	NC	No Change in Data
L	H	H	NC	NC	No Change in Data

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
↑ = LOW-to-HIGH Transition
NC = No Change

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current (Outputs OFF)		55	86	mA	V_{CC} = Max, $\overline{OE}$ = HIGH

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	100							MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay CP to O_n		7.5 9.5						ns	3-1 3-7
t_{PZH} t_{PZL}	Output Enable Time		11.5 7.5						ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time		7.0 5.5							

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C V_{CC} = +5.0 V			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
t_s(H) t_s(L)	Set-up Time, HIGH or LOW D_n to CP	2.0 2.0							ns	3-5
t_h(H) t_h(L)	Hold Time, HIGH or LOW D_n to CP	2.0 2.0								
t_w(H) t_w(L)	CP Pulse Width HIGH or LOW	5.0 5.0							ns	3-7

54F/74F579

8-Bit Bidirectional Binary Counter With 3-State Outputs

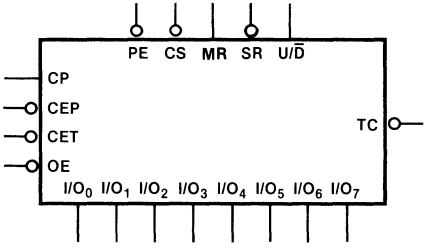
Description

The 'F579 is a fully synchronous 8-stage up/down counter with multiplexed 3-state I/O ports for bus-oriented applications. It features a preset capability for programmable operation, carry lookahead for easy cascading and a U/$\overline{D}$ input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the rising edge of the clock.

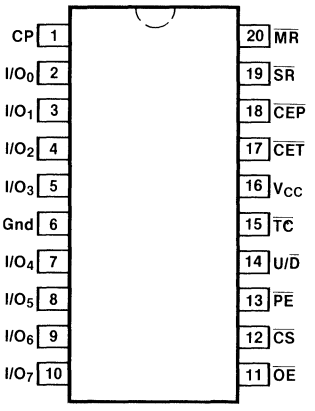
- **Multiplexed 3-State I/O ports**
- **Built-In Lookahead Carry Capability**
- **Count Frequency 100 MHz Typ**
- **Supply Current 75 mA Typ**

Ordering Code: See Section 5

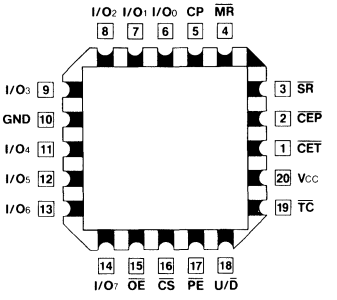
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC

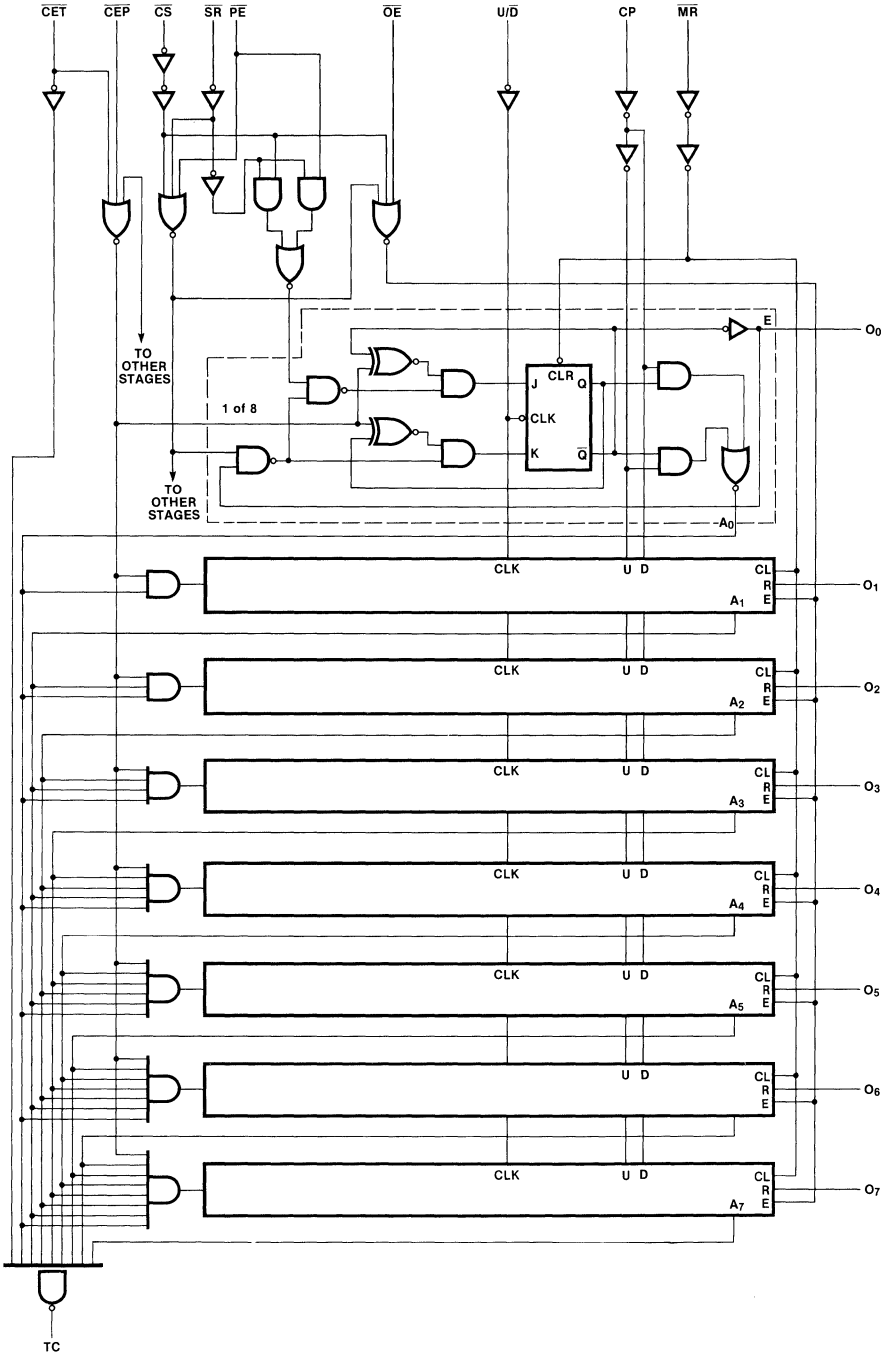


Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
I/O_0-I/O_7	Data Inputs	0.5/0.375
	Data Outputs	75/15 (12.5)
$\overline{PE}$	Parallel Enable Input (Active LOW)	0.5/0.375
U/$\overline{D}$	Up-Down Count Control Input	0.5/0.375
$\overline{MR}$	Master Reset Input (Active LOW)	0.5/0.375
$\overline{SR}$	Synchronous Reset Input (Active LOW)	0.5/0.375
$\overline{CEP}$	Count Enable Parallel Input (Active LOW)	0.5/0.375
$\overline{CET}$	Count Enable Trickle Input (Active LOW)	0.5/0.375
$\overline{CS}$	Chip Select Input Active (Active LOW)	0.5/0.375
$\overline{OE}$	Output Enable Input (Active LOW)	0.5/0.375
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
$\overline{TC}$	Terminal Count Output (Active LOW)	25/12.5

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Function Table

$\overline{MR}$	$\overline{SR}$	$\overline{CS}$	$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	U/$\overline{D}$	$\overline{OE}$	CP	Function
X	X	H	X	X	X	X	X	X	I/O_a to I/O_h in High Z ($\overline{PE}$ disabled)
X	X	L	H	X	X	X	H	X	I/O_a to I/O_h in High Z
X	X	L	H	X	X	X	L	X	Flip-flop outputs appear on I/O lines
L	X	X	X	X	X	X	X	X	Asynchronous reset for all flip-flops
H	L	X	X	X	X	X	X	↑	Synchronous reset for all flip-flops
H	H	L	L	X	X	X	X	↑	Parallel load all flip-flops
H	H	(not LL)		H	X	X	X	↑	Hold
H	H	(not LL)		X	H	X	X	↑	Hold ($\overline{TC}$ held HIGH)
H	H	(not LL)		L	L	H	X	↑	Count up
H	H	(not LL)		L	L	L	X	↑	Count down

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↑ = LOW to HIGH Clock Transition
not LL = $\overline{CS}$ and $\overline{PE}$ should never both be LOW voltage level at the same time.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions	
		Min	Typ	Max			
I_{CCH}	Power Supply Current		50	70	mA	Outputs HIGH	V_{CC} = Max
I_{CCL}			80	100		Outputs LOW	
I_{CCZ}			80	100		Outputs Disabled	

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	80	100						MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay CP to I/O_n			10.0 10.0					ns	3-1 3-2
t_{PLH} t_{PHL}	Propagation Delay U/$\overline{D}$ to $\overline{TC}$, $\overline{CET}$ to $\overline{TC}$ CP to $\overline{TC}$			15.0 15.0					ns	3-1, 3-2
t_{PZH} t_{PZL}	Output Disable Time			20.0 20.0					ns	3-1, 3-12 3-13
t_{PHZ} t_{PLZ}	Output Enable Time			20.0 20.0					ns	3-1, 3-12 3-13

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW Data to CP	5.0 5.0			ns	3-14
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW Data to CP	0 0				
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{PE}$, $\overline{SR}$ or $\overline{CS}$ to CP	12.0 12.0			ns	3-14
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{PE}$, $\overline{SR}$ or $\overline{CS}$ to CP	0 0				
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{CET}$ or $\overline{CEP}$ to CP	10.0 10.0			ns	3-14
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{CET}$ or $\overline{CEP}$ to CP	0 0				
$t_w(H)$ $t_w(L)$	Clock Pulse Width HIGH or LOW	5.0 5.0			ns	3-2 3-7

54F/74F582

4-Bit BCD Arithmetic Logic Unit

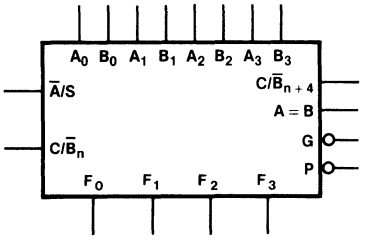
Description

The 'F582 is a 24-pin expandable Arithmetic Logic Unit (ALU) that performs two arithmetic operations (A plus B, A minus B), compare (A equals B), and binary to BCD conversion. In addition to a ripple carry output, carry Propagate (P) and Generate (G) outputs are provided for use with the 'F182 carry lookahead generator for high-speed expansion to higher decades. It is functionally equivalent to the 82S82.

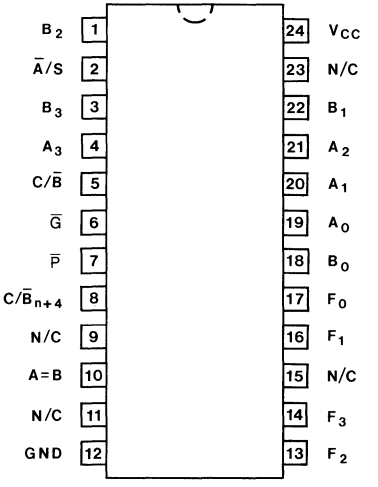
- **Performs Four BCD Functions**
- **$\overline{P}$ and $\overline{G}$ Outputs for High-Speed Expansion**
- **Add/Subtract Delay 22 ns Max**
- **Lookahead Delay 15.5 ns Max**
- **Supply Current 85 mA Max**
- **24-Lead 300 Mil Slim Package**

Ordering Code: See Section 5

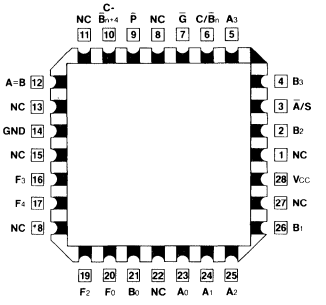
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
A_0-A_3	A Operand Inputs	0.5/.75
B_0	B Operand Input	0.5/.375
B_1	B Operand Input	0.5/1.875
B_2	B Operand Input	0.5/1.125
B_3	B Operand Input	0.5/.75
F_0-F_3	Functional Output	25/12.5
A = B	Comparator Output	OC*/12.5
$\overline{P}$	Carry Propagate Output	25/12.5
$\overline{G}$	Carry Generate Output	25/12.5
$C/\overline{B}$	Carry/$\overline{\text{Borrow}}$ Input	0.5/.875
$C/\overline{B}_{n+4}$	Carry/$\overline{\text{Borrow}}$ Output	25/12.5
$\overline{A}/S$	$\overline{\text{Add}}$/Subtract	0.5/1.125

*OC—Open Collector

Functional Description

The 'F582 Binary Coded Decimal (BCD) Arithmetic Logic Unit (ALU) is a 24-pin expandable unit that performs addition, subtraction, comparison of two numbers, and binary to BCD conversion.

The 'F582s input and output logic includes a Carry/$\overline{\text{Borrow}}$ which is generated internally in the lookahead mode, allowing BCD arithmetic to be computed directly. For more than one BCD decade, the Carry/$\overline{\text{Borrow}}$ term may ripple between 'F582s.

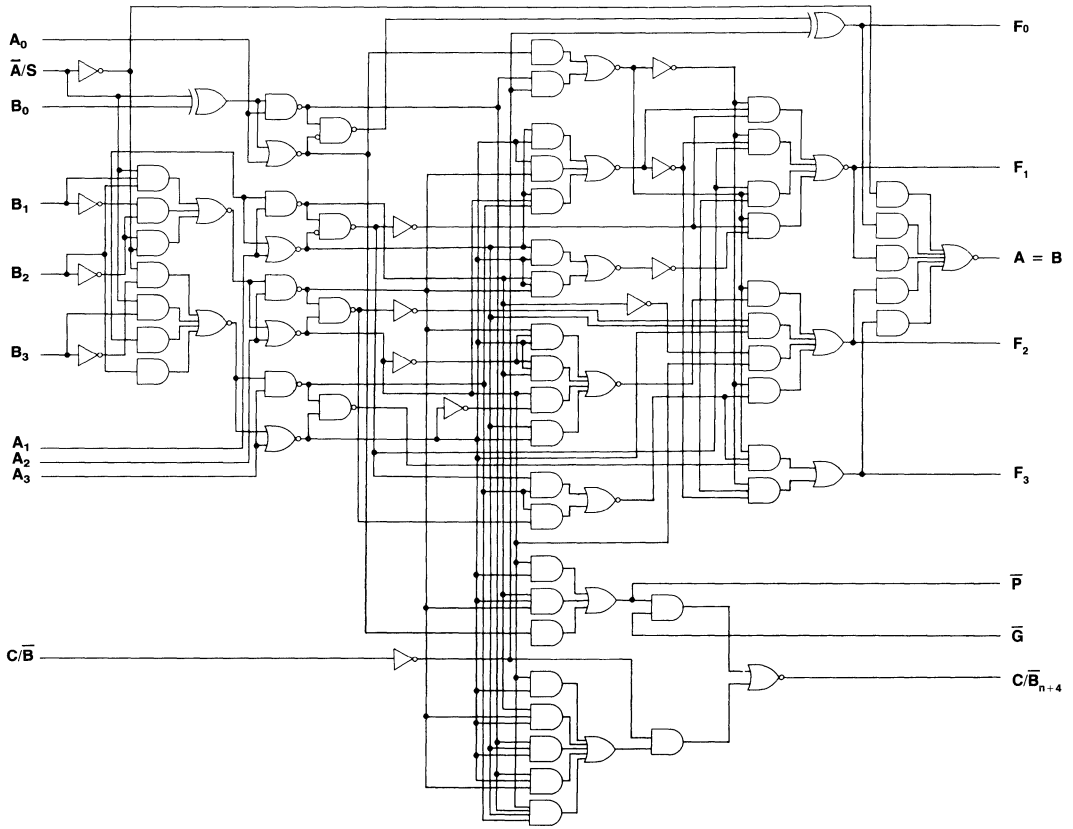
When $\overline{A}$/S is LOW, BCD addition is performed ($A + B + C/\overline{B} = F$). If an input is greater than 9, binary to BCD conversion results at the output.

When $\overline{A}$/S is HIGH, subtraction is performed. If the $C/\overline{B}$ is LOW, then the subtraction is accomplished by internally computing the 9s complement addition of two BCD numbers ($A\text{-}B\text{-}1 = F$). When $C/\overline{B}$ is HIGH, the difference of the two numbers is figured as $A\text{-}F = F$. For A is greater than or equal to B, the BCD difference appears at the output F in its true form. If A is less than B and $C/\overline{B}$ is LOW, the difference appears at the output as the 10s complement of the true form. If A is less than B and $C/\overline{B}$ is LOW, the 9s complement of the true form appears at the output F. As long as A is less than B, an Active LOW borrow is also generated.

The 'F582 also performs binary to BCD conversion. For inputs between 10 and 15, binary to BCD conversion occurs by grounding one set of the inputs, A or B, and applying the binary number to the other set of inputs. This will generate a carry term to the next decade.

4

Logic Diagram



DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		55	85	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n or B_n to F_n	2.5 2.5	17.5 17.5	22.0 22.0			2.5 2.5	23.0 23.0	ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay A_n or B_n to $C/\overline{B}_{n+4}$	4.0 4.0	17.0 12.5	21.5 16.0			4.0 4.0	22.5 17.0	ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay $C/\overline{B}_n$ to $C/\overline{B}_{n+4}$	4.0 2.5	6.5 4.5	8.5 6.0			4.0 2.5	9.5 7.0	ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay A_n or B_n to A = B	8.0 8.0	19.0 17.0	24.0 21.5			8.0 8.0	25.0 22.5	ns	3-1, 3-3 3-4
t_{PLH} t_{PHL}	Propagation Delay A_n or B_n to $\overline{G}$ or $\overline{P}$	4.0 4.0	12.0 12.0	15.5 15.5			4.0 4.0	16.5 16.5	ns	3-1 3-3
t_{PLH}	Propagation Delay $\overline{A}/S$ to F_n	2.5	21.0	27.0			2.5	28.0	ns	3-1 3-10

54F/74F583

4-Bit BCD Adder

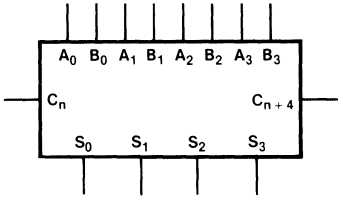
Description

The 'F583 high-speed 4-bit, BCD full adder with internal carry lookahead accepts two 4-bit decimal numbers (A_0-A_3, B_0-B_3) and a Carry Input (C_n). It generates the decimal sum outputs (S_0-S_3), and a Carry Output (C_{n+4}) if the sum is greater than 9. The 'F583 is the functional equivalent of the 82S83.

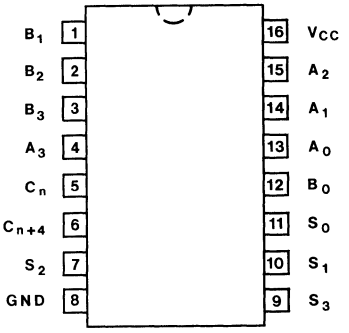
- **Adds Two Decimal Numbers**
- **Full Internal Lookahead**
- **Fast Ripple Carry for Economical Expansion**
- **Sum Output Delay Time 16.5 ns Max**
- **Ripple Carry Delay Time 8.5 ns Max**
- **Input to Ripple Delay Time 14.0 ns Max**
- **Supply Current 60 mA Max**

Ordering Code: See Section 5

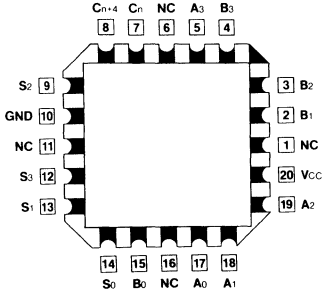
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

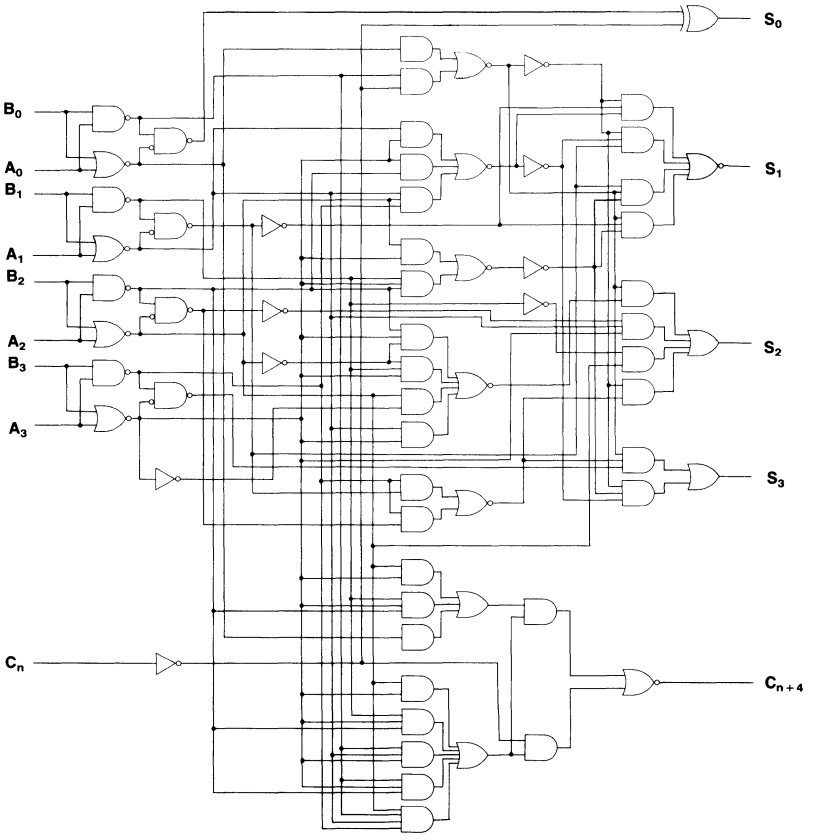
Pin Names	Description	54F/74F(U.L.) HIGH/LOW
A_0-A_3	A Operand Inputs	0.5/.75
B_0-B_3	B Operand Inputs	0.5/.75
C_n	Carry Input	0.5/.375
S_0-S_3	Sum Outputs	25/12.5
C_{n+4}	Carry Output	25/12.5

Functional Description

The 'F583 4-bit binary coded (BCD) full adder performs the addition of two decimal numbers (A_0-A_3, B_0-B_3). The lookahead generates the BCD carry terms internally, allowing the 'F583 to then do BCD addition correctly. For BCD numbers 0 through 9 at A and B inputs, the BCD sum forms at the output. In the addition of two BCD numbers totalling a number greater than 9, a valid BCD number and a carry will result.

For input values larger than 9, the number is converted from binary to BCD. Binary to BCD conversion occurs by grounding one set of inputs, A_n or B_n, and applying any 4-bit binary number to the other set of inputs. If the input is between 0 and 9, a BCD number occurs at the output. If the binary input falls between 10 and 15, a carry term is generated. Both the carry term and the sum are the BCD equivalent of the binary input. Converting binary numbers greater than 16 may be achieved through cascading 'F583s.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		40	60	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			54F T_A, V_{CC} = Mil C_L = 50 pF		74F T_A, V_{CC} = Com C_L = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n or B_n to S_n	2.5 2.5	13.0 11.0	16.5 14.0	2.5 2.5	20.5 19.0	2.5 2.5	17.5 15.0	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay C_n to C_{n+4}	2.5 2.5	6.5 5.0	8.5 6.5	2.5 2.5	10.5 8.5	2.5 2.5	9.5 7.5	ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay A_n or B_n to C_{n+4}	4.0 4.0	11.0 8.0	14.0 10.5	4.0 4.0	19.5 13.5	4.0 4.0	15.0 11.5	ns	3-1 3-4

54F/74F588

Octal Bidirectional Transceiver With 3-State Inputs/Outputs and IEEE-488 Termination Resistors

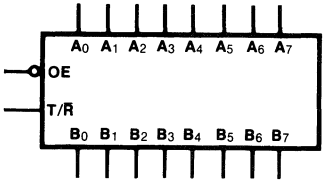
Description

The 'F588 contains eight non-inverting bidirectional buffers with 3-state outputs and is intended for bus-oriented applications. The B ports have termination resistors as specified in the IEEE-488 specifications. Current sinking capability is 20 mA at the A ports and 48mA at the B ports. The Transmit/Receive ($T/\overline{R}$) input determines the direction of data flow through the bidirectional transceiver. Transmit (active HIGH) enables data from A ports to B ports; Receive (active LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a high impedance condition.

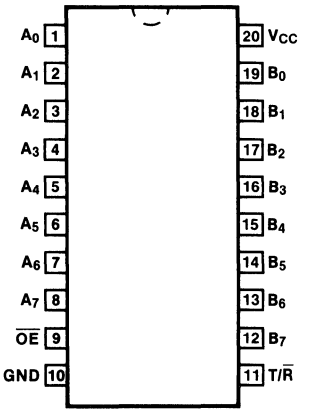
- **Non-Inverting Buffers**
- **Bidirectional Data Path**
- **B Outputs Sink 48 mA, Source 15 mA**

Ordering Code: See Section 5

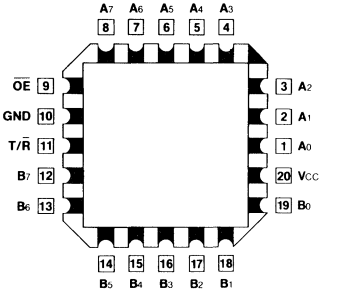
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

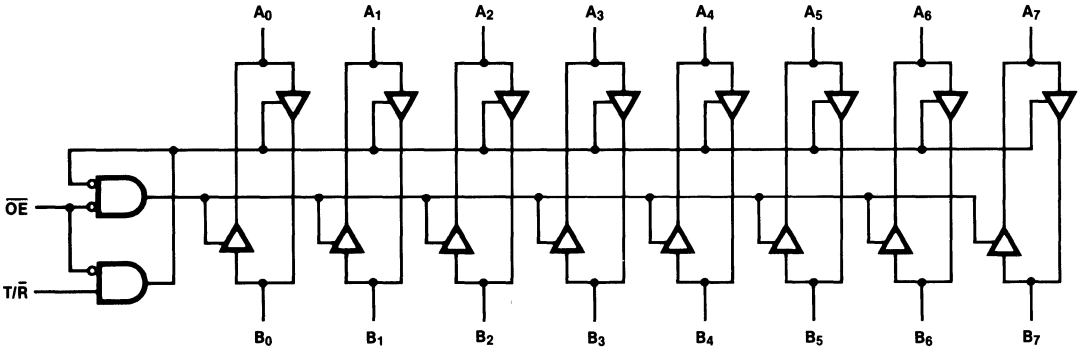
Pin Names	Description	54F/74F(U.L.) HIGH/LOW
$\overline{OE}$	Output Enable Input (Active LOW)	0.5/0.75
$T/\overline{R}$	Transmit/Receive Control Input	0.5/0.75
A_0-A_7	A Port Inputs or 3-State Outputs	1.75/0.406 75/12.5
B_0-B_7	B Port Inputs or 3-State Outputs	T*/2.0 75/15 (12.5)

*T = Restive Termination per IEEE-488 Standard

Truth Table

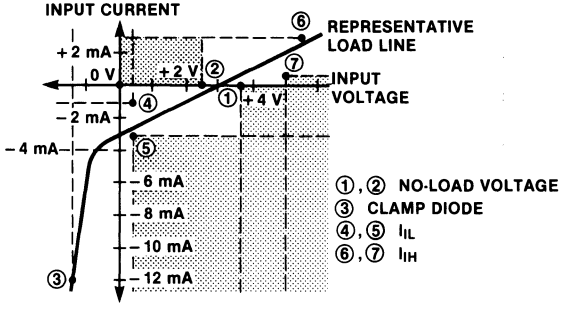
Inputs		Outputs
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Impedance

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

B Port Input Characteristic with T/$\overline{R}$ LOW



DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter		54F/74F Min	54F/74F Typ	54F/74F Max	Units	Conditions	
V_{OH}	Output HIGH Voltage A_0-A_7, B_0-B_7		2.4			V	I_{OH} = -3.0 mA, V_{CC} = Min V_{IN} = V_{IH}, $\overline{OE}$ = LOW T/$\overline{R}$ = HIGH	
V_{OL}	Output LOW Voltage B_0-B_7	XM			0.55	V	I_{OL} = 48 mA	$\overline{OE}$ = LOW
		XC					I_{OL} = 64 mA	T/$\overline{R}$ = HIGH
V_{NL}	No-load Voltage B_0-B_7		2.5[2]		3.7[1]	V	T/$\overline{R}$ = LOW, I_{OUT} = 0	
V_{CD}	Input Clamp Diode Voltage				-1.2[3]	V	I_{IN} = -18 mA V_{CC} = Min	
I_{IH}	Input HIGH Current Breakdown Test, A_0-A_7				-1.0	mA	V_{IN} = 5.5 V	
I_{IH}	Input HIGH Current B_0-B_7		0.7[7]		2.5[6]	mA	V_{IN} = 5.0 V, T/$\overline{R}$ = LOW V_{IN} = 5.5 V, T/$\overline{R}$ = LOW	
I_{IL}	Input LOW Current B_0-B_7		1.3		3.2[5]	mA	V_{IN} = 0.4 V, T/$\overline{R}$ = LOW	
$I_{IH} + I_{OZH}$	3-State Output OFF Current HIGH, A_0-A_7				70	μA	V_{IN} = 2.7 V, T/$\overline{R}$ = LOW V_{CC} = Max	
I_{CCH} I_{CCL} I_{CCZ}	Power Supply Current			67 90 83	100 135 125	mA	$\overline{OE}$ = LOW, V_{CC} = Max A_n = LOW, T/$\overline{R}$ = HIGH $\overline{OE}$ = HIGH, V_{CC} = Max	

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF Min	Typ	Max	54F T_A, V_{CC} = Mil, C_L = 50 pF Min	Max	74F T_A, V_{CC} = Com, C_L = 50 pF Min	Max	Units	Fig. No.
t_{PLH} t_{PHL}	Propagation Delay A to B or B to A	2.5 2.5	4.5 5.0	6.0 6.5			2.5 2.5	7.0 7.5	ns	3-1 3-4
t_{PZH} t_{PZL}	Output Enable Time T/$\overline{R}$ or $\overline{OE}$ to A or B	2.5 2.5	5.0 7.0	7.0 9.0			2.5 2.5	8.0 10.0	ns	3-1 3-2
t_{PHZ} t_{PLZ}	Output Disable Time T/$\overline{R}$ or $\overline{OE}$ to A or B	2.5 2.5	5.5 5.5	7.0 7.0			2.5 2.5	8.0 8.0	ns	3-13

54F/74F604

Dual Octal Registers With Multiplexed 3-State Outputs

Description

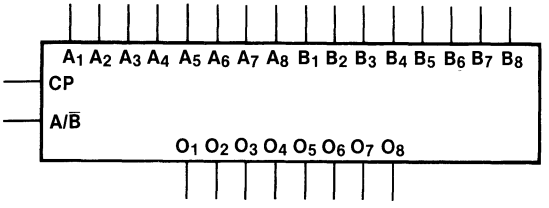
The 'F604 contains sixteen D-type edge-triggered flip-flops with common clock and individual data inputs. Organized as 8-bit A and B registers, the flip-flop outputs are connected by pairs to eight 2-input multiplexers. A Select ($A/\overline{B}$) input determines whether the A or B register contents are multiplexed to the eight 3-state outputs. Data entered from the I_0 inputs are selected when $A/\overline{B}$ is LOW; data from the I_1 inputs are selected when $A/\overline{B}$ is HIGH. Data enters the flip-flops on the rising edge of the Clock (CP) input, which also controls the 3-state outputs. The outputs are enabled when CP is HIGH and disabled when CP is LOW.

This function is well suited for receiving 16-bit simultaneous data and transmitting it as two sequential 8-bit words. The 'F604 has reduced propagation delays.

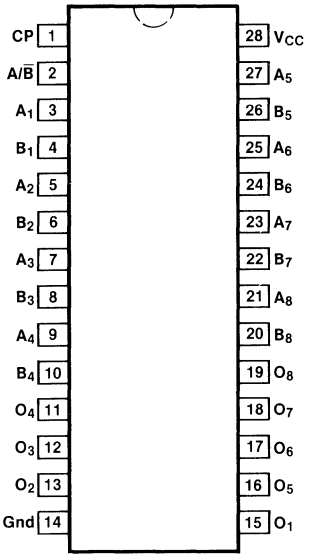
- **Stores 16-Bit Wide Data Inputs**
- **Multiplexed 8-Bit Outputs**
- **Propagation Delay 10 ns Typ**
- **Power Supply Current 140 mA Typ**

Ordering Code: See Section 5

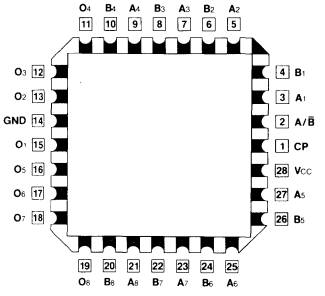
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC

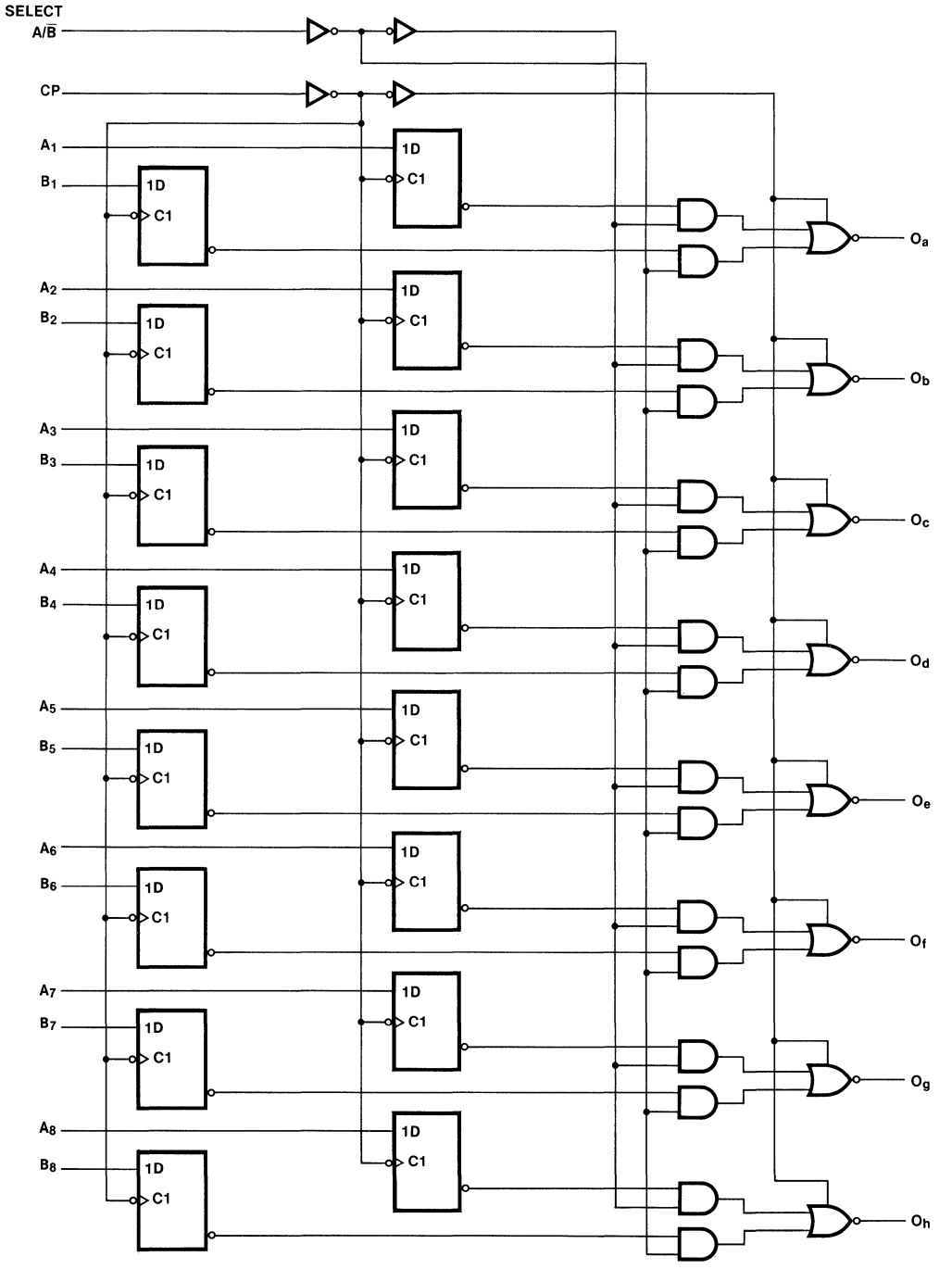


Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
A_1-A_8	Inputs A	0.5/0.375
B_1-B_8	Inputs B	0.5/0.375
$A/\overline{B}$	Select Inputs	0.5/0.375
O_1-O_8	Outputs	75/15 (12.5)
CP	Clock Pulse Input	0.5/0.375

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Function Table

Inputs				Outputs
A_1-A_8	B_1-B_8	Select A/$\overline{B}$	Clock	O_1-O_8
A data	B data	L	↑	B data
A data	B data	H	↑	A data
X	X	X	L	Z
X	X	L	H	B register stored data
X	X	H	H	A register stored data

H = HIGH Level (steady state)
L = LOW Level (steady state)
X = Immaterial
Z = HIGH Impedance state
↑ = LOW-to-HIGH Transition

4

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions	
		Min	Typ	Max			
I_{CCH}	Power Supply Current		75	100	mA	Outputs HIGH, V_{IN} = Gnd	V_{CC} = Max
I_{CCL}			85	100		Outputs LOW, V_{IN} = Open	

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	100							MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay Select A/B to O_n (Data: A = L, B = H)		11.0 10.0						ns	3-1 3.3
t_{PLH} t_{PHL}	Propagation Delay Select A/B to O_n (Data: A = L, B = H)		11.0 10.0						ns	3-1 3.4
t_{PZH} t_{PZL}	Enable Time		8.0 12.5						ns	3-1 3-13
t_{PHZ} t_{PLZ}	Disable Time		8.0 12.5						ns	3-1 3-12

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW	3.0 3.0			ns	3-14
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW	0 0			ns	3-14
$t_w(H)$ $t_w(L)$	Clock Pulse Width HIGH or LOW	5.0 5.0			ns	3-1 3-7

54F/74F610 • 54F/74F612

Memory Mappers
With 3-State Outputs and Output Latches

Description

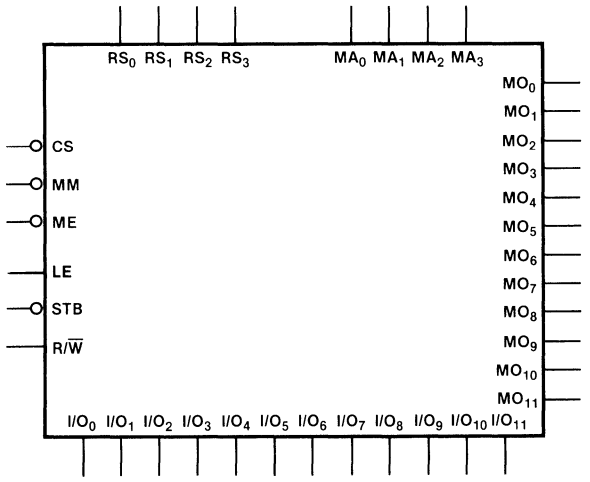
The 'F610 and 'F612 memory mappers are designed to expand the address capability of a Central Processing Unit (CPU) by eight bits. These devices contain sixteen map registers, each containing twelve bits, that are loaded by the CPU. Subsequently, the four most significant bits of the memory address select one of the sixteen registers. The twelve output bits plus the four least significant memory address bits form the expanded address. In this mode the 'F610 output stages may be transparent or latched. The addressable memory space is increased by periodically reloading the map registers.

In the pass mode the address bits on the register select inputs appear as the most significant bits at the map outputs, with LOW levels appearing on the other bit positions.

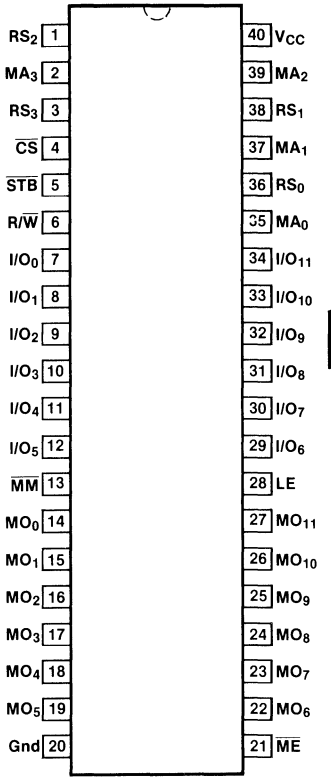
- **Expands 4 Address Lines to 12 Address Lines**
- **Designed for Paged Memory Mapping**
- **Output Latches Provided on 'F610**
- **3-State Outputs**

Ordering Code: See Section 5

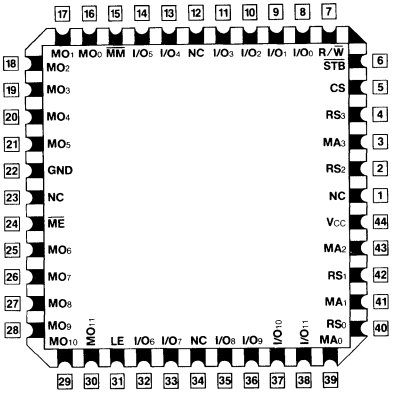
Logic Symbol



Connection Diagrams



Pin Assignment for DIP



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
IO_0-I/O_{11}	Data Inputs or	1.75/0.406
	3-State Outputs	75/15 (12.5)
RS_0-RS_3	Register Select Inputs	0.5/0.375
R/$\overline{W}$	Read/$\overline{Write}$ Control	0.5/0.375
STROBE	Strobe Input	0.5/0.375
$\overline{CS}$	Chip Select	0.5/0.375
MA_0-MA_3	Map Address Inputs	0.5/0.375
MO_0-MO_{11}	Map Outputs	75/15 (12.5)
$\overline{MM}$	Map Mode Input	0.5/0.375
$\overline{ME}$	Map Enable	0.5/0.375
LE ('F610)	Latch Enable	0.5/0.375

Functional Description

These memory-mapper integrated circuits contain a 4-line to 16-line decoder, a 16-word by 12-bit RAM, sixteen channels of 2-line to 1-line multiplexers, and other miscellaneous circuitry on a monolithic chip. The 'F610 also contains twelve latches with an enable control.

The memory mappers are designed to expand a microprocessor's memory address capability by eight bits. The four most significant bits of the memory address bus can be used to select one of sixteen map registers that contain twelve bits each. These twelve bits are presented to the system memory address through the map output buffers with the unused memory address bits from the CPU. If the memory mapper is omitted, the addressable memory space remains as if the map registers were not reloaded. The addressable memory space is increased only by periodically reloading the map registers from the data bus.

This configuration lends itself to memory utilization of sixteen pages of $2^{(n-4)}$ registers each without reloading (n = number of address bits available from CPU).

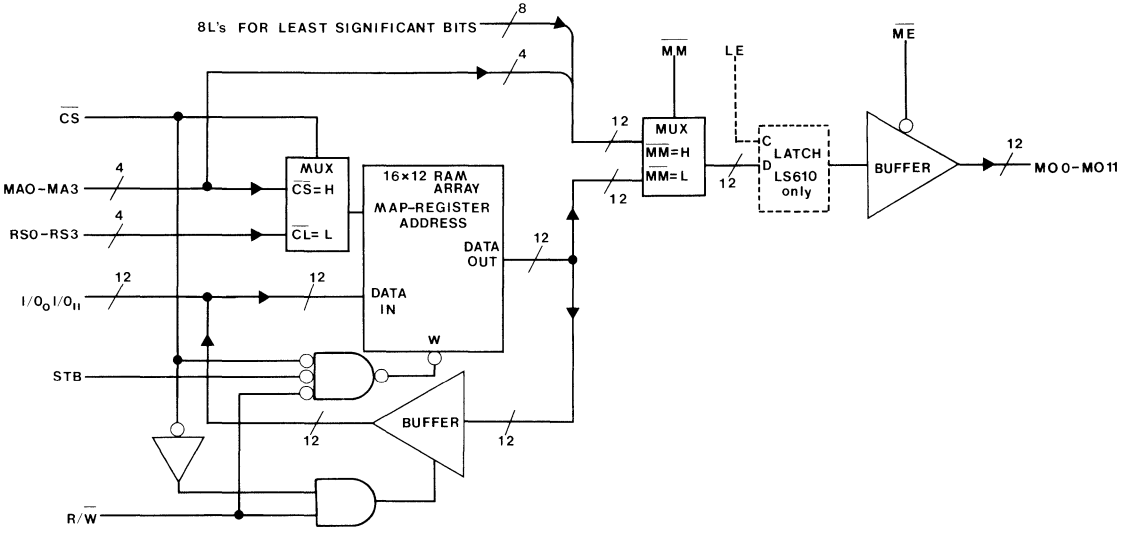
These devices have four modes of operation (Read, Write, Map, and Pass). Data may be read from or loaded into the map register selected by the register select inputs (RS_0-RS_3) under control of R/$\overline{W}$ whenever chip select ($\overline{CS}$) is LOW. The data I/O takes place on the data bus I/O_0-I/O_7. The map operation will output the contents of the map register selected by the map address inputs (MA_0-MA_3) when $\overline{CS}$ is HIGH and $\overline{MM}$ (Map Mode control) is LOW. The 'F612 output stages are transparent in this mode, while the 'F610 outputs may be transparent or latched. When $\overline{MM}$ is HIGH (pass mode), the address bits on MA_0-MA_3 appear at MO_8-MO_{11} respectively at the map outputs (assuming appropriate latch enable) with LOW levels in the other bit positions.

Function Table

Mapper Inputs	I/O		MAP	PASS
	WRITE(LOAD)	READ(VERIFY)		
$\overline{CS}$	Active LOW	Active LOW	Inactive HIGH	Inactive HIGH
$\overline{STROBE}$	Active LOW	Immaterial	Immaterial	Immaterial
$R/\overline{W}$	LOW	HIGH	Immaterial	Immaterial
$\overline{MM}$	Immaterial	Immaterial	Active LOW	Inactive HIGH
$\overline{ME}$	Inactive HIGH	Inactive HIGH	Active	Active
RS_0-RS_3	Address of Selected Register	Address of Selected Register	Immaterial	Immaterial
MA_0-MA_3	Immaterial	Immaterial	Address of Selected Register	Address of Selected Register
MO_0-MO_{11}	High Impedance	High Impedance	Valid Address	Valid Address
I/O_0-I/O_{11}	Register contents to be loaded (input)	Register contents to be read (output)	Input Mode	Input Mode

4

Block Diagram



DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		150	230	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units
		T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay $\overline{CS}$ to MO			45.0 45.0					ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{MM}$ to MO			15.0 15.0					ns
t_{PLH} t_{PHL}	Propagation Delay MA to MO ($\overline{MM}$ = LOW)			35.0 35.0					ns
t_{PLH} t_{PHL}	Propagation Delay MA to MO ($\overline{MM}$ = HIGH)			20.0 20.0					ns
t_{PLH} t_{PHL}	Propagation Delay C to MO			20.0 20.0					ns
t_{PLH} t_{PHL}	Propagation Delay RS to D			35.0 35.0					ns
t_{PZH} t_{PZL}	Enable Time ME to MO			15.0 15.0					ns
t_{PHZ} t_{PLZ}	Disable Time ME to MO			15.0 15.0					ns
t_{PZH} t_{PZL}	Enable Time $\overline{CS}$ to I/O			25.0 25.0					ns
t_{PHZ} t_{PLZ}	Disable Time $\overline{CS}$ to I/O			25.0 25.0					ns
t_{PZH} t_{PZL}	Enable Time R/$\overline{W}$ to I/O			25.0 25.0					ns
t_{PHZ} t_{PLZ}	Disable Time R/$\overline{W}$ to I/O			25.0 25.0					ns

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com	
		Min Typ Max	Min Max	Min Max	
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{CS}$ to STROBE	10.0 10.0			ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{CS}$ to STROBE	10.0 10.0			ns
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW R/$\overline{W}$ to STROBE	10.0 10.0			ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW R/$\overline{W}$ to STROBE	10.0 10.0			ns
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW RS to STROBE	10.0 10.0			ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW RS to STROBE	10.0 10.0			ns
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW I/O to STROBE	75.0 75.0			ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW I/O to STROBE	10.0 10.0			ns
$t_w(H)$ $t_w(L)$	STROBE Pulse Width HIGH or LOW	30.0 30.0			ns

Fig. a Memory Mapper

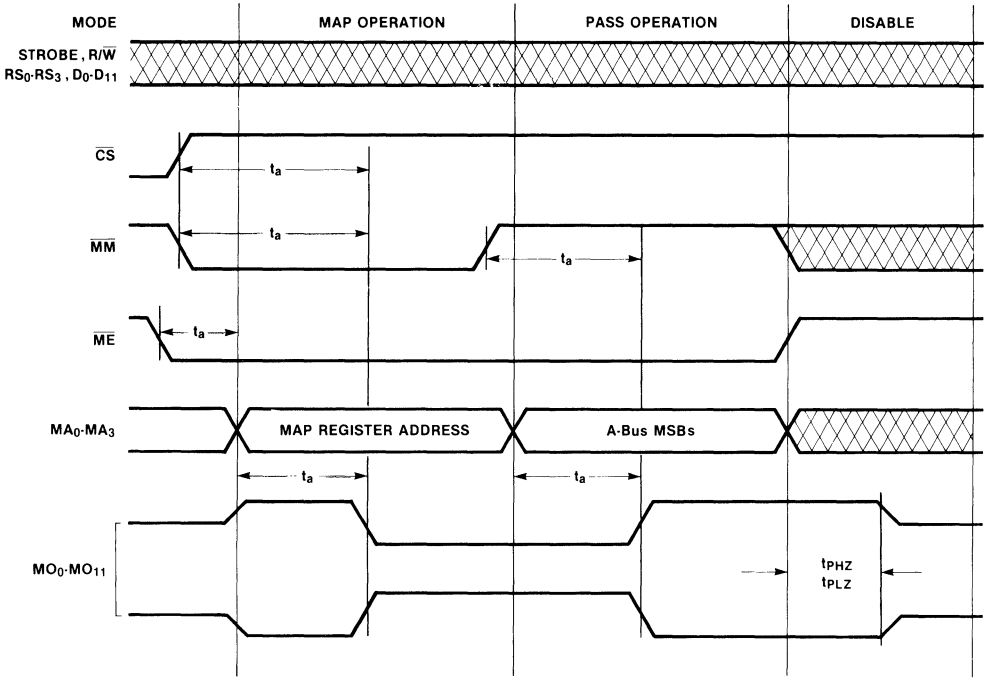
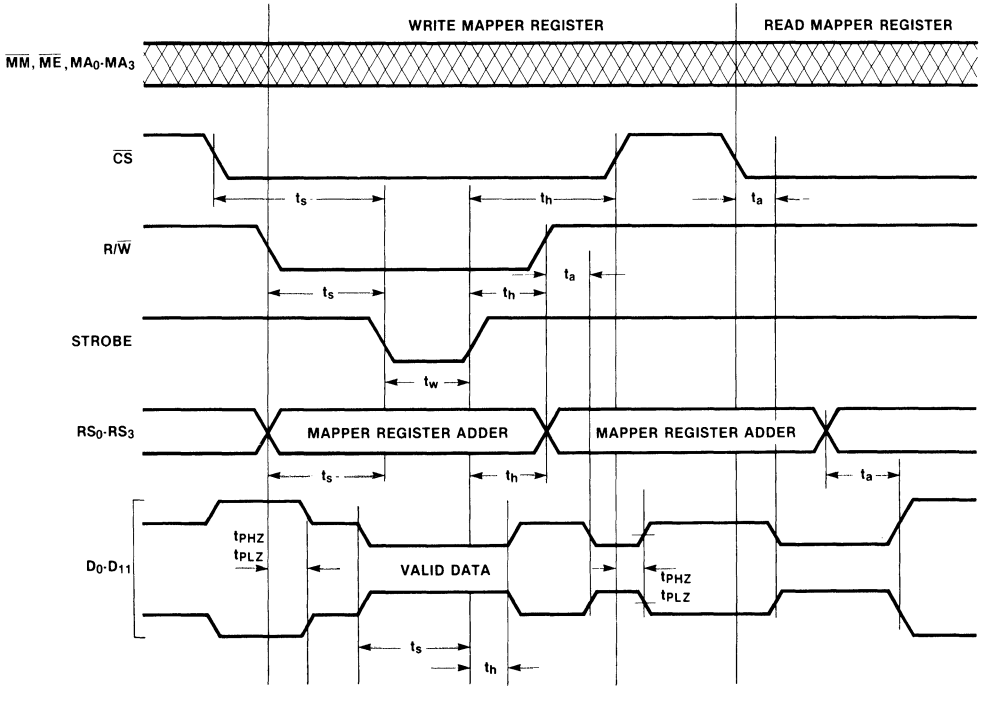


Fig. b Switching Characteristics



54F/74F620 • 54F/74F623

Inverting Octal Bus Transceiver With 3-State Outputs

Description

The 'F623 is an octal transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. The outputs are capable of sinking 64 mA and sourcing up to 15 mA, providing very good capacitive drive characteristics. The 'F620 is an inverting version of the 'F623.

These octal bus transceivers are designed for asynchronous two-way data flow between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs ($\overline{G}$BA and GAB).

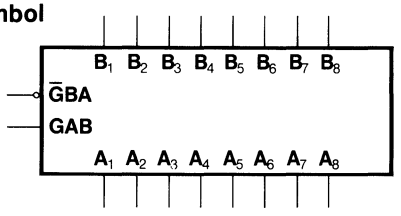
The enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives the 'F620 and 'F623 the capability to store data by simultaneous enabling of $\overline{G}$BA and GAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of the bus lines are at high impedance, both sets of bus lines (sixteen in all) will remain at their last states.

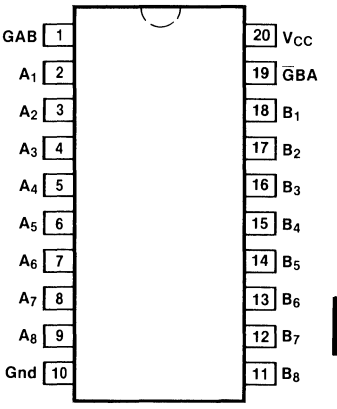
- **Octal Bidirectional Bus Interface**
- **3-State Buffer Outputs Sink 64 mA**
- **15 mA Source Current**
- **'F620 Inverting Option of 'F623**

Ordering Code: See Section 5

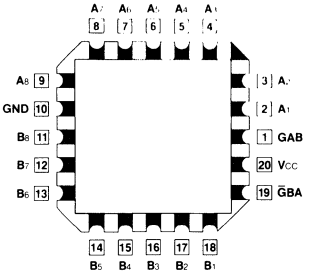
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

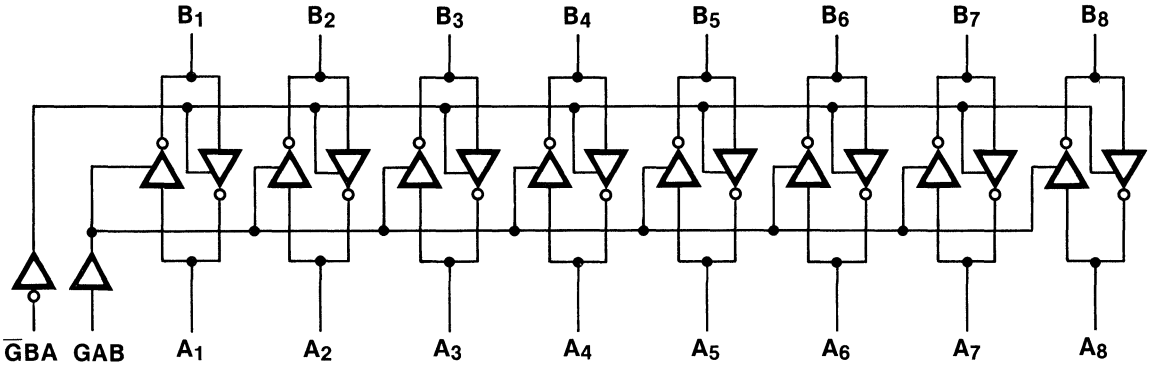
Pin Names	Description	54F/74F(U.L.) HIGH/LOW
$\overline{G}$BA,GAB	Enable Inputs	0.5/0.375
A_1-A_8	A Inputs or	1.75/0.406
	3-State Outputs	75/15 (12.5)
B_1-B_8	B Inputs or	1.75/0.406
	3-State Outputs	75/40(30)

Function Table

Enable Inputs		Operation	
$\overline{G}BA$	GAB	'F620	'F623
L	L	$\overline{B}$ data to A bus	B data to A bus
H	H	$\overline{A}$ data to B bus	A data to B bus
H	L	Z	Z
L	H	$\overline{B}$ data to A bus, A data to B bus	B data to A bus, $\overline{A}$ data to B bus

H = HIGH Voltage Level
L = LOW Voltage Level
Z = High Impedance

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current			143	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A Input to B Output ('F620)		8.0 9.0						ns	3-1 3-3
t_{PLH} t_{PHL}	Propagation Delay B Input to A Output ('F620)		8.0 9.0						ns	3-1 3-3
t_{PLH} t_{PHL}	Propagation Delay A Input to B Output ('F623)		6.5 7.0						ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay B Input to A Output ('F623)		6.5 7.0						ns	3-1 3-4
t_{PZH} t_{PZL}	Enable Time $\overline{G}$BA Input to A Output		8.0 11.0						ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Disable Time $\overline{G}$BA Input to A Output		7.5 6.0							
t_{PZH} t_{PZL}	Enable Time GAB Input to B Output		8.0 11.0						ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Disable Time GAB Input to B Output		7.5 6.0							

54F/74F630

16-Bit Error Detection and Correction Circuit With 3-State Outputs

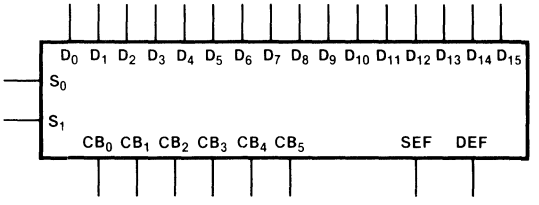
Description

The 'F630 is a 16-bit Error Detection And Correction (EDAC) circuit with 3-state outputs. It uses a modified Hamming code to generate a 6-bit check word from a 16-bit data word. This check word is stored along with the data word during the memory write cycle. During the memory read cycle, the 22-bit word from the memory is processed by the EDAC to determine if errors have occurred in memory.

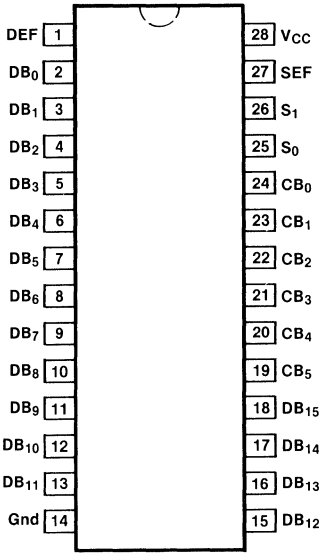
- **Detects and Corrects Single-bit Errors**
- **Detects and Flags Dual-bit Errors**
- **Fast Processing Times:**
  Write cycle: Generates check word in 20 ns typical
  Read cycle: Flags errors in 25 ns typical
- **Power Dissipation 600 mW typical**
- **3-State Outputs**

Ordering Code: See Section 5

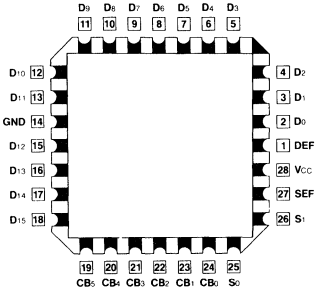
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
S_0, S_1	Control	0.5/0.375
CB_0-CB_{15}	Check Bits, Input	0.5/0.375
DB_0-DB_{15}	Data Bits, Input	0.5/0.375
CB_0-CB_{15}	Check Bits, Output	25/12.5
DB_0-DB_{15}	Data Bits, Output	25/12.5
SEF, DEF	Error Flags	25/12.5

Functional Description

The 'F630 is a 16-bit parallel error detection and correction circuit (EDAC) in a 28-pin, 600 mil package. It uses a modified Hamming code to generate a 6-bit check word from a 16-bit data word. This check word is stored along with the data word during the memory write cycle. During the memory read cycle, the 22-bit word from the memory is processed by the EDAC to determine if errors have occurred in memory.

Single-bit errors in the 16-bit data word are flagged and corrected.

Single-bit errors in the 6-bit check word are flagged, and the CPU sends the EDAC through the correction cycle even though the 16-bit word is not in error. The correction cycle will simply pass along the original 16-bit word in this case and produce error syndrome bits to pinpoint the error-generating location.

Dual-bit errors are flagged but not corrected. These dual errors may occur in any 2 bits of the 22-bit word from memory (two errors in the 16-bit data word, two errors in the 6-bit check word, or one error in each word).

The gross-error condition of all LOWs or all HIGHs from memory will be detected. Otherwise, errors in three or more bits of the 22-bit word are beyond the capabilities of these devices to detect.

In order to be able to determine whether the data from the memory is acceptable to use as presented to the bus, the EDAC must be strobed to enable the error flags; the flags will have to be tested for the zero condition.

The first case in the error function table represents the normal, no-error condition. The CPU sees LOWs on both flags. The next two cases of single-bit errors require data correction. Although the EDAC can discern the single check bit error and ignore it, the error flags are identical to the single error in the 16-bit data word. The CPU will ask for data correction in both cases. An interrupt condition to the CPU results in each of the last three cases, where dual errors occur.

During a memory write cycle, six check bits (CB_0-CB_5) are generated by eight input parity generators using the data bits as defined below. During a memory read cycle, the 6-bit check word is retrieved along with the actual data.

Error detection is accomplished as the 6-bit check word and the 16-bit data word from memory are applied to internal parity generators/checkers. If the parity of all six groupings of data and check bits is correct, it is assumed that no error has occurred and both error flags will be LOW. It should be noted that the sense of two of the check bits, CB_0 and CB_1, is inverted to ensure that the gross-error condition of all LOWs and all HIGHs is detected.

If the parity of one or more of the check groups is incorrect, an error has occurred and the proper error flag or flags will be set HIGH. Any single error in the 16-bit data word will change the sense of exactly 3-bits of the 6-bit check word. Any single error in the 6-bit check word changes the sense of only that one bit. In either case, the single-error flag will be set HIGH while the dual-error flag will remain LOW.

Any 2-bit error will change the sense of an even number of check bits. The 2-bit error is not correctable, since the parity tree can only identify single-bit errors. Both error flags are set HIGH when any 2-bit error is detected.

Three or more simultaneous bit errors can fool the EDAC into believing that no error, a correctable error, or an uncorrectable error has occurred and produce erroneous results in all three cases.

Error correction is accomplished by identifying the bad bit and inverting it. Identification of the erroneous bit is achieved by comparing the 16-bit data word and 6-bit check word from memory with the new check word with one (check word error) or three (data word error) inverted bits.

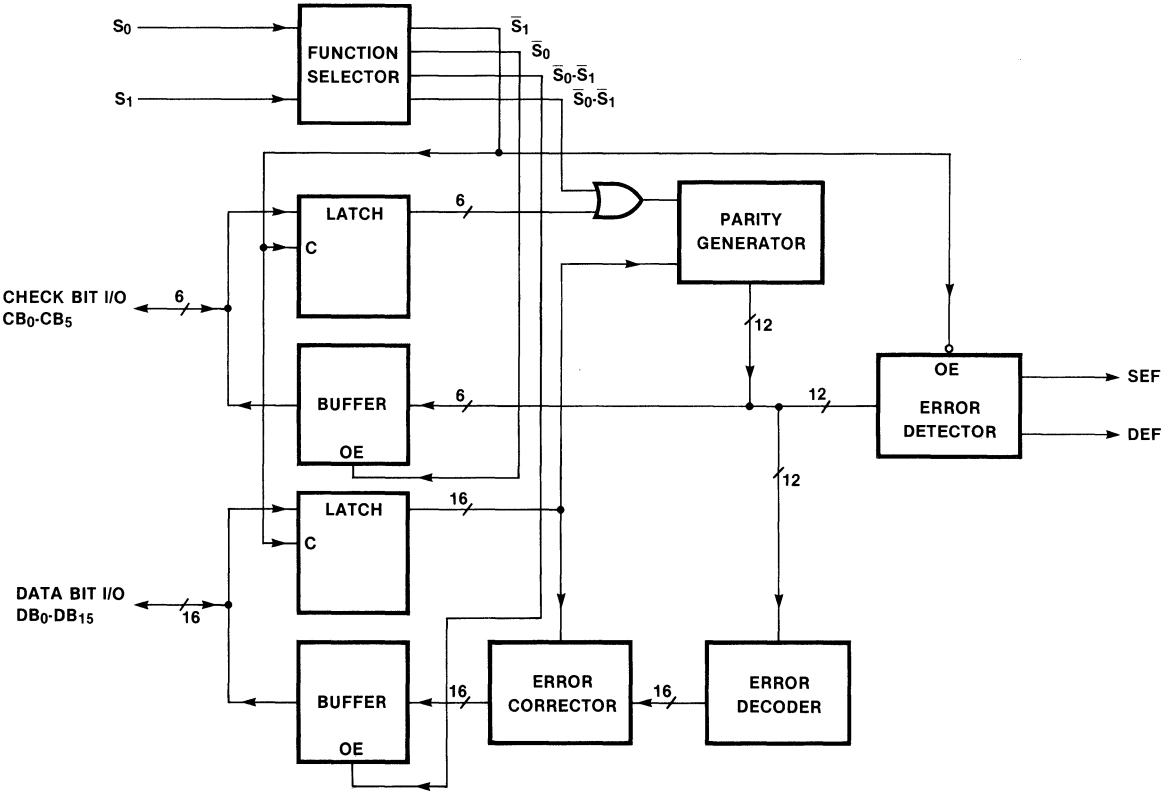
As the corrected word is made available on the data word I/O port, the check word I/O port presents a 6-bit syndrome error code. This syndrome code can be used to identify the bad memory chip.

Parity Algorithm

Check Word Bit	16-Bit Data Word															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CB_0	X	X		X	X				X	X	X			X		
CB_1	X		X	X		X	X		X			X			X	
CB_2		X	X		X	X		X		X			X			X
CB_3	X	X	X				X	X			X	X	X			
CB_4				X	X	X	X	X						X	X	X
CB_5									X	X	X	X	X	X	X	X

The six check bits are parity bits derived from the matrix of data bits as indicated by 'x' for each bit.

Block Diagram



Function Table

Total Number of Errors		Error Flags		Data Correction
16-Bit Data	6-Bit Checkword	SEF	DEF	
0	0	L	L	Not Applicable
1	0	H	L	Correction
0	1	H	L	Correction
1	1	H	H	Interrupt
2	0	H	H	Interrupt
0	2	H	H	Interrupt

H = HIGH Voltage Level
L = LOW Voltage Level

Error Syndrome Table

Error Location	Syndrome Error Code					
	CB_0	CB_1	CB_2	CB_3	CB_4	CB_5
DB_0	L	L	H	L	H	H
DB_1	L	H	L	L	H	H
DB_2	H	L	L	L	H	H
DB_3	L	L	H	H	L	H
DB_4	L	H	L	H	L	H
DB_5	H	L	L	H	L	H
DB_6	H	L	H	L	L	H
DB_7	H	H	L	L	L	H
DB_8	L	L	H	H	H	L
DB_9	L	H	L	H	H	L
DB_{10}	L	H	H	L	H	L
DB_{11}	H	L	H	L	H	L
DB_{12}	H	H	L	L	H	L
DB_{13}	L	H	H	H	L	L
DB_{14}	H	L	H	H	L	L
DB_{15}	H	H	L	H	L	L
CB_0	L	H	H	H	H	H
CB_1	H	L	H	H	H	H
CB_2	H	H	L	H	H	H
CB_3	H	H	H	L	H	H
CB_4	H	H	H	H	L	H
CB_5	H	H	H	H	H	L
No Error	H	H	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current				mA	V_{CC} = Max Outputs Open

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay DB to CB		25.0 18.0						ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay SI to DEF, SEF		16.0 11.0						ns	3-1 3-10
t_{PZH} t_{PZL}	Output Enable Time SO to CB or DB		12.0 12.0						ns	3-1, 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time SO to CB or DB		16.0 16.0						ns	3-1, 3-12 3-13

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C V_{CC} = +5.0 V			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
t_s(H) t_s(L)	Setup Time, HIGH or LOW CB or DB to SI	4.0 4.0							ns	3-1 3-5
t_h(H) t_h(L)	Hold Time, HIGH or LOW CB or DB to SI	4.0 4.0							ns	3-5

54F/74F632

32-Bit Parallel Error Detection and Correction Circuit

Description

The 'F632 device is a 32-bit parallel error detection and correction circuit (EDAC) in a 52-pin package. The EDAC uses a modified Hamming code to generate a 7-bit check word from a 32-bit data word. This check word is stored along with the data word during the memory write cycle. During the memory read cycle, the 39-bit words from memory are processed by the EDAC to determine if errors have occurred in memory.

Single-bit errors in the 32-bit data word are flagged and corrected.

Single-bit errors in the 7-bit check word are flagged, and the CPU sends the EDAC through the correction cycle even though the 32-bit data word is not in error. The correction cycle will simply pass along the original 32-bit data word in this case and produce error syndrome bits to pinpoint the error-generating location.

Dual-bit errors are flagged but not corrected. These errors may occur in any two bits of the 39-bit word from memory (two errors in the 32-bit data word, two errors in the 7-bit check word, or one error in each word). The gross-error condition of all LOWs or all HIGHs from memory will be detected. Otherwise, errors in three or more bits of the 39-bit word are beyond the capabilities of these devices to detect.

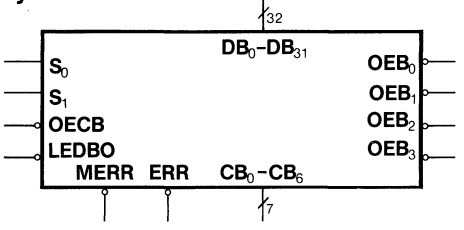
Read-modify-write (byte-control) operations can be performed by using output latch enable, $\overline{\text{LEDBO}}$, and the individual OEB_0 through OEB_3 byte control pins.

Diagnostics are performed on the EDACs by controls and internal paths that allow the user to read the contents of the Data Bit and Check Bit input latches. These will determine if the failure occurred in memory or in the EDAC.

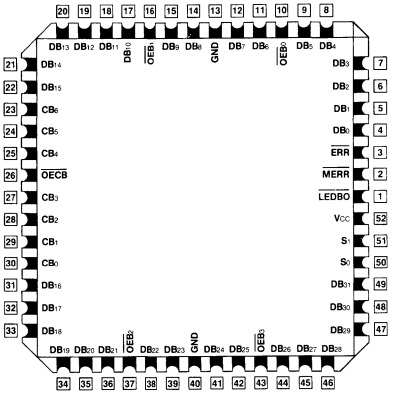
- **Detects and Corrects Single-Bit Errors**
- **Detects and Flags Dual-Bit Errors**
- **Built-In Diagnostic Capability**
- **Fast Write and Read Cycle Processing Times**
- **Byte-Write Capability**

Ordering Code: See Section 5

Logic Symbol



Connection Diagram



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
CB_0-CB_6	Check Word Bit, Input	0.5/0.375
	or 3-State Output	75/15(12.5)
DB_0-DB_{31}	Data Word Bit, Input	0.5/0.375
	or 3-State Output	75/15(12.5)
$\overline{OEB}_0$-$\overline{OEB}_3$	Output Enable Data Bit	0.5/0.375
$\overline{LEDBO}$	Output Latch Enable Data Bits	0.5/0.375
$\overline{OECB}$	Output Enable Check Bit	0.5/0.375
S_0, S_1	Select Pins	0.5/0.375
$\overline{ERR}$	Single Error Flag	25/12.5
$\overline{MERR}$	Multiple Error Flag	25/12.5

Functional Description

Memory Write Cycle Details

During a memory write cycle, the check bits (CB_0 through CB_6) are generated internally in the EDAC by seven 16-input parity generators using the 32-bit data word as defined in Table 2. These seven check bits are stored in memory along with the original 32-bit data word. This 32-bit word will later be used in the memory read cycle for error detection and correction.

Error Detection and Correction Details

During a memory read cycle, the 7-bit check word is retrieved along with the actual data. In order to be able to determine whether the data from memory is acceptable to use as presented to the bus, the error flags must be tested to determine if they are at the HIGH level.

The first case in Table 3 represents the normal, no-error conditions. The EDAC presents HIGHs on both flags. The next two cases of single-bit errors give a HIGH on $\overline{MERR}$ and a LOW on $\overline{ERR}$, which is the signal for a correctable error, and the EDAC should be sent through the correction cycle. The last three cases of double-bit errors will cause the EDAC to signal LOWs on both $\overline{ERR}$ and $\overline{MERR}$, which is the interrupt indication for the CPU.

Error detection is accomplished as the 7-bit check word and the 32-bit data word from memory are applied to internal parity generators/checkers. If the parity of all seven groupings of data and check bits are correct, it is assumed that no error has occurred and both error flags will be HIGH.

If the parity of one or more of the check groups is incorrect, an error has occurred and the proper error flag or flags will be set LOW. Any single error in the 32-bit data word will change the state of either three or five bits of the 7-bit check word. Any single error in the 7-bit check word changes the state of only that one bit. In either case, the single error flag ($\overline{ERR}$) will be set LOW while the dual error flag ($\overline{MERR}$) will remain HIGH.

Any 2-bit error will change the state of an even number of check bits. The 2-bit error is not correctable since the parity tree can only identify single-bit errors. Both error flags are set LOW when any 2-bit error is detected.

Three or more simultaneous bit errors can cause the EDAC to believe that no error, a correctable error, or an uncorrectable error has occurred and will produce erroneous results in all three cases. It should be noted that the gross-error conditions of all LOWs and all HIGHs will be detected.

As the corrected word is made available on the data I/O port (DB_0 through DB_{31}) the check word I/O port (CB_0 through CB_6) presents a 7-bit syndrome error code. This syndrome error code can be used to locate the bad memory chip. See Table 5 for syndrome decoding.

Read-Modify-Write (Byte Control) Operations

The 'F632 device is capable of byte-write operations. The 39-bit word from memory must first be latched into the Data Bit and Check Bit input latches. This is easily accomplished by switching from the read and flag mode ($S_1 = H$, $S_0 = L$) to the latch input mode ($S_1 = H$, $S_0 = H$). The EDAC will then make any corrections, if necessary, to the data word and place it at the input of the output data latch. This data word must then be latched into the output data latch by taking $\overline{LEDBO}$ from a LOW to a HIGH.

Byte control can now be employed on the data word through the $\overline{OEB}_0$ through $\overline{OEB}_3$ controls. $\overline{OEB}_0$ controls DB_0-DB_7 (byte 0), $\overline{OEB}_1$ controls DB_8-DB_{15} (byte 1), $\overline{OEB}_2$ controls DB_{16}-DB_{23} (byte 2), and $\overline{OEB}_3$ controls DB_{24}-DB_{31} (byte 3). Placing a HIGH on the byte control will disable the output and the user can modify the byte. If a LOW is placed on the byte control, then the original byte is allowed to pass onto the data bus unchanged. If the original data word is altered through byte control, a new check word must be generated before it is written back into memory. This is easily accomplished by taking control S_1 and S_0 LOW. Table 6 lists the read-modify-write functions.

Diagnostic Operations

The 'F632 is capable of diagnostics that allow the user to determine whether the EDAC or the memory is failing. The diagnostic function tables will help the user to see the possibilities for diagnostic control. In the diagnostic mode ($S_1 = L$, $S_0 = H$), the checkword is latched into the input latch while the data input latch remains transparent. This lets the user apply various data words against a fixed known checkword. If the user applies a diagnostic data word with an error in any bit location, the $\overline{ERR}$ flag should be LOW. If a diagnostic data word with two errors in any bit location is applied, the $\overline{MERR}$ flag should be LOW. After the checkword is latched into the input latch, it can be verified by taking $\overline{OECB}$ LOW. This outputs the latched checkword. The diagnostic data word can be latched into the output data latch and verified. By changing from the diagnostic mode ($S_1 = L$, $S_0 = H$) to the correction mode ($S_1 = H$, $S_0 = H$), the user can verify that the EDAC will correct the diagnostic data word. Also, the syndrome bits can be produced to verify that the EDAC pinpoints the error location. Table 7 lists the diagnostic functions.

Block Diagram

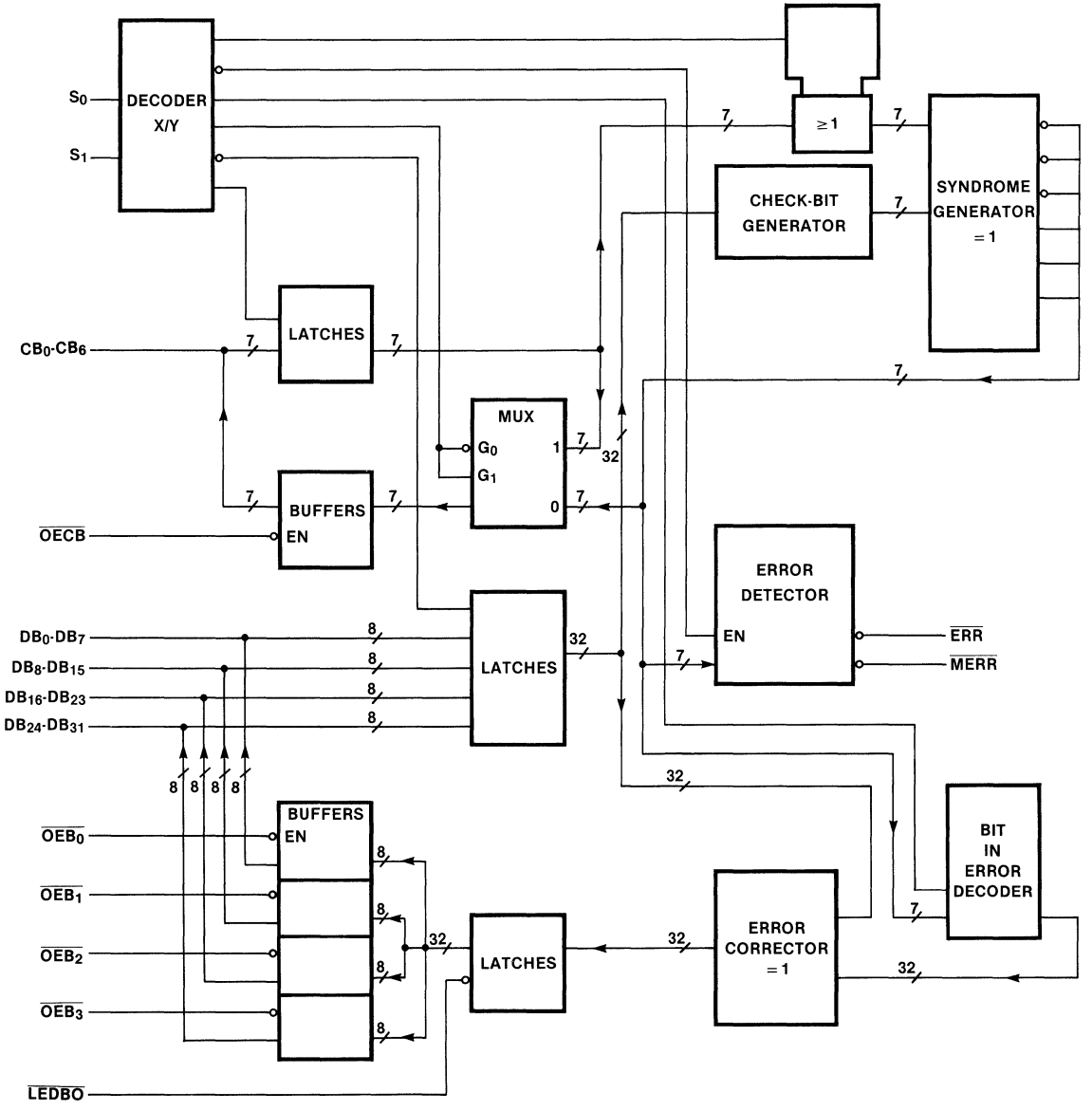


Table 1 Write Control Function

Memory Cycle	EDAC Function	Control S_1 S_0	Data I/O	DB Control $\overline{OEB_n}$	DP Output Latch $\overline{LEDBO}$	Check I/O	CB Control $\overline{OECB}$	Error Flags $\overline{ERR}$ $\overline{MERR}$
Write	Generate Check Word	L L	Input	H	X	Output Check Bit	L	H H

Table 2 Parity Algorithm

Check Word Bit	32-Bit Data Word																													
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CB_0	X		X	X		X					X		X	X	X			X			X		X	X	X	X		X			X
CB_1				X		X		X		X		X		X	X	X				X		X		X		X		X	X	X
CB_2	X		X			X	X		X			X	X			X	X		X				X	X		X		X	X		X
CB_3			X	X	X				X	X	X				X	X			X	X	X				X	X	X			X	X
CB_4		X	X							X	X	X	X	X	X			X	X							X	X	X	X	X	
CB_5				X	X	X	X	X	X	X	X									X	X	X	X	X	X	X	X				
CB_6	X	X	X	X	X	X	X	X																	X	X	X	X	X	X	X	X

The seven check bits are parity bits derived from the matrix of data bits as indicated by 'X' for each bit.

Table 3 Error Function

Total Number of Errors		Error Flags		Data Correction
32-Bit Data Word	7-Bit Check Word	$\overline{ERR}$	$\overline{MERR}$	
0	0	H	H	Not applicable
1	0	L	H	Correction
0	1	L	H	Correction
1	1	L	L	Interrupt
2	0	L	L	Interrupt
0	2	L	L	Interrupt

H = HIGH Voltage Level
L = LOW Voltage Level

Table 4 Read, Flag, and Correct Function

Memory Cycle	EDAC Function	Control S_1 S_0	Data I/O	DB Control OEB_n	DB Output Latch $\overline{LEDBO}$	Check I/O	CB Control $\overline{OECB}$	Error Flags $\overline{ERR}$ $\overline{MERR}$
Read	Read & Flag	H L	Input	H	X	Input	H	Enabled[1]
Read	Latch Input Data & Check Bits	H H	Latched Input Data	H	L	Latched Input Check Word	H	Enabled[1]
Read	Output Corrected Data & Syndrome	H H	Output Corrected Data Word	L	X	Output Syndrome Bits[2]	L	Enabled[1]

1. See Table 3 for error description. 2. See Table 5 for error location.

Table 5 Syndrome Decoding

Syndrome Bits							Error
6	5	4	3	2	1	0	
L	L	L	L	L	L	L	unc
L	L	L	L	L	L	H	2-bit
L	L	L	L	L	H	L	2-bit
L	L	L	L	L	H	H	unc
L	L	L	L	H	L	L	2-bit
L	L	L	L	H	L	H	unc
L	L	L	L	H	H	L	unc
L	L	L	L	H	H	H	2-bit
L	L	L	H	L	L	L	2-bit
L	L	L	H	L	L	H	unc
L	L	L	H	L	H	L	DB_{31}
L	L	L	H	L	H	H	2-bit
L	L	L	H	H	L	L	unc
L	L	L	H	H	L	H	2-bit
L	L	L	H	H	H	L	2-bit
L	L	L	H	H	H	H	DB_{30}
L	L	H	L	L	L	L	2-bit
L	L	H	L	L	L	H	unc
L	L	H	L	L	H	L	DB_{29}
L	L	H	L	L	H	H	2-bit
L	L	H	L	H	L	L	DB_{28}
L	L	H	L	H	L	H	2-bit
L	L	H	L	H	H	L	2-bit
L	L	H	L	H	H	H	DB_{27}
L	L	H	H	L	L	L	DB_{26}
L	L	H	H	L	L	H	2-bit
L	L	H	H	L	H	L	2-bit
L	L	H	H	L	H	H	DB_{25}
L	L	H	H	H	L	L	2-bit
L	L	H	H	H	L	H	DB_{24}
L	L	H	H	H	H	L	unc
L	L	H	H	H	H	H	2-bit
H	H	L	L	L	L	L	unc
H	H	L	L	L	L	H	2-bit
H	H	L	L	L	H	L	2-bit
H	H	L	L	L	H	H	DB_{23}
H	H	L	L	H	L	L	2-bit
H	H	L	L	H	L	H	DB_{22}
H	H	L	L	H	H	L	DB_{21}
H	H	L	L	H	H	H	2-bit
H	H	L	H	L	L	L	2-bit
H	H	L	H	L	L	H	DB_{20}
H	H	L	H	L	H	L	DB_{19}
H	H	L	H	L	H	H	2-bit
H	H	L	H	H	L	L	DB_{18}
H	H	L	H	H	L	H	2-bit
H	H	L	H	H	H	L	2-bit
H	H	L	H	H	H	H	CB_4
H	H	H	L	L	L	L	2-bit
H	H	H	L	L	L	H	DB_{16}
H	H	H	L	L	H	L	unc
H	H	H	L	L	H	H	2-bit
H	H	H	L	H	L	L	DB_{17}
H	H	H	L	H	L	H	2-bit
H	H	H	L	H	H	L	2-bit
H	H	H	L	H	H	H	CB_3
H	H	H	H	L	L	L	unc
H	H	H	H	L	L	H	2-bit
H	H	H	H	L	H	L	2-bit
H	H	H	H	L	H	H	CB_2
H	H	H	H	H	L	L	2-bit
H	H	H	H	H	L	H	CB_1
H	H	H	H	H	H	L	CB_0
H	H	H	H	H	H	H	none

CB_X = error in check bit X
DB_Y = error in data bit Y
2-bit = double-bit error
unc = uncorrectable multibit error

Table 5 (cont'd) Syndrome Decoding

Syndrome Bits							Error
6	5	4	3	2	1	0	
H	L	L	L	L	L	L	2-bit
H	L	L	L	L	L	H	unc
H	L	L	L	L	H	L	unc
H	L	L	L	L	H	H	2-bit
H	L	L	L	H	L	L	unc
H	L	L	L	H	L	H	2-bit
H	L	L	L	H	H	L	2-bit
H	L	L	L	H	H	H	unc
H	L	L	H	L	L	L	unc
H	L	L	H	L	L	H	2-bit
H	L	L	H	L	H	L	2-bit
H	L	L	H	L	H	H	DB_{15}
H	L	L	H	H	L	L	2-bit
H	L	L	H	H	L	H	unc
H	L	L	H	H	H	L	DB_{14}
H	L	L	H	H	H	H	2-bit
H	L	H	L	L	L	L	unc
H	L	H	L	L	L	H	2-bit
H	L	H	L	L	H	L	2-bit
H	L	H	L	L	H	H	DB_{13}
H	L	H	L	H	L	L	2-bit
H	L	H	L	H	L	H	DB_{12}
H	L	H	L	H	H	L	DB_{11}
H	L	H	L	H	H	H	2-bit
H	L	H	H	L	L	L	2-bit
H	L	H	H	L	L	H	DB_{10}
H	L	H	H	L	H	L	DB_9
H	L	H	H	L	H	H	2-bit
H	L	H	H	H	L	L	DB_8
H	L	H	H	H	L	H	2-bit
H	L	H	H	H	H	L	2-bit
H	L	H	H	H	H	H	CB_5

Syndrome Bits							Error
6	5	4	3	2	1	0	
L	H	L	L	L	L	L	2-bit
L	H	L	L	L	L	H	unc
L	H	L	L	L	H	L	DB_7
L	H	L	L	L	H	H	2-bit
L	H	L	L	H	L	L	DB_6
L	H	L	L	H	L	H	2-bit
L	H	L	L	H	H	L	2-bit
L	H	L	L	H	H	H	DB_5
L	H	L	H	L	L	L	DB_4
L	H	L	H	L	L	H	2-bit
L	H	L	H	L	H	L	2-bit
L	H	L	H	L	H	H	DB_3
L	H	L	H	H	L	L	2-bit
L	H	L	H	H	L	H	DB_2
L	H	L	H	H	H	L	unc
L	H	L	H	H	H	H	2-bit
L	H	H	L	L	L	L	DB_0
L	H	H	L	L	L	H	2-bit
L	H	H	L	L	H	L	2-bit
L	H	H	L	L	H	H	unc
L	H	H	L	H	L	L	2-bit
L	H	H	L	H	L	H	DB_1
L	H	H	L	H	H	L	unc
L	H	H	L	H	H	H	2-bit
L	H	H	H	L	L	L	2-bit
L	H	H	H	L	L	H	unc
L	H	H	H	L	H	L	unc
L	H	H	H	L	H	H	2-bit
L	H	H	H	H	L	L	unc
L	H	H	H	H	L	H	2-bit
L	H	H	H	H	H	L	2-bit
L	H	H	H	H	H	H	CB_6

CC_X = error in check bit X
DB_Y = error in data bit Y
2-bit = double-bit error
unc = uncorrectable multibit error

Table 6 Read-Modify-Write Function

Memory Cycle	EDAC Function	Control S_1	Control S_0	$BYTE_n$*	OEB_n*	DB Output Latch $\overline{LEDBO}$	Check I/O	CB Control $\overline{OECB}$	Error Flags $\overline{ERR}$	Error Flags $\overline{MERR}$
Read	Read & Flag	H	L	Input	H	X	Input	H	Enabled	
Read	Latch Input Data & Check Bits	H	H	Latched Input Data	H	L	Latched Input Check Word	H	Enabled	
Read	Latch Corrected Data Word into Output Latch	H	H	Latched Output Data Word	H	H	High Z	H	Enabled	
							Output Syndrome Bits	L		
Modify/ Write	Modify Appropriate Byte or Bytes & Generate New Check Word	L	L	Input Modified $BYTE_0$	H	H	Output Check Word	L	H	H
				Output Unchanged $BYTE_0$	L					

* $\overline{OEB}_0$ controls DB_0-DB_7 ($BYTE_0$), $\overline{OEB}_1$ controls DB_8-DB_{15} ($BYTE_1$), $\overline{OEB}_2$ controls DB_{16}-DB_{23} ($BYTE_2$), $\overline{OEB}_3$ controls DB_{24}-DB_{31} ($BYTE_3$).

Table 7 Diagnostic Function

EDAC Function	Control S_1 S_0	DATA I/O	DB Byte Control $\overline{OEB_n}$	DB Output Latch $\overline{LEDBO}$	Check I/O	CB Control $\overline{OECB}$	Error Flags $\overline{ERR}$ $\overline{MERR}$
Read & flag	H L	Input Correct Data Word	H	X	Input Correct Check Bits	H	H H
Latch Input Check Word while Data Input Latch Remains Transparent	L H	Input Diagnostic Data Word*	H	L	Latched Input Check Bits	H	Enabled
Latch Diagnostic Data Word into Output Latch	L H	Input Diagnostic Data Word*	H	H	Output Latched Check Bits	L	Enabled
					High Z	H	
Latch Diagnostic Data Word into Input Latch	H H	Latched Input Diagnostic Data Word	H	H	Output Syndrome Bits	L	Enabled
					High Z	H	
Output Diagnostic Data Word & Syndrome Bits	H H	Output Diagnostic Data Word	L	H	Output Syndrome Bits	L	Enabled
					High Z	H	
Output Corrected Diagnostic Data Word & Output Syndrome Bits	H H	Output Corrected Diagnostic Data Word	L	L	Output Syndrome Bits	L	Enabled
					High Z	H	

*Diagnostic data is a data word with an error in one bit location except when testing the $\overline{MERR}$ error flag. In this case, the diagnostic data word will contain errors in two bit locations.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		200	260	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F	54F	74F	Units
		$T_A = +25°C$ $V_{CC} = +5.0\,V$ $C_L = 50\,pF$	T_A, V_{CC} = Mil $C_L = 50\,pF$	T_A, V_{CC} = Com $C_L = 50\,pF$	
		Min Typ Max	Min Max	Min Max	
t_{PLH} t_{PHL}	Propagation Delay DB or CB to $\overline{ERR}$	30.0 30.0			ns
t_{PLH} t_{PHL}	Propagation Delay DB to $\overline{ERR}$	30.0 30.0			ns
t_{PLH} t_{PHL}	Propagation Delay DB or CB to $\overline{MERR}$	35.0 35.0			ns
t_{PLH} t_{PHL}	Propagation Delay DB to $\overline{MERR}$	35.0 35.0			ns
t_{PHL}	Propagation Delay S_0 or S_1 LOW to CB	38.0 38.0			ns
t_{PLH} t_{PHL}	Propagation Delay DB to CB	30.0 30.0			ns
t_{PHL}	Propagation Delay $\overline{LEDBO}$ to DB	23.0 23.0			ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEB}_n$ to DB	7.5 9.0			ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEB}_n$ to DB	7.5 9.0			ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OECB}$ to CB	7.5 9.0			ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OECB}$ to CB	7.5 9.0			ns

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com	
		Min Typ Max	Min Max	Min Max	
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW DB before SO HIGH	0 0			ns
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW SO HIGH before LEDBO HIGH	15.0 15.0			ns
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW LEDBO HIGH before S_0 or S_1 LOW	0 0			ns
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW LEDBO HIGH before S_1 HIGH	0 0			ns
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW Diagnostic DB before S_1 HIGH	0 0			ns
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW Diagnostic CB before S_1 LOW or S_0 HIGH	0 0			ns
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW Diagnostic DB before LEDBO HIGH	15.0 15.0			ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW S_0 LOW and S_1 HIGH	6.0 6.0			ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW DB and CB hold after S_0 HIGH	10.0 10.0			ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW DB hold after S_1 HIGH	10.0 10.0			ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW CB hold after S_1 LOW or S_0 HIGH	10.0 10.0			ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW Diagnostic DB after LEDBO HIGH	0 0			ns

54F/74F646 • 54F/74F648

Octal Transceiver/Register With 3-State Outputs

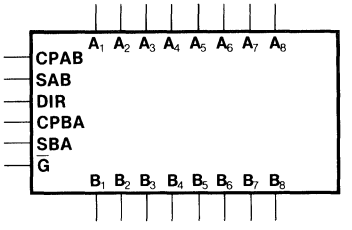
Description

These devices consist of bus transceiver circuits with 3-state or open-collector outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a high logic level. Control $\overline{G}$ and direction pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or the B register or in both. The select controls can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when the enable control $\overline{G}$ is Active LOW. In the isolation mode (control $\overline{G}$ HIGH), A data may be stored in the B register and/or B data may be stored in the A register.

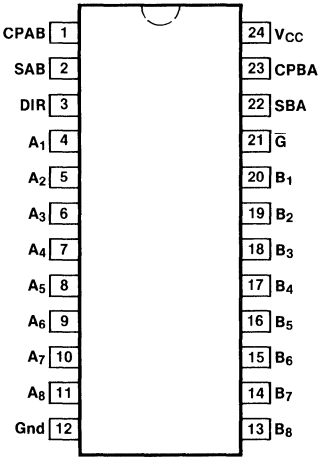
- **Independent Registers for A and B Buses**
- **Multiplexed Real-Time and Stored Data**
- **Choice of True and Inverting Data Paths**
- **3-State Outputs**
- **300 mil Slim Package**

Ordering Code: See Section 5

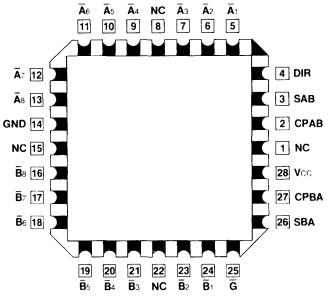
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC

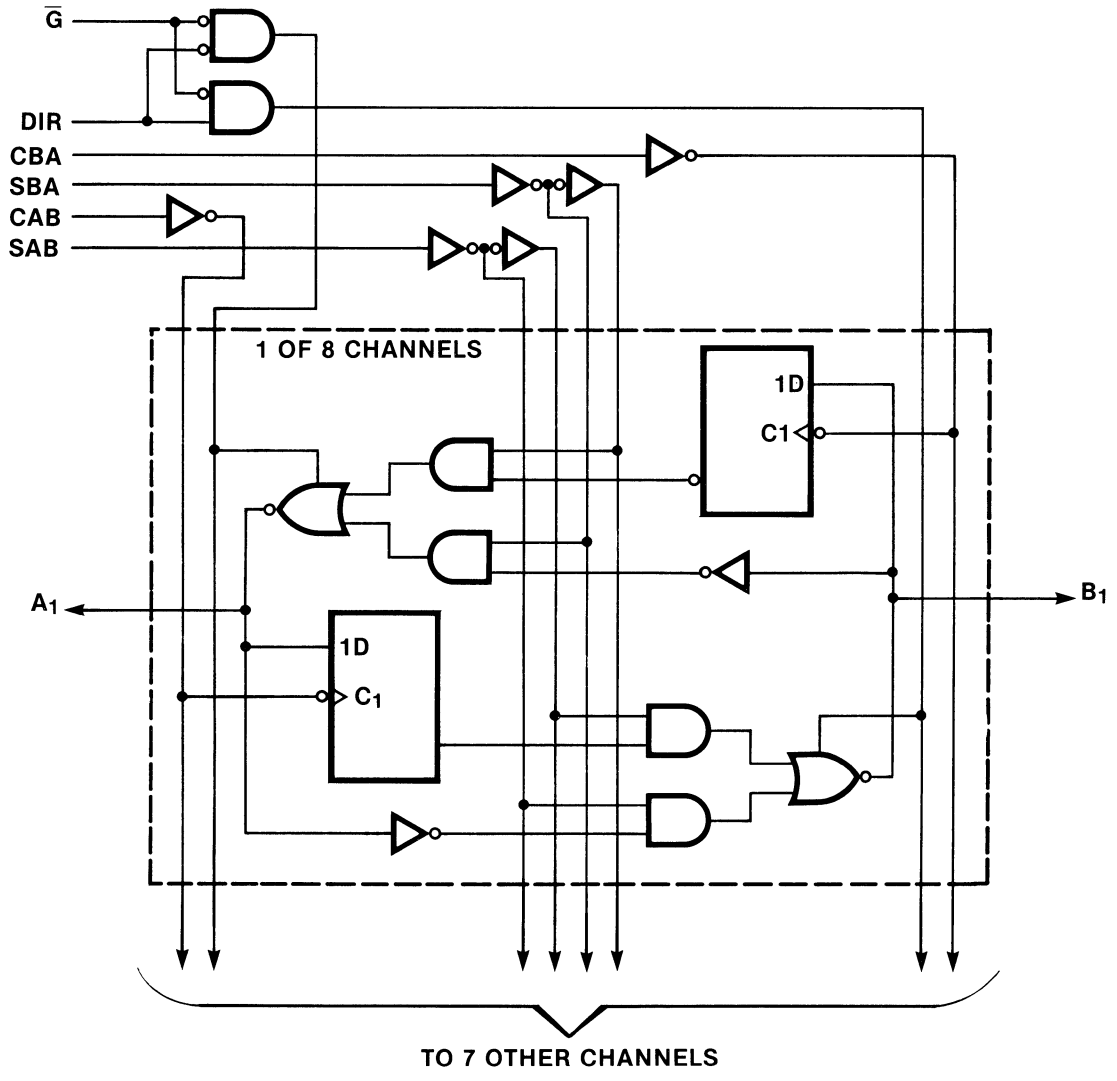


Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
A_1-A_8	Data Register Inputs	0.5/0.375
	Data Register A Outputs	75/15 (12.5)
B_1-B_8	Data Register B Inputs	0.5/0.375
	Data Register B Outputs	75/40 (30)
CPAB, CPBA	Clock Pulse Inputs	0.5/0.375
SAB, SBA	Transmit/Receive Inputs	0.5/0.375
DIR,$\overline{G}$	Output Enable Inputs	1.0/0.75

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Function Table

Inputs						Data I/O*		Operation or Function	
$\overline{G}$	DIR	CPAB	CPBA	SAB	SBA	A_1-A_8	B_1-B_8	'646	'648
H	X	H or L	H or L	X	X	Input	Input	Isolation	Isolation
H	X	↑	↑	X	X			Store A and B Data	Store A and B Data
L	L	X	X	X	L	Output	Input	Real Time B Data to A Bus	Real Time $\overline{B}$ Data to A Bus
L	L	X	X	X	H			Stored B Data to A Bus	Stored $\overline{B}$ Data to A Bus
L	H	X	X	L	X	Input	Output	Real Time A Data to B Bus	Real Time $\overline{A}$ Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus	Stored $\overline{A}$ Data to B Bus

*The data output functions may be enabled or disabled by various signals at the G and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the clock inputs.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Irrelevant
↑ = LOW-to-HIGH Transition

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current				mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$	T_A, V_{CC} = Mil $C_L = 50\ pF$	T_A, V_{CC} = Com $C_L = 50\ pF$		
		Min Typ Max	Min Max	Min Max		
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus	13.0 13.0			ns	3-1 3-7
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	11.0 11.0			ns	3-1, 3-3 3-4
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to A or B	13.0 13.0			ns	3-1, 3-3 3-4
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to A or B	13.0 13.0			ns	3-1, 3-3 3-4
t_{PZH} t_{PZL}	Enable to Bus	12.5 12.5			ns	3-1 3-12 3-13
t_{PZH} t_{PZL}	Direction to Bus DIR to A or B	12.5 12.5				
t_{PHZ} t_{PLZ}	Enable to Bus	10.5 10.5			ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Direction to Bus	10.5 10.5				

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW Bus to Clock	3.0 3.0			ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW Bus to Clock	1.0 1.0			ns	3-5
$t_w(H)$ $t_w(L)$	Clock Pulse Width HIGH or LOW	4.0 4.0			ns	3-7

54F/74F655 • 54F/74F656

Octal Buffer/Line Driver with Parity With 3-State Outputs

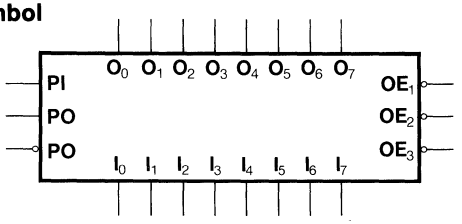
Description

The 'F655 and 'F656 are octal buffers and line drivers with parity generating and checking designed to be employed as memory address drivers, clock drivers and bus-oriented transmitters/receivers. These parts include parity generator/checker to improve PC board density.

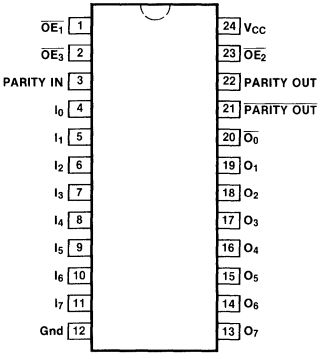
- **Inverting ('F655) or Non-Inverting ('F656) Outputs**
- **300 mil 24-Pin Plastic Slim Package**
- **'F655 Combines 'F240 and 'F280 Functions in One Package**
- **'F656 Combines 'F241 and 'F280 Functions in One Package**
- **Inputs on One Side and Outputs on the Other Side to Simplify PC Board Layout**
- **3-State Outputs**

Ordering Code: See Section 5

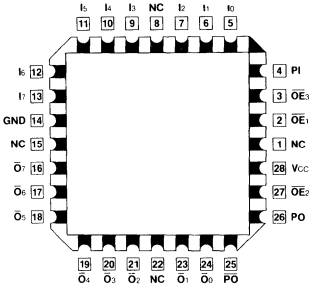
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

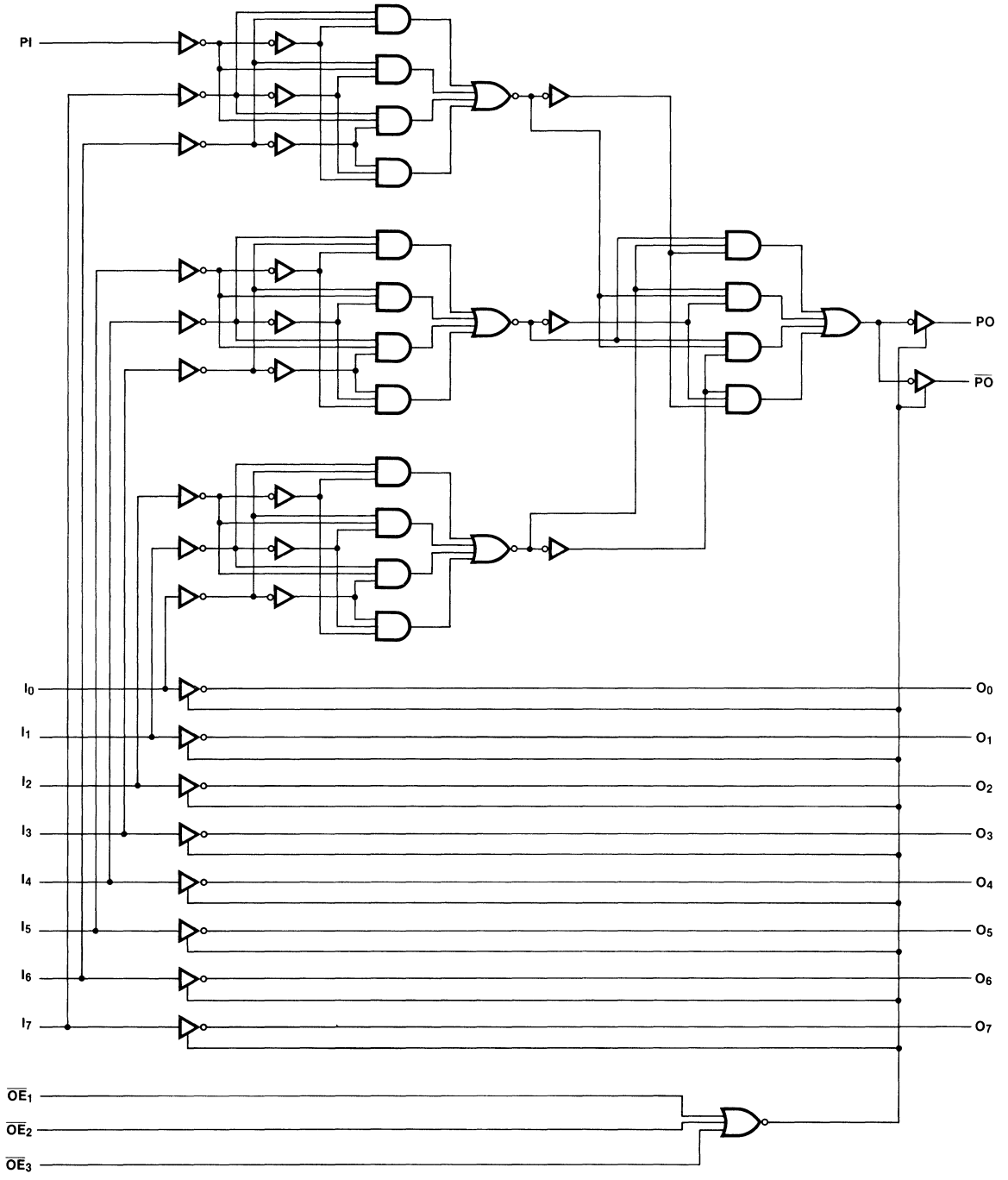
Pin Names	Description	54F/74F(U.L.) HIGH/LOW
I_0-I_7	Input	0.5/0.375
$\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$	Enable Input, 3-State Output (Active LOW)	0.5/0.375
PI	Parity Input	0.5/0.375
PO, $\overline{PO}$	Parity Output	75/40 (30)
O_0-O_7	Output	75/40 (30)

Function Table

Inputs				Output	
$\overline{OE}_1$	$\overline{OE}_2$	$\overline{OE}_3$	D	'F655	'F656
L	L	L	L	H	L
L	L	L	H	L	H
H	H	H	X	Z	Z

H = HIGH Voltage Level
L = LOW Voltage Level
Z = High Impedance

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions	
		Min	Typ	Max			
I_{CCH}	Power Supply Current		45	70	mA	Outputs HIGH	V_{CC} = Max
I_{CCL}			65	105		Outputs LOW	
I_{CCZ}			55	95		Outputs OFF	

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output ('F655)		11.5 5.0						ns	3-1 3-7 3-8
t_{PLH} t_{PHL}	Propagation Delay Data to Output ('F656)		6.5 9.5							
t_{PLH} t_{PHL}	Propagation Delay Data to Parity Outputs ('F655)		13.0 14.5						ns	3-1 3-7 3-8
t_{PLH} t_{PHL}	Propagation Delay Data to Parity Outputs ('F656)		13.0 15.0							
t_{PZH} t_{PZL}	Enable Time HIGH or LOW ('F655)		16.5 19.5						ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Disable Time HIGH or LOW ('F655)		9.0 8.5							
t_{PZH} t_{PZL}	Enable Time HIGH or LOW ('F656)		17.5 18.5						ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Disable Time HIGH or LOW ('F656)		6.5 7.5							

54F/74F657

Octal Bidirectional Transceiver With 8-Bit Parity Generator/Checker and 3-State Outputs

Description

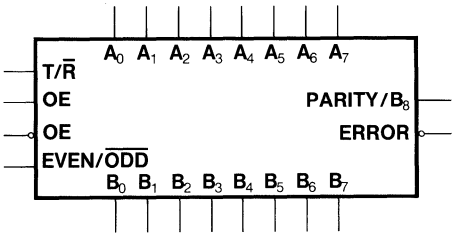
The 'F657 contains eight non-inverting buffers with 3-state outputs and an 8-bit parity generator/checker, and is intended for bus-oriented applications. The buffers have a guaranteed current sinking capability of 20 mA at the A ports and 64 mA at the B ports. The Transmit/Receive ($T/\overline{R}$) input determines the direction of the data flow through the bidirectional transceivers. Transmit (active HIGH) enables data from A ports to B ports; Receive (Active LOW) enables data from B ports to A ports. The Output Enable inputs disable both the A and B ports by placing them in a High Z condition when either the $\overline{OE}$ input is HIGH or the $\overline{OE}$ input is LOW.

The parity generator detects whether an even or odd number of bits on the A ports is HIGH, depending on the condition of the Even/$\overline{Odd}$ input. If the Even input is active HIGH and an even number of A inputs is HIGH, the Parity output is HIGH. The parity of the data received on the B ports is compared with the Even/$\overline{Odd}$ input and the Error output is LOW if not equal.

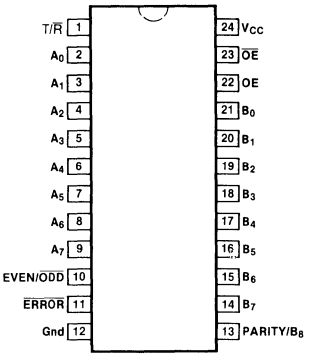
- **300 mil 24-Pin Plastic Slim Package**
- **Combines 'F245 and 'F280A Functions in One Package**
- **3-State Outputs**
- **Outputs Sink 64 mA**
- **15 mA Source Current**
- **Input Diodes for Termination Effects**

Ordering Code: See Section 5

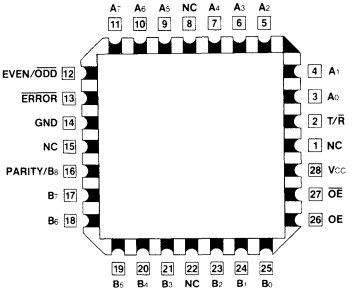
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
A_0-A_7	Data Inputs	0.5/0.375
	Data Outputs	25/12.5
B_0-B_7	Data Inputs	0.5/0.375
	Data Outputs	25/12.5
T/$\overline{R}$	Transmit/Receive Input	0.5/0.375
$\overline{OE}$, OE	Enable Outputs	0.5/0.375
PARITY/B_8	Parity	25/12.5
E/O	Even/Odd	0.5/0.375
ERROR	Error	0.5/0.375

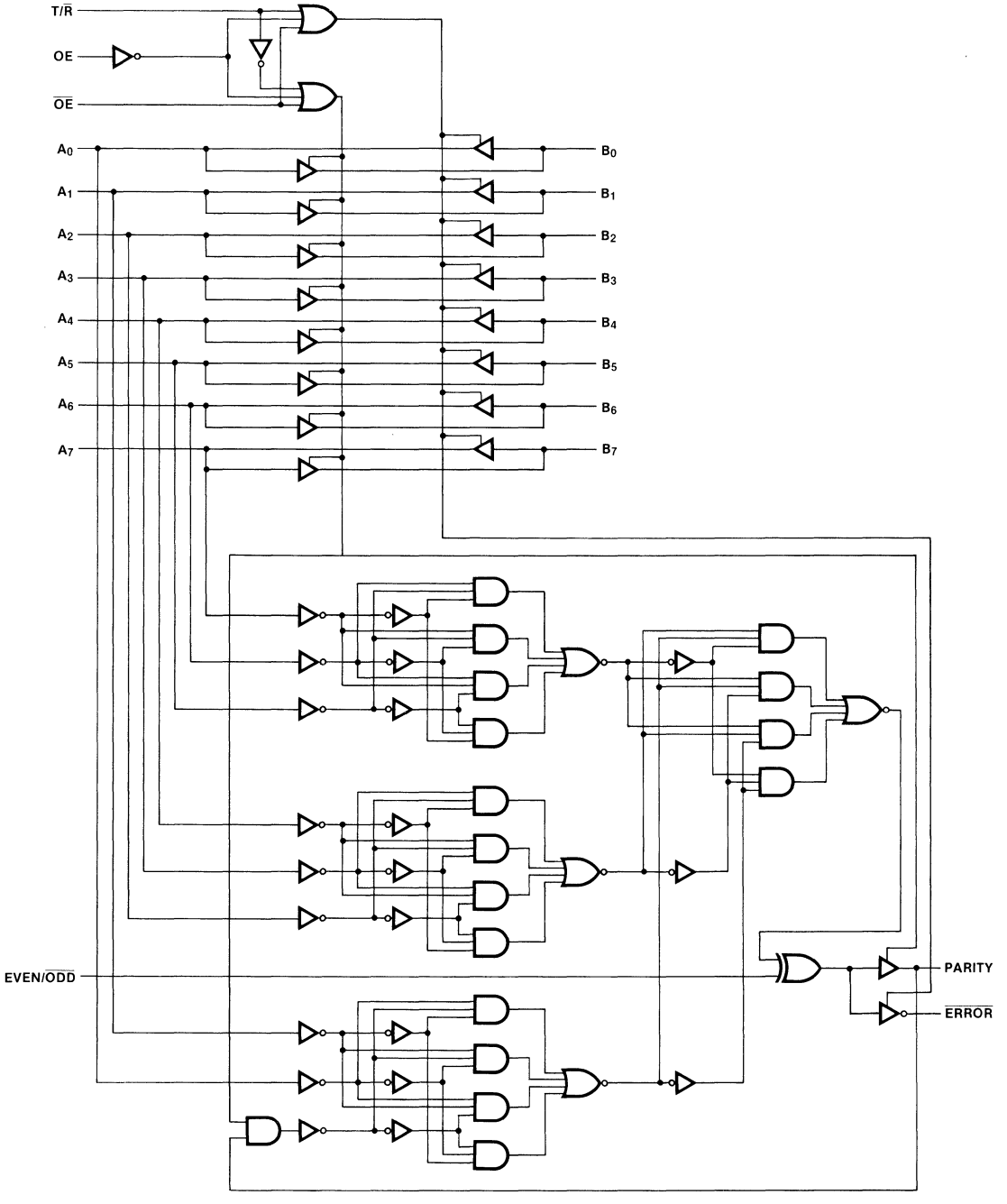
Function Table

Inputs		Output
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Number of HIGH Inputs I_0-I_8	Parity	
	Even	Odd
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		120	165	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF	T_A, V_{CC} = Mil, C_L = 50 pF	T_A, V_{CC} = Com, C_L = 50 pF		
		Min Typ Max	Min Max	Min Max		
t_{PLH} t_{PHL}	Propagation Delay A_n to B_n or B_n to A_n	5.5 6.0			ns	3-1 3-7 3-8
t_{PLH} t_{PHL}	Propagation Delay A_n to Parity	14.0 15.5				
t_{PZH} t_{PZL}	Output Enable Time	7.0 10.0			ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time	6.5 5.0				

54F/74F673A

16-Bit Serial-In, Serial/Parallel-Out Shift Register

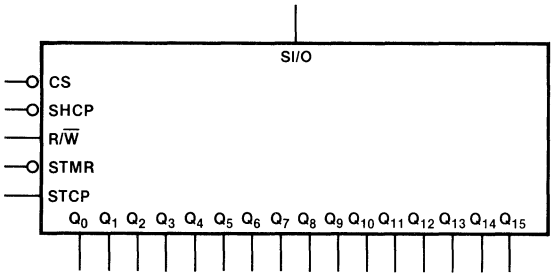
Description

The 'F673A contains a 16-bit serial-in, serial-out shift register and a 16-bit parallel-out storage register. A single pin serves either as an input for serial entry or as a 3-state serial output. In the Serial-out mode, the data recirculates in the shift register. By means of a separate clock, The contents of the shift register are transferred to the storage register for parallel outputting. The contents of the storage register can also be parallel loaded back into the shift register. A HIGH signal on the Chip Select input prevents both shifting and parallel transfer. The storage register may be cleared via $\overline{STMR}$.

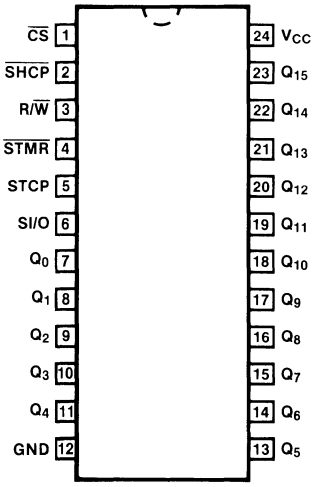
- **Serial-to-Parallel Converter**
- **16-Bit Serial I/O Shift Register**
- **16-Bit Parallel-Out Storage Register**
- **Recirculating Serial Shifting**
- **Recirculating Parallel Transfer**
- **Common Serial Data I/O Pin**
- **Slim 24 Lead Package**

Ordering Code: See Section 5

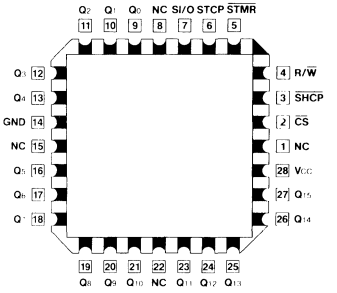
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
$\overline{CS}$	Chip Select Input (Active LOW)	0.5/0.375
$\overline{SHCP}$	Shift Clock Pulse Input (Active Falling Edge)	0.5/0.375
$\overline{STMR}$	Store Master Reset Input (Active LOW)	0.5/0.375
STCP	Store Clock Pulse Input	0.5/0.375
R/$\overline{W}$	Read/Write Input	0.5/0.375
SI/O	Serial Data Input or	1.75/0.375
	3-State Serial Output	75/15 (12.5)
Q_0-Q_{15}	Parallel Data Outputs	25/12.5

Functional Description

The 16-bit shift register operates in one of four modes, as indicated in the Shift Register Operations Table. A HIGH signal on the Chip Select ($\overline{CS}$) input prevents clocking and forces the Serial Input/Output (SI/O) 3-state buffer into the high impedance state. During serial shift-out operations, the SI/O buffer is active (i.e., enabled) and the output data is also recirculated back into the shift register. When parallel loading the shift register from the storage register, serial shifting is inhibited.

The storage register has an asynchronous master reset ($\overline{STMR}$) input that overrides all other inputs and forces the Q_0-Q_{15} outputs LOW. The storage register is in the Hold mode when either $\overline{CS}$ or the Read/Write (R/$\overline{W}$) input is HIGH. With $\overline{CS}$ and R/$\overline{W}$ both LOW, the storage register is parallel loaded from the shift register.

Shift Register Operations Table

Control Inputs				SI/O Status	Operating Mode
$\overline{CS}$	R/$\overline{W}$	$\overline{SHCP}$	STCP		
H	X	X	X	High Z	Hold
L	L		X	Data In	Serial Load
L	H	↓	L	Data Out	Serial Output with Recirculation
L	H	↓	H	Active	Parallel Load; No Shifting

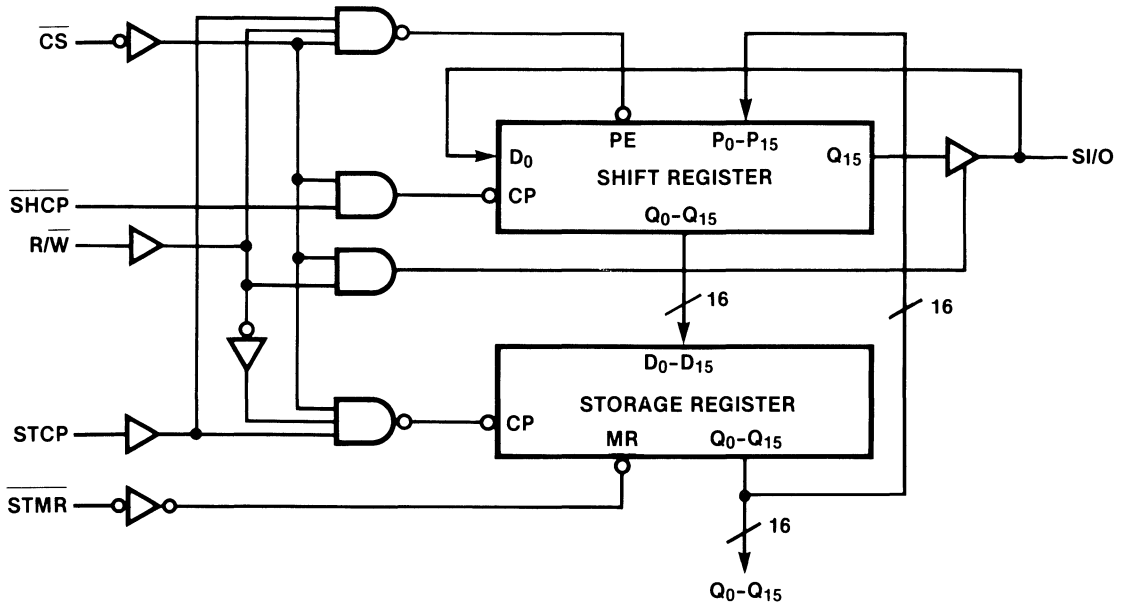
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↓ = HIGH-to-LOW Transition

Storage Register Operations Table

Control Inputs				Operating Mode
$\overline{STMR}$	$\overline{CS}$	R/$\overline{W}$	STCP	
L	X	X	X	Reset; Outputs LOW
H	H	X	X	Hold
H	X	H	X	Hold
H	L	L	↑	Parallel Load

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↑ = LOW-to-HIGH Transition

Block Diagram



4

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		106	160	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$			T_A, V_{CC} = Mil $C_L = 50\ pF$		T_A, V_{CC} = Com $C_L = 50\ pF$			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	100	130				85		MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay STCP to Q_n	3.0 3.0	8.0 10.5	10.5 13.5			2.5 2.5	12.0 15.0	ns	3-1 3-7
t_{PHL}	Propagation Delay $\overline{STMR}$ to Q_n	6.5	16.5	20.5			5.5	22.5	ns	3-1 3-11
t_{PLH} t_{PHL}	Propagation Delay $\overline{SHCP}$ to SI/O	4.0 4.5	6.5 8.0	8.5 10.5			3.5 4.0	9.5 12.0	ns	3-1 3-8
t_{PZH} t_{PZL}	Output Enable Time $\overline{CS}$ or R/$\overline{W}$ to SI/O	5.0 5.5	8.5 9.0	11.0 11.5			4.0 4.5	12.5 13.0	ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{CS}$ or R/$\overline{W}$ to SI/O	3.5 3.0	5.5 4.5	7.5 6.5			3.0 2.5	8.5 7.5		
t_{PZH} t_{PZL}	Output Enable Time R/$\overline{W}$ to SI/O	4.5 4.5	7.5 8.0	9.5 10.0			4.0 4.0	10.5 11.5	ns	3-1 3-12 3-13
t_{PHZ} t_{PHL}	Output Disable Time R/$\overline{W}$ to SI/O	3.0 2.5	5.5 4.0	7.0 5.5			2.5 2.0	8.0 6.5		

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F $T_A = +25°C$ $V_{CC} = +5.0\ V$			54F T_A, V_{CC} = Mil		74F T_A, V_{CC} = Com		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{CS}$ or R/$\overline{W}$ to STCP	3.5 6.0					4.0 7.0		ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{CS}$ or R/$\overline{W}$ to STCP	0 0					0 0			
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW SI/O to $\overline{SHCP}$	3.0 3.0					3.5 3.5		ns	3-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW SI/O to $\overline{SHCP}$	3.0 3.0					3.5 3.5			
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{CS}$ to $\overline{SHCP}$	3.0 3.0					3.5 3.5		ns	3-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{CS}$ to $\overline{SHCP}$	3.0 3.0					3.5 3.5			
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW R/$\overline{W}$ to $\overline{SHCP}$	6.5 9.0					7.5 10.0		ns	3-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW R/$\overline{W}$ to $\overline{SHCP}$	0 0					0 0			
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW STCP to $\overline{SHCP}$	7.0 7.0					8.0 8.0		ns	3-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW STCP to $\overline{SHCP}$	0 0					0 0			
$t_s(L)$	Setup Time, LOW $\overline{SHCP}$ to STCP	7.5					8.5		ns	3-6
$t_h(H)$	Hold Time, HIGH $\overline{SHCP}$ to STCP	0					0			
$t_w(H)$ $t_w(L)$	$\overline{SHCP}$ Pulse Width HIGH or LOW	4.0 5.5					4.5 6.5		ns	3-8
$t_w(H)$ $t_w(L)$	STCP Pulse Width HIGH or LOW	3.5 3.5					4.0 4.0		ns	3-7
$t_w(L)$	$\overline{STMR}$ Pulse Width, LOW	7.5					8.5		ns	3-11
t_{rec}	Recovery Time $\overline{STMR}$ to STCP	2.5					3.0		ns	3-11

54F/74F674

16-Bit Serial/Parallel-In, Serial-Out Shift Register

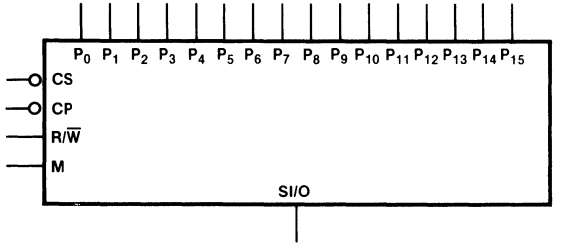
Description

The 'F674 is a 16-bit shift register with serial and parallel load capability and serial output. A single pin serves alternately as an input for serial entry or as a 3-state serial output. In the serial-out mode the data recirculates in the register. Chip Select, Read/Write and Mode inputs provide control flexibility.

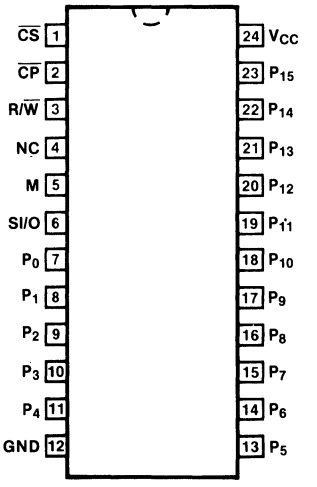
- **16-Bit Serial I/O Shift Register**
- **16-Bit Parallel-In, Serial-Out Converter**
- **Recirculating Serial Shifting**
- **Common Serial Data I/O Pin**
- **Slim 24 Lead Package**

Ordering Code: See Section 5

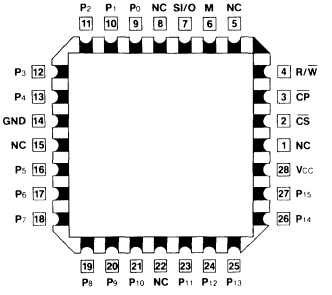
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
$\overline{P_0}$-P_{15}	Parallel Data Inputs	0.5/0.375
$\overline{CS}$	Chip Select Input (Active LOW)	0.5/0.375
$\overline{CP}$	Clock Pulse Input (Active LOW)	0.5/0.375
M	Mode Select Input	0.5/0.375
R/$\overline{W}$	Read/Write Input	0.5/0.375
SI/O	3-State Serial Data Input or	1.75/0.375
	3-State Serial Output	75/15 (12.5)

Functional Description

The 16-bit shift register operates in one of four modes, as indicated in the Shift Register Operations Table.

Hold—a HIGH signal on the Chip Select ($\overline{CS}$) input prevents clocking and forces the Serial Input/Output (SI/O) 3-state buffer into the high impedance state.

Serial Load—data present on the SI/O pin shifts into the register on the falling edge of $\overline{CP}$. Data enters the Q_0 position and shifts toward Q_{15} on successive clocks.

Serial Output—the SI/O 3-state buffer is active and the register contents are shifted out from Q_{15} and simultaneously shifted back into Q_0.

Parallel Load—data present on P_0-P_{15} are entered into the register on the falling edge of $\overline{CP}$. The SI/O 3-state buffer is active and represents the Q_{15} output.

To prevent false clocking, $\overline{CP}$ must be LOW during a LOW-to-HIGH transition of $\overline{CS}$.

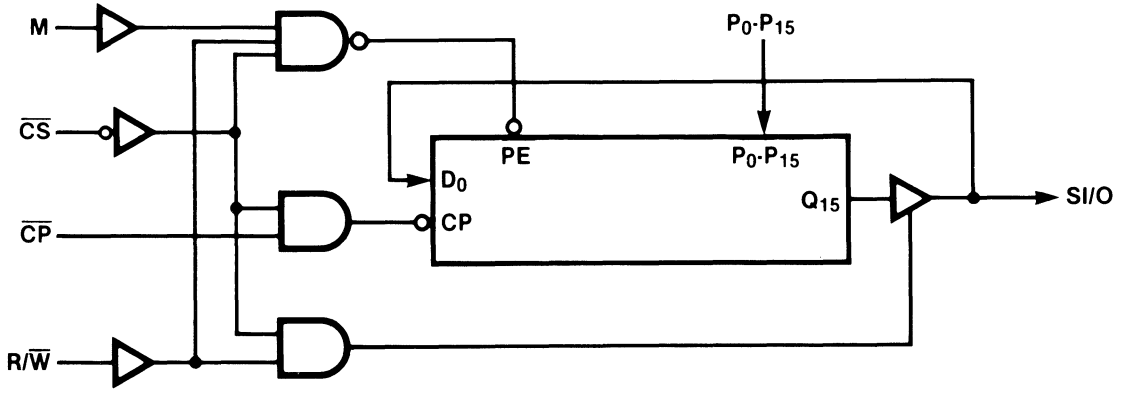
4

Shift Register Operations Table

Control Inputs				SI/O Status	Operating Mode
$\overline{CS}$	R/$\overline{W}$	$\overline{M}$	$\overline{CP}$		
H	X	X	X	High Z	Hold
L	L	X	↓	Data In	Serial Load
L	H	L	↓	Data Out	Serial Output with Recirculation
L	H	H	↓	Active	Parallel Load; No Shifting

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↓ = HIGH-to-LOW Transition

Block Diagram



DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		53	80	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF	T_A, V_{CC} = Mil, C_L = 50 pF	T_A, V_{CC} = Com, C_L = 50 pF		
		Min Typ Max	Min Max	Min Max		
f_{max}	Maximum Clock Frequency	100 140			MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to SI/O	11.0 12.5			ns	3-1 3-8
t_{PZH} t_{PZL}	Output Enable Time $\overline{CS}$ or R/$\overline{W}$ to SI/O	7.0 7.0			ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{CS}$ or R/$\overline{W}$ to SI/O	7.0 7.0				

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW SI/O to $\overline{CP}$	7.0 7.0			ns	3-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW SI/O to $\overline{CP}$	0 0				
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW P_n to $\overline{CP}$	3.0 3.0			ns	3-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW P_n to $\overline{CP}$	0 0				
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW R/$\overline{W}$ or $\overline{CS}$ to $\overline{CP}$	5.0 5.0			ns	3-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW R/$\overline{W}$ or $\overline{CS}$ to $\overline{CP}$	0 0				
$t_w(H)$ $t_w(L)$	$\overline{CP}$ Pulse Width HIGH or LOW	4.0 5.0			ns	3-8

54F/74F675

16-Bit Serial-In, Serial/Parallel-Out Shift Register

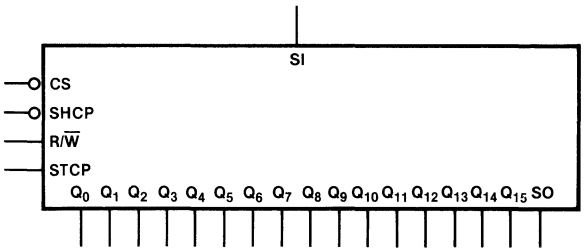
Description

The 'F675 contains a 16-bit serial-in, serial-out shift register and a 16-bit parallel-out storage register. Separate serial input and output pins are provided for expansion to longer words. By means of a separate clock, the contents of the shift register are transferred to the storage register. The contents of the storage register can also be loaded back into the shift register. A HIGH signal on the Chip Select input prevents both shifting and parallel loading.

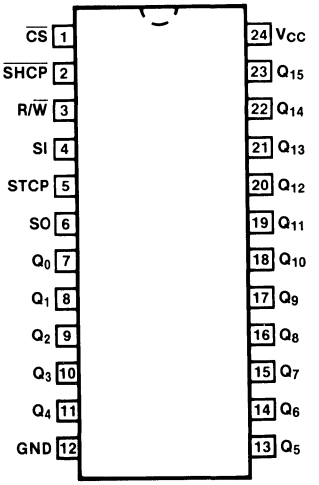
- **Serial-to-Parallel Converter**
- **16-Bit Serial I/O Shift Registerd**
- **16-Bit Parallel-Out Storage Register**
- **Recirculating Parallel Transfer**
- **Expandable for Longer Words**

Ordering Code: See Section 5

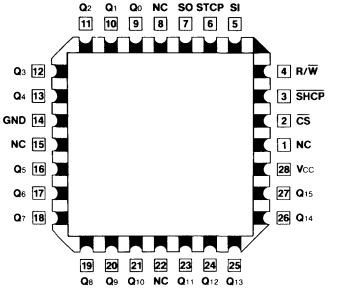
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
SI	Serial Data Input	0.5/0.375
$\overline{CS}$	Chip Select Input (Active LOW)	0.5/0.375
$\overline{SHCP}$	Shift Clock Pulse Input (Active Falling Edge)	0.5/0.375
STCP	Store Clock Pulse Input (Active Rising Edge)	0.5/0.375
R/$\overline{W}$	Read/Write Input	0.5/0.375
SO	Serial Data Output	25/12.5
Q_0-Q_{15}	Parallel Data Outputs	25/12.5

Functional Description

The 16-bit shift register operates in one of four modes, as determined by the signals applied to the Chip Select ($\overline{CS}$), Read/Write (R/$\overline{W}$) and Store Clock Pulse (STCP) input. State changes are indicated by the falling edge of the Shift Clock Pulse ($\overline{SHCP}$). In the Shift Right mode, data enters D_0 from the Serial Input (SI) pin and exits from Q_{15} via the Serial Data Output (SO) pin. In the Parallel Load mode, data from the storage register outputs enter the shift register and serial shifting is inhibited.

The storage register is in the Hold mode when either $\overline{CS}$ or R/$\overline{W}$ is HIGH. With $\overline{CS}$ and R/$\overline{W}$ both LOW, the storage register is parallel loaded from the shift register on the rising edge of STCP.

To prevent false clocking of the shift register, $\overline{SHCP}$ should be in the LOW state during a LOW-to-HIGH transition of $\overline{CS}$. To prevent false clocking of the storage register, STCP should be LOW during a HIGH-to-LOW transition of $\overline{CS}$ if R/$\overline{W}$ is LOW, and should also be LOW during a HIGH-to-LOW transition of R/$\overline{W}$ if $\overline{CS}$ is LOW.

Shift Register Operations Table

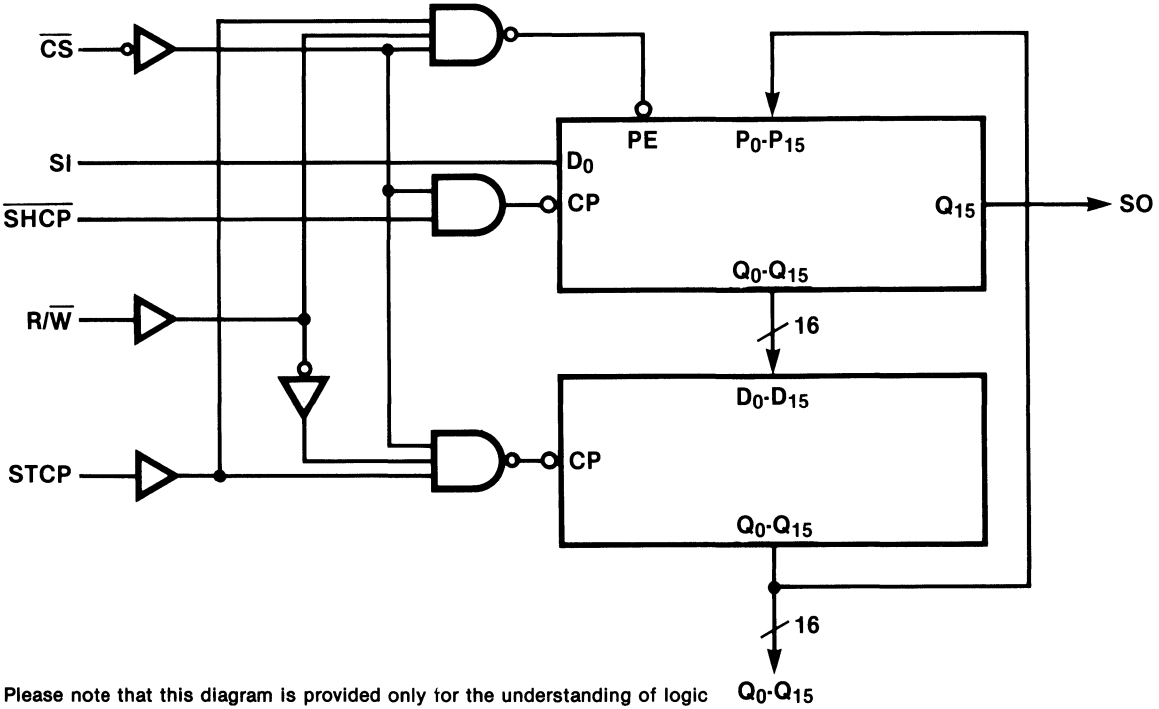
Control Inputs				Operating Mode
$\overline{CS}$	R/$\overline{W}$	$\overline{SHCP}$	STCP	
H	X	X	X	Hold
L	L	↓	X	Shift Right
L	H	↓	L	Shift Right
L	H	↓	H	Parallel Load; No Shifting

Storage Register Operations Table

Inputs			Operating Mode
$\overline{CS}$	R/$\overline{W}$	STCP	
H	X	X	Hold
L	H	X	Hold
L	L	↑	Parallel Load

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↑ = LOW-to-HIGH Transition
↓ = HIGH-to-LOW Transition

Block Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		106	160	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	100	130				80		MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay STCP to Q_n	6.5 6.5	11.0 11.0	14.0 14.0			6.5 6.5	15.0 15.0	ns	3-1 3-7
t_{PLH} t_{PHL}	Propagation Delay $\overline{SHCP}$ to SO	5.5 5.5	9.0 9.0	11.5 11.5			5.5 5.5	12.5 12.5	ns	3-1 3-8

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$	Setup Time, HIGH $\overline{CS}$ or R/$\overline{W}$ to STCP	0		0	ns	3-5
$t_h(L)$	Hold Time, LOW $\overline{CS}$ or R/$\overline{W}$ to STCP	7.0		7.0		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW SI to $\overline{SHCP}$	3.0 3.0		3.0 3.0	ns	3-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW SI to $\overline{SHCP}$	3.0 3.0		3.0 3.0		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW R/$\overline{W}$ to $\overline{SHCP}$	10.0 10.0		10.0 10.0	ns	3-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW R/$\overline{W}$ to $\overline{SHCP}$	0 0		0 0		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW STCP to $\overline{SHCP}$	10.0 10.0		10.0 10.0	ns	3-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW STCP to $\overline{SHCP}$	0 0		0 0		
$t_s(L)$	Setup Time, LOW $\overline{CS}$ to $\overline{SHCP}$	7.0		7.0	ns	3-6
$t_h(H)$	Hold Time, HIGH $\overline{CS}$ to $\overline{SHCP}$	0		0		
$t_w(H)$ $t_w(L)$	$\overline{SHCP}$ Pulse Width, HIGH or LOW	5.0 5.0		6.0 6.0	ns	3-8
$t_w(H)$ $t_w(L)$	STCP Pulse Width, HIGH or LOW	6.0 5.0		7.0 6.0	ns	3-8

54F/74F675A

16-Bit Serial-In, Serial/Parallel-Out Shift Register

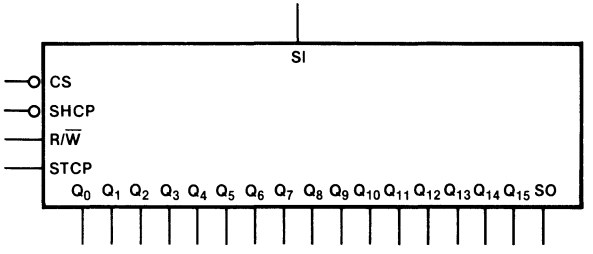
Description

The 'F675A contains a 16-bit serial in/serial out shift register and a 16-bit parallel out storage register. Separate serial input and output pins are provided for expansion to longer words. By means of a separate clock, the contents of the shift register are transferred to the storage register. The contents of the storage register can also be loaded back into the shift register. A HIGH signal on the Chip Select input prevents both shifting and parallel loading.

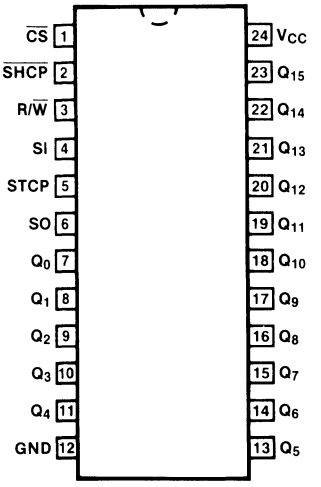
- **Serial-to-Parallel Converter**
- **16-Bit Serial I/O Shift Register**
- **16-Bit Parallel Out Storage Register**
- **Recirculating Parallel Transfer**
- **Expandable for Longer Words**
- **Slim 24 Lead Package**
- **'F675A Version Prevents False Clocking through $\overline{CS}$ or R/$\overline{W}$ Inputs**

Ordering Code: See Section 5

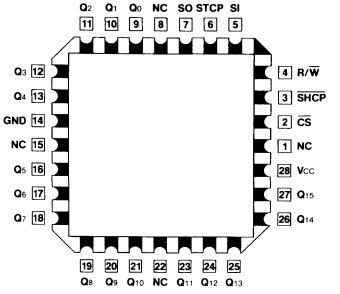
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
SI	Serial Data Input	0.5/0.375
$\overline{CS}$	Chip Select Input (Active LOW)	0.5/0.375
$\overline{SHCP}$	Shift Clock Pulse Input (Active Falling Edge)	0.5/0.375
STCP	Store Clock Pulse Input (Active Rising Edge)	0.5/0.375
R/$\overline{W}$	Read/Write Input	0.5/0.375
SO	Serial Data Output	25/12.5
Q_0-Q_{15}	Parallel Data Outputs	25/12.5

Functional Description

The 16-bit shift register operates in one of four modes, as determined by the signals applied to the Chip Select ($\overline{CS}$), Read/Write (R/$\overline{W}$) and Store Clock Pulse (STCP) input. State changes are indicated by the falling edge of the Shift Clock Pulse ($\overline{SHCP}$). In the Shift Right mode, data enters D_0 from the Serial Input (SI) pin and exits from Q_{15} via the Serial Data Output (SO) pin. In the Parallel Load mode, data from the storage register outputs enter the shift register and serial shifting is inhibited.

The storage register is in the Hold mode when either $\overline{CS}$ or R/$\overline{W}$ is HIGH. With $\overline{CS}$ and R/$\overline{W}$ both LOW, the storage register is parallel loaded from the shift register on the rising edge of STCP.

To prevent false clocking of the shift register, $\overline{SHCP}$ should be in the LOW state during a LOW-to-HIGH transition of $\overline{CS}$. To prevent false clocking of the storage register, STCP should be LOW during a HIGH-to-LOW transition of $\overline{CS}$ if R/$\overline{W}$ is LOW, and should also be LOW during a HIGH-to-LOW transition of R/$\overline{W}$ if $\overline{CS}$ is LOW.

Shift Register Operations Table

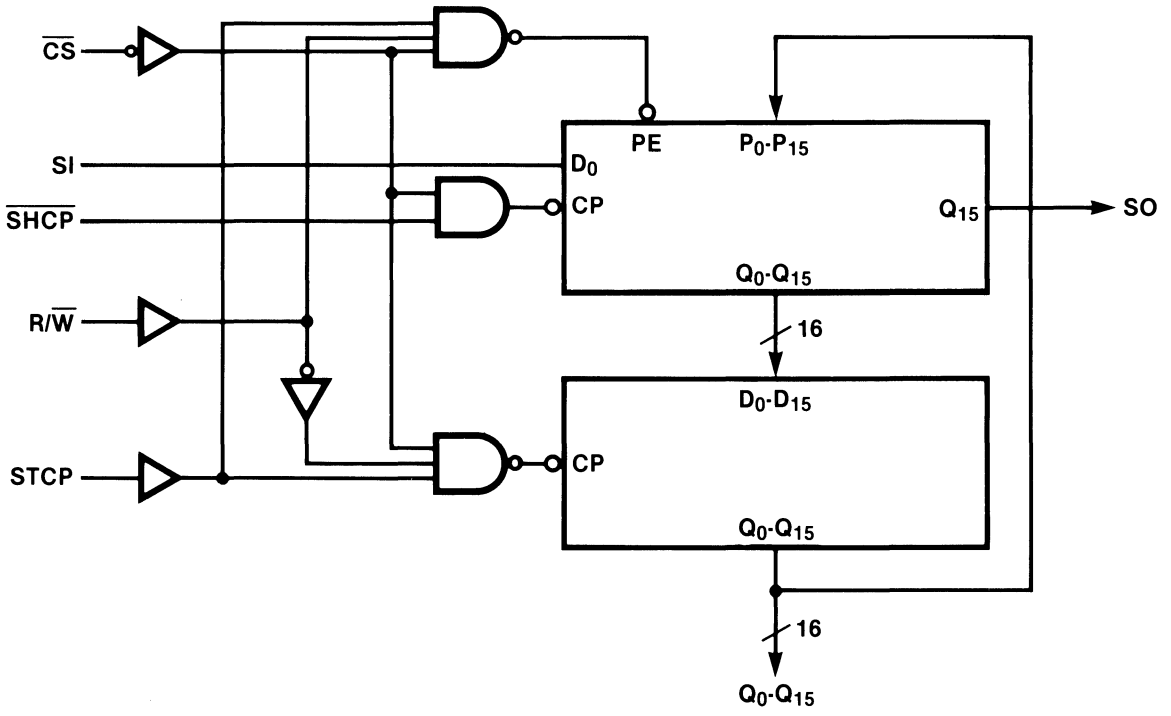
Control Inputs				Operating Mode
$\overline{CS}$	R/$\overline{W}$	$\overline{SHCP}$	STCP	
H	X	X	X	Hold
L	L	↑	X	Shift Right
L	H	↑	L	Shift Right
L	H	↑	H	Parallel Load, No Shifting

Storage Register Operations Table

Inputs			Operating Mode
$\overline{CS}$	R/$\overline{W}$	STCP	
H	X	X	Hold
L	H	X	Hold
L	L	↑	Parallel Load

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↑ = LOW-to-HIGH Transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		106	160	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	100	130				85		MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay STCP to Q_n	3.0 3.0	8.0 10.5	10.5 13.5			2.5 2.5	12.0 15.0	ns	3-1 3-7
t_{PLH} t_{PHL}	Propagation Delay $\overline{SHCP}$ to SO	4.0 4.5	7.0 8.0	9.5 10.5			3.5 4.0	10.5 12.0	ns	3-1 3-8

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{CS}$ or R/$\overline{W}$ to STCP	3.5 5.5		4.0 6.5	ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{CS}$ or R/$\overline{W}$ to STCP	0 0		0 0		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW SI to $\overline{SHCP}$	3.0 3.0		3.5 3.5	ns	3-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW SI to $\overline{SHCP}$	3.0 3.0		3.5 3.5		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW R/$\overline{W}$ to $\overline{SHCP}$	6.5 9.0		7.5 10.0	ns	3-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW R/$\overline{W}$ to $\overline{SHCP}$	0 0		0 0		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW STCP to $\overline{SHCP}$	7.0 7.0		8.0 8.0	ns	3-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW STCP to $\overline{SHCP}$	0 0		0 0		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{CS}$ to $\overline{SHCP}$	3.0 3.0		3.5 3.5	ns	3-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{CS}$ to $\overline{SHCP}$	3.0 3.0		3.5 3.5		
$t_s(L)$	Setup Time, LOW $\overline{SHCP}$ to STCP	8.0		9.0	ns	3-5
$t_h(H)$	Hold Time, HIGH $\overline{SHCP}$ to STCP	0		0		
$t_w(H)$ $t_w(L)$	$\overline{SHCP}$ Pulse Width HIGH or LOW	5.0 5.0		6.0 6.0	ns	3-8
$t_w(H)$ $t_w(L)$	STCP Pulse Width HIGH or LOW	6.0 5.0		7.0 6.0		

54F/74F676

16-Bit Serial/Parallel-In, Serial-Out Shift Register

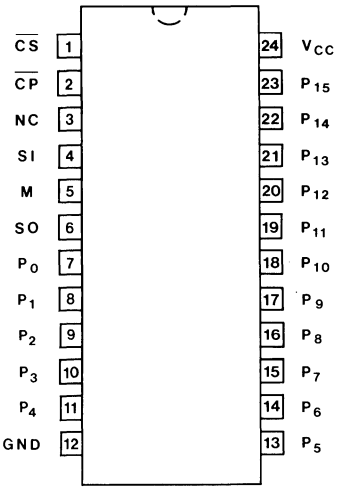
Description

The 'F676 contains 16 flip-flops with provision for synchronous parallel or serial entry and serial output. When the Mode (M) input is HIGH, information present on the parallel data (P_0-P_{15}) inputs is entered on the falling edge of the Clock Pulse ($\overline{CP}$) input signal. When M is LOW, data is shifted out of the most significant bit position while information present on the Serial (SI) input shifts into the least significant bit position. A HIGH signal on the Chip Select ($\overline{CS}$) input prevents both parallel and serial operations.

- **16-Bit Parallel-to-Serial Conversion**
- **16-Bit Serial-In, Serial-Out**
- **Chip Select Control**
- **Slim 24 Lead 300 mil Package**

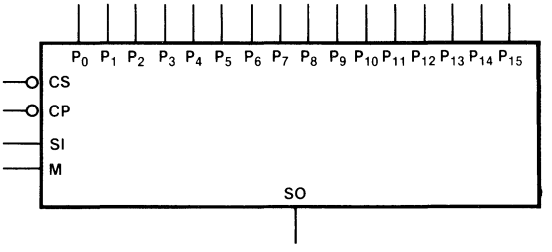
Ordering Code: See Section 5

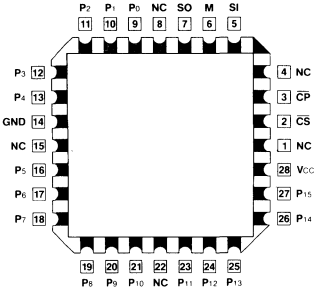
Connection Diagrams



Pin Assignment for DIP and SOIC

Logic Symbol





Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
P_0-P_{15}	Parallel Data Inputs	0.5/0.375
$\overline{CS}$	Chip Select Input (Active LOW)	0.5/0.375
$\overline{CP}$	Clock Pulse Input (Active LOW)	0.5/0.375
M	Mode Select Input	0.5/0.375
SI	Serial Data Input	0.5/0.375
SO	Serial Output	25/12.5

Functional Description

The 16-bit shift register operates in one of three modes, as indicated in the Shift Register Operations Table.

HOLD—a HIGH signal on the Chip Select ($\overline{CS}$) input prevents clocking, and data is stored in the sixteen registers.

Shift/Serial Load—data present on the SI pin shifts into the register on the falling edge of $\overline{CP}$. Data enters the Q_0 position and shifts toward Q_{15} on successive clocks, finally appearing on the SO pin.

Parallel Load—data present on P_0-P_{15} are entered into the register on the falling edge of $\overline{CP}$. The SO output represents the Q_{15} register output.

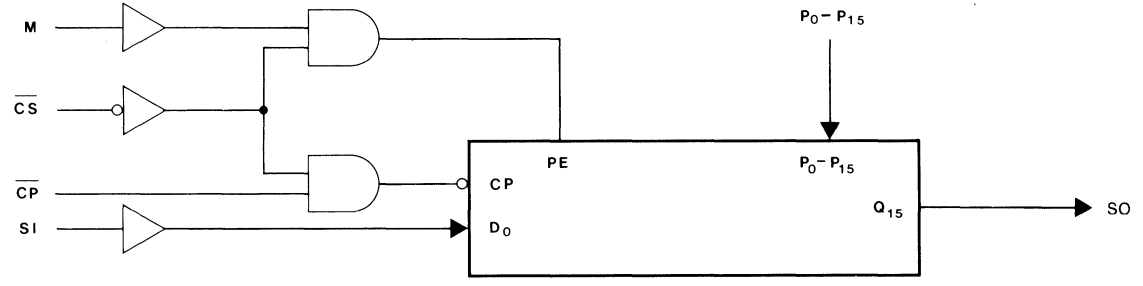
To prevent false clocking, $\overline{CP}$ must be LOW during a LOW-to-HIGH transition of $\overline{CS}$.

Shift Register Operations Table

Control Input			Operating Mode
$\overline{CS}$	M	$\overline{CP}$	
H	X	X	Hold
L	L	↓	Shift/Serial Load
L	H	↓	Parallel Load

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↓ = HIGH-to-LOW Transition

Block Diagram



DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		48	72	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$			T_A, V_{CC} = Mil $C_L = 50\ pF$		T_A, V_{CC} = Com $C_L = 50\ pF$			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	100	110		75		90		MHz	3-1
t_{PLH}	Propagation Delay	4.5	9.0	11.0	4.5	17.0	4.5	12.0	ns	3-1
t_{PHL}	$\overline{CP}$ to SO	5.0	9.0	12.5	5.0	14.5	5.0	13.5		3-8

4

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
$t_s(H)$	Setup Time, HIGH or LOW	4.0			4.0		4.0		ns	3-6
$t_s(L)$	SI to $\overline{CP}$	4.0			4.0		4.0			
$t_h(H)$	Hold Time, HIGH or LOW	4.0			4.0		4.0			
$t_h(L)$	SI to $\overline{CP}$	4.0			4.0		4.0			
$t_s(H)$	Setup Time, HIGH or LOW	3.0			3.0		3.0		ns	3-6
$t_s(L)$	P_n to $\overline{CP}$	3.0			3.0		3.0			
$t_h(H)$	Hold Time, HIGH or LOW	4.0			4.0		4.0			
$t_h(L)$	P_n to $\overline{CP}$	4.0			4.0		4.0			
$t_s(H)$	Setup Time, HIGH or LOW	8.0			8.0		8.0		ns	3-6
$t_s(L)$	M to $\overline{CP}$	8.0			8.0		8.0			
$t_h(H)$	Hold Time, HIGH or LOW	2.0			2.0		2.0			
$t_h(L)$	M to $\overline{CP}$	2.0			2.0		2.0			
$t_s(L)$	Setup Time, LOW $\overline{CS}$ to $\overline{CP}$	10.0			12.0		10.0		ns	3-6
$t_h(H)$	Hold Time, HIGH $\overline{CS}$ to $\overline{CP}$	10.0			10.0		10.0			
$t_w(H)$	$\overline{CP}$ Pulse Width	4.0			5.0		4.0		ns	3-8
$t_w(L)$	HIGH or LOW	6.0			8.0		6.0			

54F/74F779

8-Bit Bidirectional Binary Counter With 3-State Outputs

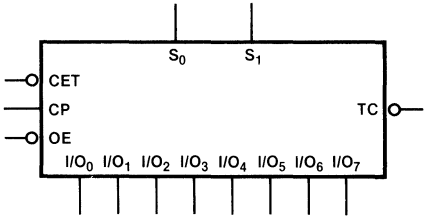
Description

The 'F779 is a fully synchronous 8-stage up/down counter with multiplexed 3-state I/O ports for bus-oriented applications. All control functions (hold, count up, count down, synchronous load) are controlled by two mode pins (S_0, S_1). The device also features carry lookahead for easy cascading. All state changes are initiated by the rising edge of the clock.

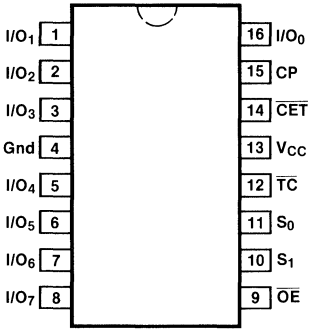
- **Multiplexed 3-State I/O Ports**
- **Built in Lookahead Carry Capability**
- **Count Frequency 100 MHz Typ**
- **Supply Current 80 mA Typ**

Ordering Code: See Section 5

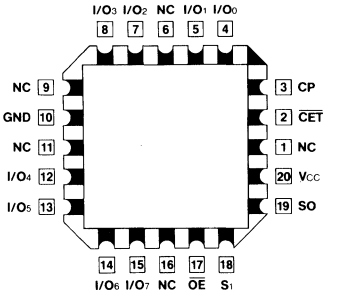
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC

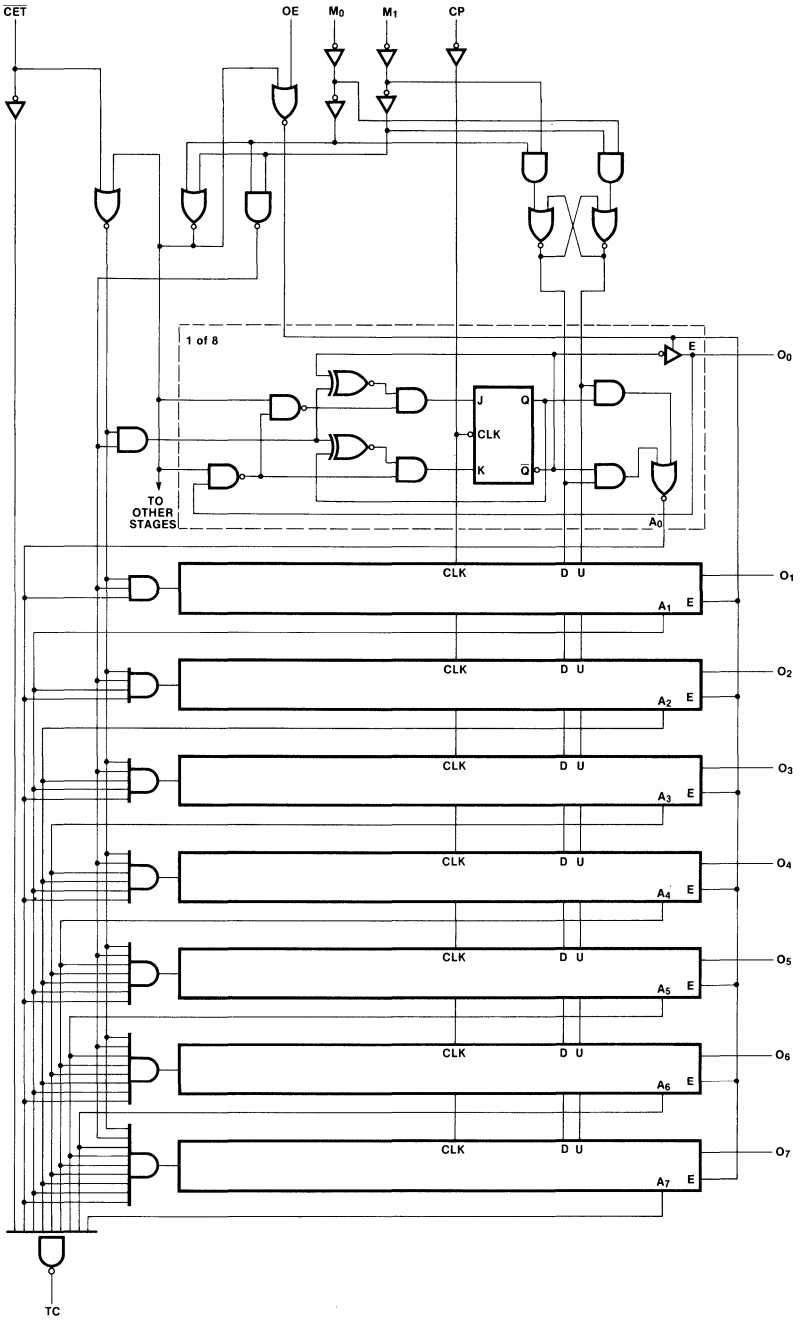


Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
I/O_0-I/O_7	Data Inputs	0.5/0.375
	Data Outputs	75/15 (12.5)
S_0,S_1	Select Inputs	0.5/0.375
$\overline{OE}$	Output Enable Input (Active LOW)	0.5/0.375
$\overline{CET}$	Count Enable Trickle Input (Active LOW)	0.5/0.375
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
$\overline{TC}$	Terminal Count Output (Active LOW)	25/12.5

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Function Table

S_1	S_0	$\overline{CET}$	$\overline{OE}$	CP	Function
X	X	X	H	X	I/O_0 to I/O_7 in High Z
X	X	X	L	X	Flip-flop outputs appear on I/O lines
L	L	X	X	↑	Parallel load all flip-flops
(not LL)		H	X	↑	Hold ($\overline{TC}$ held HIGH)
H	H	X	X	↑	Hold
H	L	L	X	↑	Count Up
L	H	L	X	↑	Count Down

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↑ = LOW-to-HIGH Clock Transition
(not LL) means S_0 and S_1 should never both be LOW level at the same time.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions	
		Min	Typ	Max			
I_{CCH}	Power Supply Current		50	70	mA	Outputs HIGH	V_{CC} = Max
I_{CCL}			80	100		Outputs LOW	
I_{CCZ}			80	100		Outputs Disabled	

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$	T_A, V_{CC} = Mil $C_L = 50\ pF$	T_A, V_{CC} = Com $C_L = 50\ pF$		
		Min Typ Max	Min Max	Min Max		
f_{max}	Maximum Clock Frequency	80 100			MHz	3-1 3-2
t_{PLH} t_{PHL}	Propagation Delay CP to I/O_n	3.0 4.5			ns	3-1 3-2
t_{PLH}	Propagation Delay $\overline{CET}$ to $\overline{TC}$	6.0			ns	3-1 3-2
t_{PHL}	Propagation Delay CP to $\overline{TC}$	5.0			ns	3-1 3-2
t_{PZH} t_{PZL}	Output Enable Time	12.0 12.0			ns	3-1, 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time	12.0 12.0			ns	3-1, 3-12 3-13

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW Data to CP	5.0 5.0			ns	3-14
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW Data to CP	0 0				
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{OE}$ to CP	12.0 12.0			ns	3-14
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{OE}$ to CP	0 0				
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{CET}$ to CP	10.0 10.0			ns	3-14
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{CET}$ to CP	0 0				
$t_w(H)$	Clock Pulse Width, HIGH	5.0			ns	3-2, 3-7

54F/74F784

8-Bit Serial-Parallel Multiplier With Adder/Subtractor

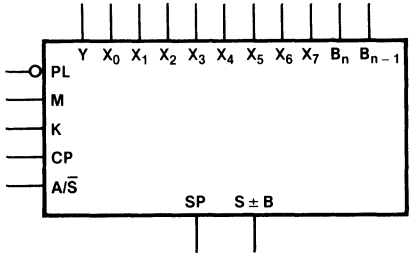
Description

The 'F784 is a serial (nx8)-bit multiplier with a final stage adder/subtractor for optional use in adding a B bit to obtain S ± B. A (B_{n-1})-bit can also be added via an internal flip-flop to achieve a 1-bit delay. The x word is parallel loaded (eight bits wide) into latches and the y word is clocked in serially from a shift register. The 'F784 is particularly useful for high-speed digital filtering or butterfly networks in Fast Fourier Transforms.

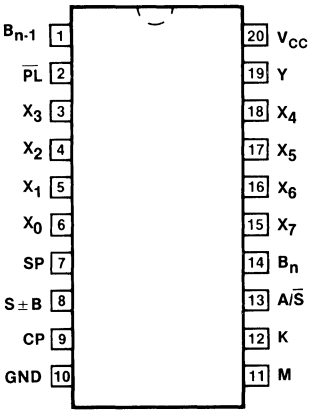
- **Twos Complement Multiplication**
- **Cascadable for any Number of Bits**
- **Full Adder and B-1 Input Included for Maximum Flexibility**
- **Maximum Clock Frequency 50 MHz Guaranteed**
- **Supply Current 100 mA Max**

Ordering Code: See Section 5

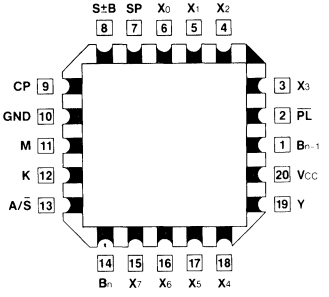
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
X_0-X_7	Multiplicand Data Inputs	0.5/0.375
Y	Serial Multiplier Input	0.5/0.375
CP	Clock Pulse Input	0.5/0.375
K	Serial Expansion Input	0.5/0.375
M	Mode Control Input	0.5/0.375
$\overline{PL}$	Parallel Load Input	0.5/0.75
A/$\overline{S}$	Add/Subtract	0.5/0.375
SP	Serial X•Y Product Output	25/12.5
S ± B	Serial X•Y ± B Output	25/12.5
B_n	Serial B Input	0.5/0.375
B_{n-1}	Delayed Serial B Input	0.5/0.375

Functional Description

The 'F784 is a serial-parallel 8-bit multiplier. Also included is an adder/subtractor stage. The X word (multiplicand) is loaded into a register while simultaneously clearing the arithmetic cell flip-flops in preparation for a multiplication. The Y word (multiplier) is clocked in serially.

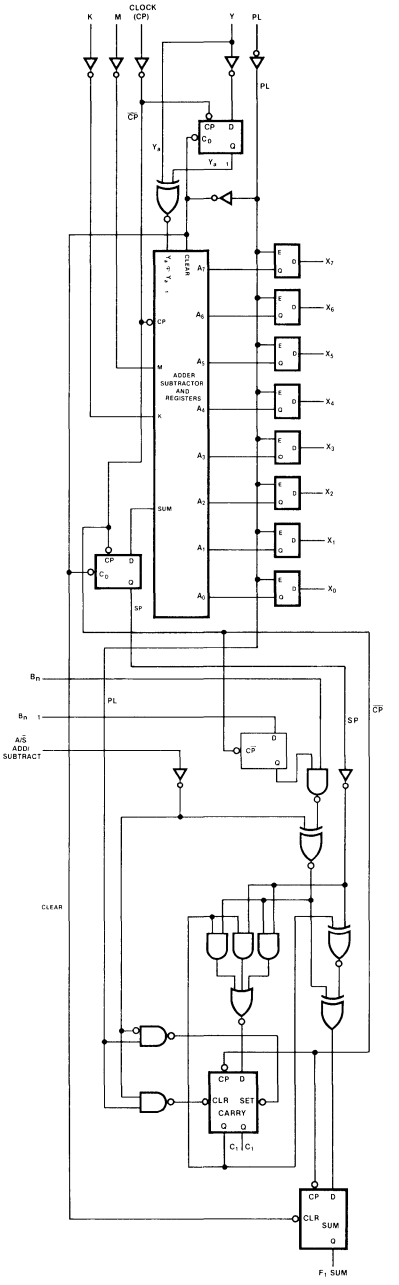
Expansion capability is provided via the M and K inputs. The K (cascade) input is connected to the S_0 output of the more significant chip. The M (mode) input is used to determine whether the multiplicand is to be treated as a two's complement or unsigned number.

The 'F784 has logic to enable complex arithmetic to be performed. A serial adder/subtractor enables constants to be added to the product. Typically this feature would be used in FFT butterfly networks to reduce package count and power.

Two outputs are provided: the product XY and the product XY ± B. Because of the internal adder/subtractor, a speed advantage is gained when using the 'F784 over using a separate adder and multiplier chip.

During a multiplication operation, the first clock cycle is used to load both the X word (multiplicand) and the first bit of the Y word (operand) into the input registers. At this time there is no valid data at the SP output so that B bits added will not give the correct sum output. In order to load the first B bit on the same clock as X and Y, a B_{n-1} input is provided which delays the B data by one clock cycle. Thus, a valid output results.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		67	100	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	50	65				50		MHz	3-1
t_{PHL}	Propagation Delay $\overline{PL}$ to SP	6.0	10.0	13.0			5.0	14.5	ns	3-1 3-11
t_{PHL}	Propagation Delay $\overline{PL}$ to S ± B	5.5	9.5	12.0			4.5	13.5	ns	3-1 3-11
t_{PLH} t_{PHL}	Propagation Delay CP to SP	4.0 4.5	6.5 8.0	9.0 10.5			3.5 4.0	10.0 12.0	ns	3-1 3-7
t_{PLH} t_{PHL}	Propagation Delay CP to S ± B	4.0 4.0	7.0 7.0	9.0 9.0			3.5 3.5	10.0 10.0	ns	3-1 3-7

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F $T_A = +25°C$ $V_{CC} = +5.0\,V$			54F T_A, V_{CC} = Mil		74F T_A, V_{CC} = Com		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Set up Time, HIGH or LOW K to CP	13.0 9.0					14.0 10.0		ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW K to CP	0 1.0					0 1.0			
$t_s(H)$ $t_s(L)$	Set up Time, HIGH or LOW Y to CP	15.0 15.0					16.0 16.0		ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW Y to CP	1.5 1.5					1.5 1.5			
$t_s(H)$ $t_s(L)$	Set up Time, HIGH or LOW X to $\overline{PL}$	5.0 5.0					6.0 6.0		ns	3-14
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW X to $\overline{PL}$	2.0 2.0					2.0 2.0			
$t_s(H)$ $t_s(L)$	Set up Time, HIGH or LOW B_n to CP	7.0 7.0					8.0 8.0		ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW B_n to CP	0 0					0 0			
$t_s(H)$ $t_s(L)$	Set up Time, HIGH or LOW A/$\overline{S}$ to CP	12.0 12.0					13.0 13.0		ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW A/$\overline{S}$ to CP	1.5 1.5					1.5 1.5			
$t_s(H)$ $t_s(L)$	Set up Time, HIGH or LOW B_{n-1} to CP	4.0 4.0					5.0 5.0		ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW B_{n-1} to CP	0 0					1.0 1.0			
$t_w(L)$	$\overline{PL}$ Pulse Width, LOW	5.0					6.0		ns	3-11
$t_w(H)$ $t_w(L)$	CP Pulse Width HIGH or LOW	5.0 5.0					6.0 6.0		ns	3-7
t_{rec}	Recovery Time $\overline{PL}$ to CP	6.5					7.5		ns	3-11

4

54F/74F821

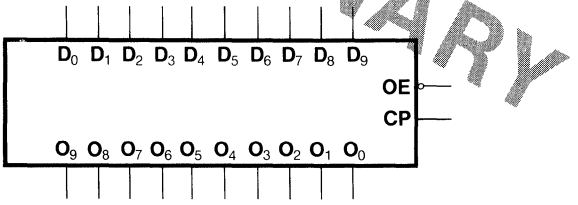
10-Bit D-Type Flip-Flop

Description

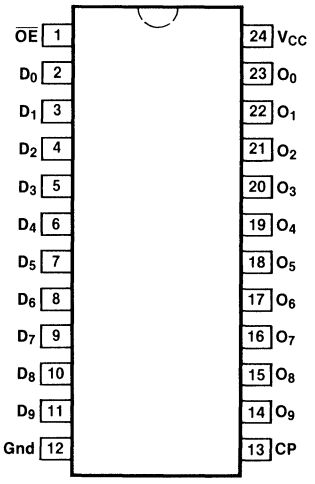
The 'F821 is a 10-bit D-type flip-flop with 3-state true outputs arranged in a broadside pinout. The 'F821 is functionally identical to the AM29821.

Ordering Code: See Section 5

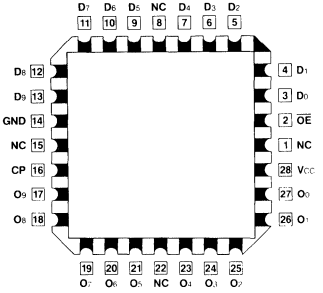
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
D_0-D_9	Data Inputs	0.5/0.375
O_0-O_9	Data Outputs	75/15 (12.5)
$\overline{OE}$	Output Enable	0.5/0.375
CP	Clock Input	0.5/0.75

Functional Description

The 'F821 consists of ten D-type edge-triggered flip-flops. This device has 3-state true outputs for bus systems organized in a broadside pinning. The buffered Clock (CP) and buffered Output Enable ($\overline{OE}$) are common to all flip-flops. The flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH CP transition. With the $\overline{OE}$ LOW the contents of the flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

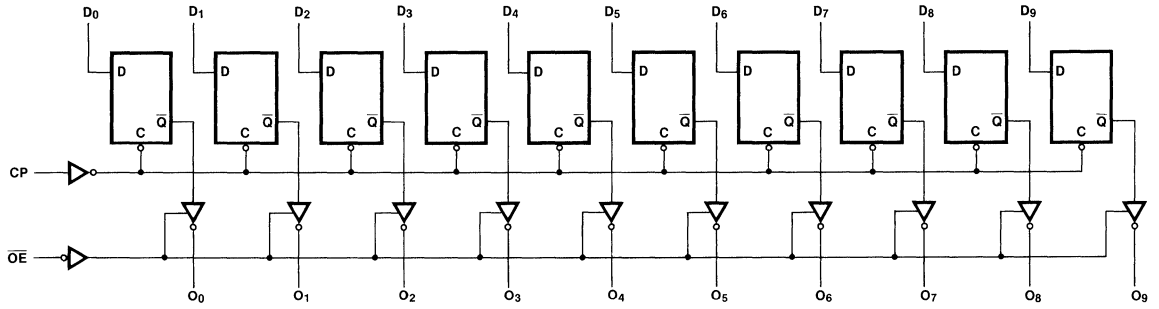
The 'F821 is functionally and pin compatible with the AM29821.

Function Table

Inputs					Internal	Output	Function
$\overline{OE}$	CLR	EN	CP	D	Q	O	
H	X	L	↑	L	L	Z	High Z
H	X	L	↑	H	H	Z	High Z
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	Clear
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	Hold
H	H	L	↑	L	L	Z	Load
H	H	L	↑	H	H	Z	Load
L	H	L	↑	L	L	L	Load
L	H	L	↑	H	H	H	Load

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
↑ = LOW-to-HIGH Transition
NC = No Change

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		75	110	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	100							MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay CP to O_n		7.5 9.5						ns	3-1 3-7
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to O_n		11.5 7.5						ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n		7.0 5.5							

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW D_n to CP	2.0 2.0			ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D_n to CP	2.0 2.0				
$t_w(H)$ $t_w(L)$	CP Pulse Width HIGH or LOW	5.0 5.0			ns	3-7

54F/74F823

9-Bit D-Type Flip Flop

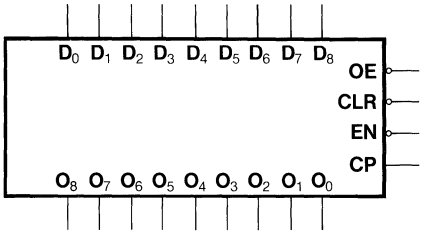
Description

The 'F823 is a 9-bit buffered register. It features Clock Enable and Clear which are ideal for parity bus interfacing in high performance microprogramming systems.

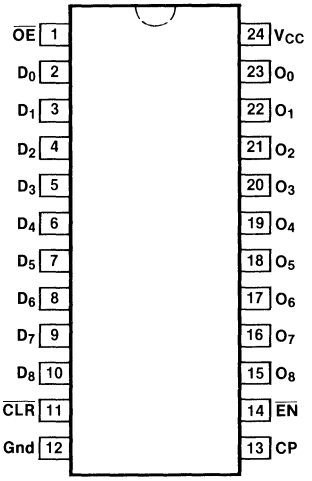
The 'F823 is fully compatible with AMD's Am29823.

Ordering Code: See Section 5

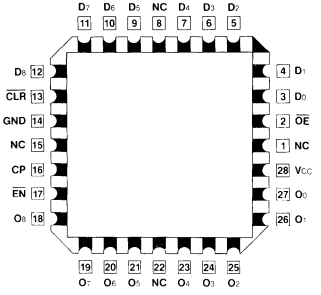
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
D_0-D_8	Data Inputs	0.5/0.375
O_0-O_8	Data Outputs	75/15 (12.5)
$\overline{OE}$	Output Enable	0.5/0.375
$\overline{CLR}$	Clear	0.5/0.375
CP	Clock Input	0.5/0.75
$\overline{EN}$	Clock Enable	0.5/0.375

Functional Description

The 'F823 device consists of nine D-type edge-triggered flip-flops. It has 3-state true outputs for bus systems organized in a broadside pinning. The buffered Clock (CP) and buffered Output Enable ($\overline{OE}$) are common to all flip-flops. The flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH CP transition. With the $\overline{OE}$ LOW the contents of the flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops. In addition to the Clock and Output Enable pins, the 'F823 has Clear ($\overline{CLR}$) and Clock Enable ($\overline{EN}$) pins. This device is ideal for parity bus interfacing in high performance systems.

When the $\overline{CLR}$ is LOW and the $\overline{OE}$ is LOW, the outputs are LOW. When $\overline{CLR}$ is HIGH, data can be entered into the flip-flops. When $\overline{EN}$ is LOW, data on the inputs is transferred to the outputs on the LOW to HIGH clock transition. When the $\overline{EN}$ is HIGH, the outputs do not change state regardless of the data or clock inputs transitions.

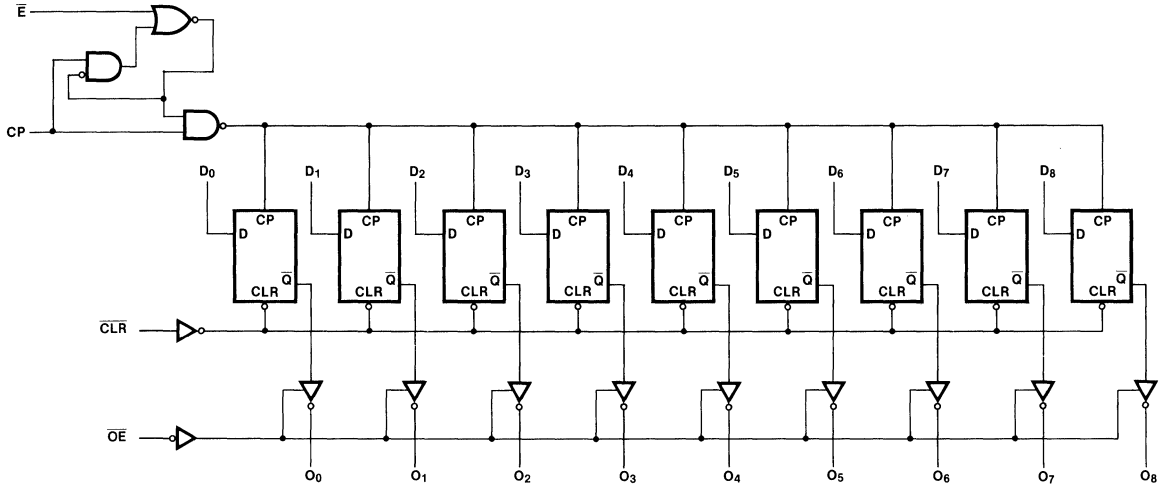
4

Function Table

Inputs					Internal	Output	Function
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	CP	D	Q	O	
H	X	L	↑	L	L	Z	High Z
H	X	L	↑	H	H	Z	High Z
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	Clear
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	Hold
H	H	L	↑	L	L	Z	Load
H	H	L	↑	H	H	Z	Load
L	H	L	↑	L	L	L	Load
L	H	L	↑	H	H	H	Load

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
↑ = LOW-to-HIGH Transition
NC = No Change

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current			110	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	100							MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay CP to O_n		7.5 9.5						ns	3-1 3-7
t_{PHL}	Propagation Delay $\overline{CLR}$ to O_n		15.0						ns	3-1 3-9
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to O_n		11.5 7.5						ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n		7.0 5.5							

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\,V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW D_n to CP	2.0 2.0			ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D_n to CP	2.0 2.0				
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{EN}$ to CP	3.0 3.0			ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{EN}$ to CP	0 0				
$t_w(H)$ $t_w(L)$	CP Pulse Width HIGH or LOW	5.0 5.0			ns	3-7
$t_w(L)$	$\overline{CLR}$ Pulse Width, LOW	5.0			ns	3-9
t_{rec}	$\overline{CLR}$ Recovery Time	5.0			ns	3-11

54F/74F825

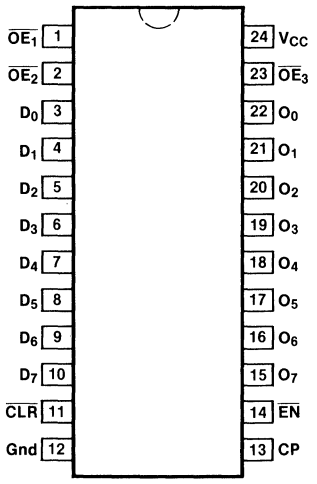
8-Bit D-Type Flip Flop

Description
The 'F825 is an 8-bit buffered register. It has Clock Enable and Clear features which are ideal for parity bus interfacing in high performance microprogramming systems. Also included in the 'F825 are multiple enables that allow multiuser control of the interface.

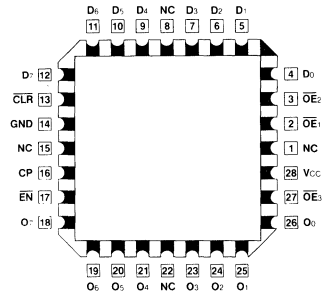
The 'F825 is fully compatible with AMD's AM29825.

Ordering Code: See Section 5

Connection Diagrams

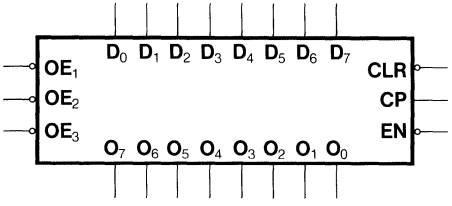


Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Logic Symbol



Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
D_0-D_7	Data Inputs	0.5/0.375
O_0-O_7	Data Outputs	75/15 (12.5)
$\overline{OE_1}$, $\overline{OE_2}$, $\overline{OE_3}$	Output Enable	0.5/0.375
$\overline{EN}$	Clock Enable	0.5/0.375
$\overline{CLR}$	Clear	0.5/0.375
CP	Clock Input	0.5/0.75

Functional Description

The 'F825 consists of eight D-type edge-triggered flip-flops. This device has 3-state true outputs for bus systems, organized in a broadside pinning. In addition to the clock and output enable pins, the buffered clock (CP) and buffered Output Enable ($\overline{OE}$) are common to all flip-flops. The flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH CP transition. With the $\overline{OE}$ LOW, the contents of the flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops. The 'F825 has Clear ($\overline{CLR}$) and Clock Enable ($\overline{EN}$) pins. These pins are ideal for parity bus interfacing in high performance systems.

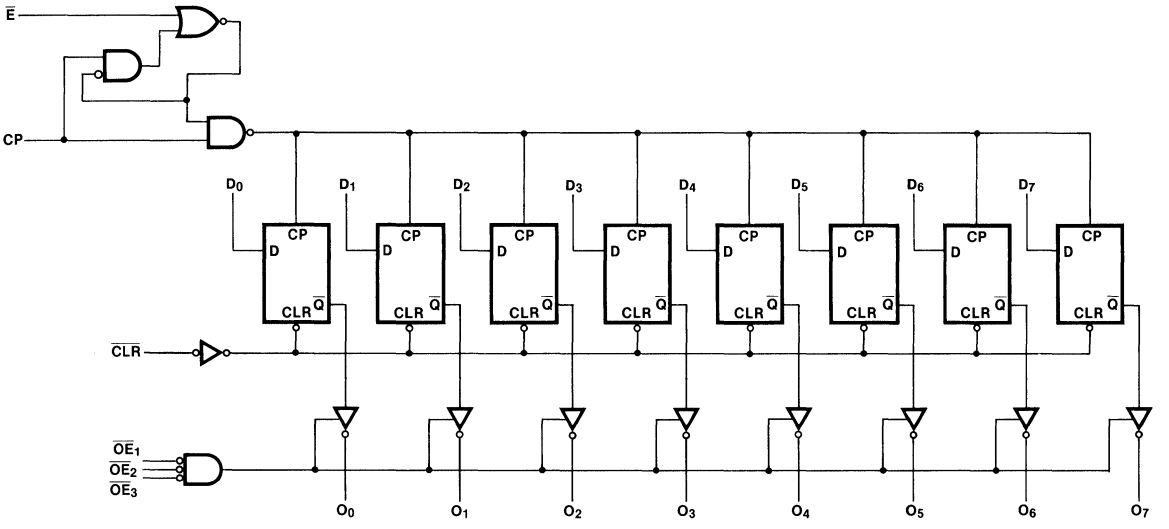
When the $\overline{CLR}$ is LOW and the $\overline{OE}$ is LOW the outputs are LOW. When $\overline{CLR}$ is HIGH, data can be entered into the flip-flops. When $\overline{EN}$ is LOW, data on the inputs is transferred to the outputs on the LOW-to-HIGH clock transition. When the $\overline{EN}$ is HIGH the outputs do not change state, regardless of the data or clock input transitions.

Function Table

Inputs					Internal	Output	Function
$\overline{OE}$	$\overline{CLR}$	EN	CP	D	Q	O	
H	X	L	↑	L	L	Z	High Z
H	X	L	↑	H	H	Z	High Z
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	Clear
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	Hold
H	H	L	↑	L	L	Z	Load
H	H	L	↑	H	H	Z	Load
L	H	L	↑	L	L	L	Load
L	H	L	↑	H	H	H	Load

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
↑ = LOW-to-HIGH Transition
NC = No Change

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current			86	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF	T_A, V_{CC} = Mil, C_L = 50 pF	T_A, V_{CC} = Com, C_L = 50 pF		
		Min Typ Max	Min Max	Min Max		
f_{max}	Maximum Clock Frequency	100			MHz	3-1,
t_{PLH} t_{PHL}	Propagation Delay CP to O_n	7.5 9.5			ns	3-1 3-7
t_{PHL}	Propagation Delay $\overline{CLR}$ to O_n	15.0			ns	3-1 3-9
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	11.5 7.5			ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n	7.0 5.5				

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW D to CP	2.0 2.0			ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D to CP	2.0 2.0				
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{EN}$ to CP	3.0 3.0			ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{EN}$ to CP	0 0				
$t_w(H)$ $t_w(L)$	CP Pulse Width HIGH or LOW	5.0 5.0			ns	3-7
$t_w(L)$	$\overline{CLR}$ Pulse Width, LOW	5.0			ns	3-9
t_{rec}	$\overline{CLR}$ Recovery Time	5.0			ns	3-11

54F/74F827 • 54F/74F828

10-Bit Buffers/Line Drivers

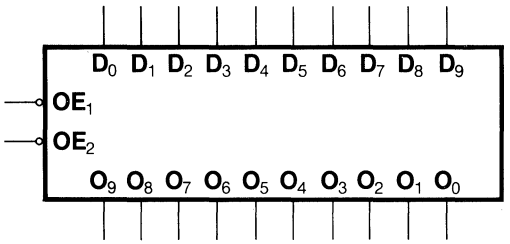
Description

The 'F827 and 'F828 10-bit bus buffers provide high performance bus interface buffering for wide data/address paths or buses carrying parity. The 10-bit buffers have NOR output enables for maximum control flexibility.

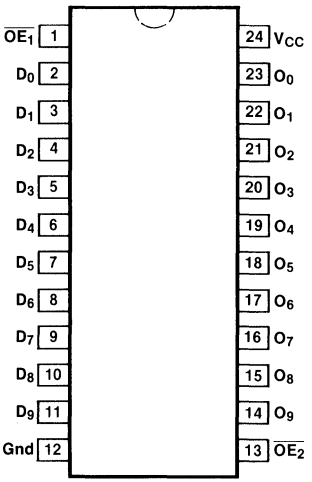
The 'F827 and 'F828 are functionally and pin compatible to AMD's 29827 and 29828. The 'F828 is an inverting inversion of the 'F827.

Ordering Code: See Section 5

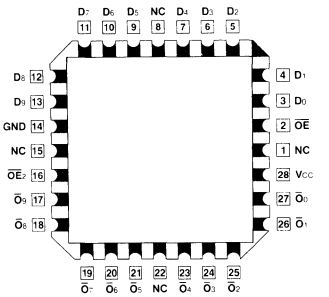
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
$\overline{OE}_1$, $\overline{OE}_2$	Output Enable	0.5/0.375
D_0-D_7	Data Inputs	0.5/0.375
O_0-O_7	Data Outputs	75/40 (30)

Functional Description

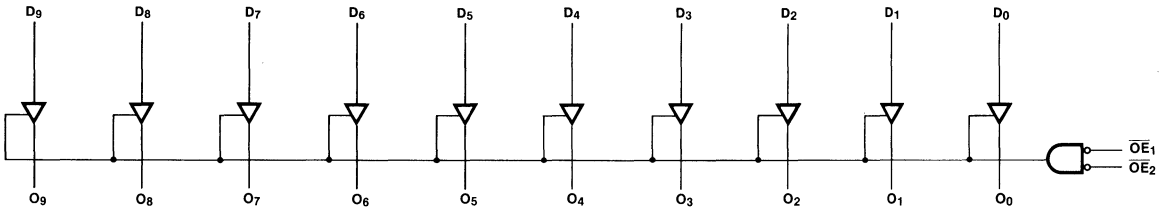
The 'F827 and 'F828 are line drivers designed to be employed as memory address drivers, clock drivers and bus oriented transmitters/receivers which provide improved PC board density. The devices have 3-state outputs controlled by the Output Enable ($\overline{OE}$) pins. The outputs can sink 64 mA and source 15 mA. Input clamp diodes limit high speed termination effects.

Function Table

Inputs		Outputs		Function
		O_n		
$\overline{OE}$	D_n	'F827	'F828	
L	H	H	L	Transparent
L	L	L	H	Transparent
H	X	Z	Z	High Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CCH}	Power Supply Current		40	60	mA	V_{CC} = Max
I_{CCL}			60	90		
I_{CCZ}			60	90		

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay			6.0					ns	3-1
t_{PHL}	Data to Output ('F827)			5.0						3-4
t_{PLH}	Propagation Delay			5.0					ns	3-1
t_{PHL}	Data to Output ('F828)			5.0						3-3
t_{PZH}	Output Enable Time			7.0					ns	3-1
t_{PZL}	$\overline{OE}$ to O_n			8.0						3-12
t_{PHZ}	Output Disable Time			7.0						3-13
t_{PLZ}	$\overline{OE}$ to O_n			8.0						

54F/74F841

10-Bit Transparent Latch

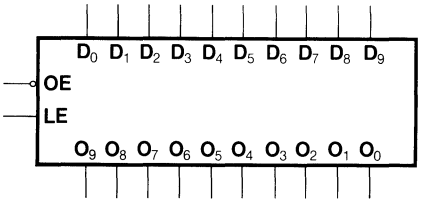
Description

The 'F841 bus interface latch is designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The 'F841 is a 10-bit transparent latch, a 10-bit version of the 'F373.

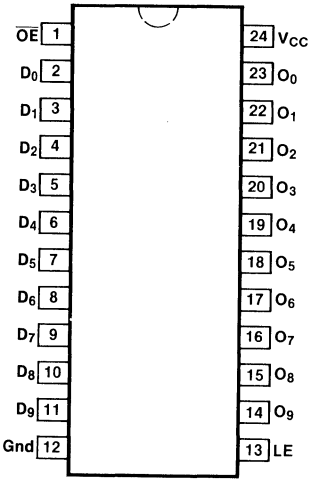
The 'F841 is functionally and pin compatible to AMD's AM29841.

Ordering Code: See Section 5

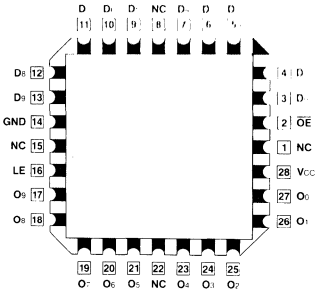
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
D_0-D_9	Data Inputs	0.5/0.375
O_0-O_9	Data Outputs	75/15 (12.5)
$\overline{OE}$	Output Enable	0.5/0.375
LE	Latch Enable	0.5/0.375

Functional Description

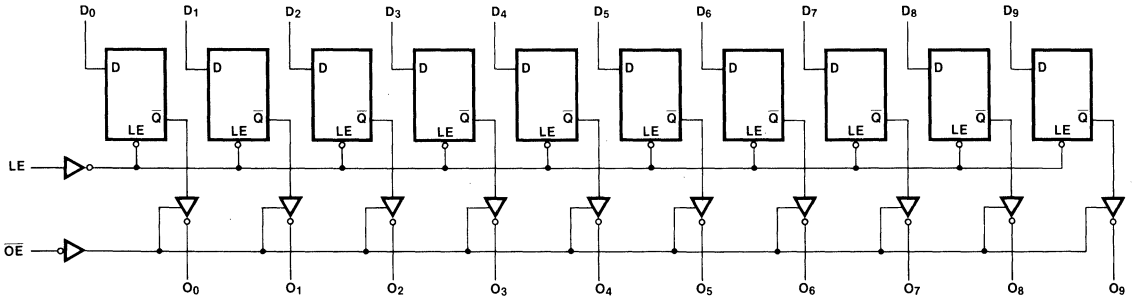
The 'F841 device consists of ten D-type latches with 3-state outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. This allows asynchronous operation, as the output transition follows the data in transition. On the LE HIGH-to-LOW transition, the data that meets the setup and hold time is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH the bus output is in the high impedance state.

Function Table

Inputs			Internal	Output	Function
$\overline{OE}$	LE	D	Q	O	
X	X	X	X	Z	High Z
H	H	L	L	Z	High Z
H	H	H	H	Z	High Z
H	L	X	NC	Z	Latched
L	H	L	L	L	Transparent
L	H	H	H	H	Transparent
L	L	X	NC	NC	Latched
L	X	X	H	H	Preset
L	X	X	L	L	Clear
L	X	X	H	H	Preset
H	L	X	L	Z	Latched
H	L	X	H	Z	Latched

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = HIGH Impedance
NC = No Change

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		50	75	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF	T_A, V_{CC} = Mil, C_L = 50 pF	T_A, V_{CC} = Com, C_L = 50 pF		
		Min Typ Max	Min Max	Min Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to O_n	8.0 6.0			ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay LE to O_n	13.0 8.0			ns	3-1 3-7
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	11.0 8.0			ns	3-1 3-12
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n	7.0 5.0				3-13

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
t_s(H) t_s(L)	Setup Time, HIGH or LOW D_n to LE	3.0 3.0			ns	3-15
t_h(H) t_h(L)	Hold Time, HIGH or LOW D_n to LE	3.0 3.0				
t_w(H)	LE Pulse Width, HIGH	4.0			ns	3-7

54F/74F843

9-Bit Transparent Latch

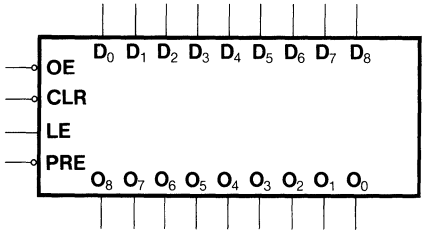
Description

The 'F843 bus interface latch is designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity.

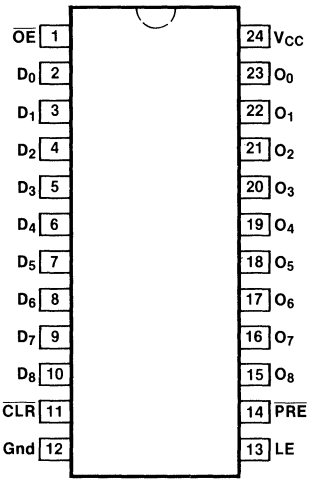
The 'F843 is functionally and pin compatible with AMD's AM29843.

Ordering Code: See Section 5

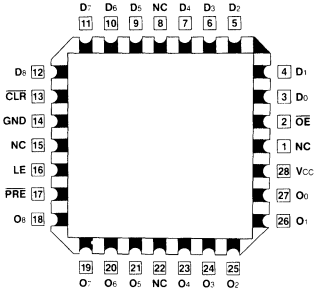
Logic Symbol



Connection Diagram



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
D_0-D_8	Data Inputs	0.5/0.375
O_0-O_8	Data Outputs	75/15 (12.5)
$\overline{OE}$	Output Enable	0.5/0.375
LE	Latch Enable	0.5/0.375
$\overline{CLR}$	Clear	0.5/0.375
$\overline{PRE}$	Preset	0.5/0.375

Functional Description

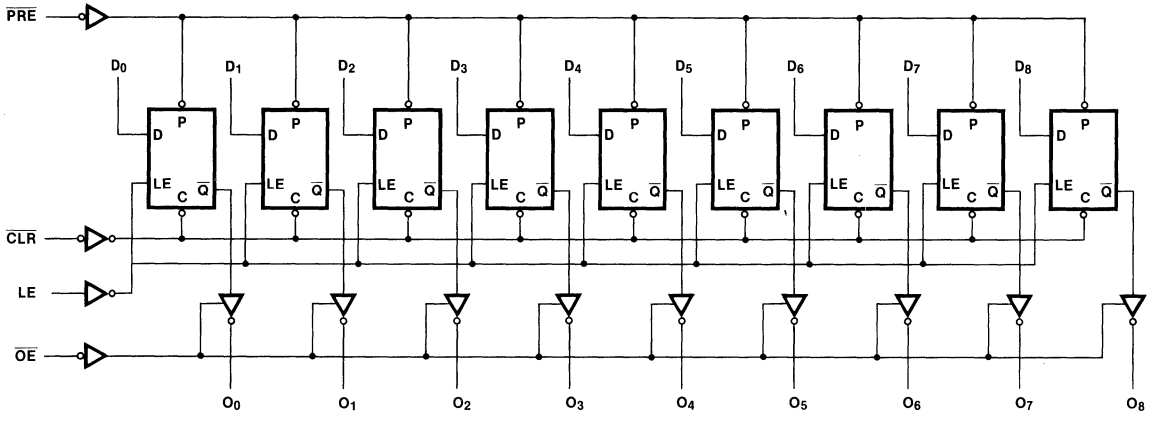
The 'F843 consists of nine D-type latches with 3-state outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. This allows asynchronous operation, as the output transition follows the data in transition. On the LE HIGH-to-LOW transition, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state. In addition to the LE and $\overline{OE}$ pins, the 'F843 has a Clear ($\overline{CLR}$) pin and a Preset ($\overline{PRE}$) pin. These pins are ideal for parity bus interfacing in high performance systems. When $\overline{CLR}$ is LOW, the outputs are LOW if $\overline{OE}$ is LOW. When $\overline{CLR}$ is HIGH, data can be entered into the latch. When $\overline{PRE}$ is LOW, the outputs are HIGH if $\overline{OE}$ is LOW. Preset overrides $\overline{CLR}$.

Function Tables

Inputs					Internal	Output	Function
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	LE	D	Q	O	
H	H	X	X	X	X	Z	High Z
H	H	H	H	L	L	Z	High Z
H	H	H	H	H	H	Z	High Z
H	H	H	L	X	NC	Z	Latched
H	H	L	H	L	L	L	Transparent
H	H	L	H	H	H	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Latched
H	L	H	L	X	H	Z	Latched

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
NC = No Change

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		50	75	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF	T_A, V_{CC} = Mil, C_L = 50 pF	T_A, V_{CC} = Com, C_L = 50 pF		
		Min Typ Max	Min Max	Min Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to O_n	8.0 6.0			ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay LE to O_n	13.0 8.0			ns	3-1 3-7
t_{PLH}	Propagation Delay $\overline{PRE}$ to O_n	9.0			ns	3-1 3-7
t_{PHL}	Propagation Delay $\overline{CLR}$ to O_n	18.0			ns	3-1 3-9
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	11.0 8.0			ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n	7.0 5.0				

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW D_n to LE	3.0 3.0			ns	3-15
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D_n to LE	3.0 3.0				
$t_w(H)$	LE Pulse Width, HIGH	4.0			ns	3-7
$t_w(L)$	$\overline{PRE}$ Pulse width, LOW	5.0			ns	3-9
$t_w(L)$	$\overline{CLR}$ Pulse Width, LOW	6.0			ns	3-9
t_{rec}	$\overline{PRE}$ Recovery Time	12.0			ns	3-11
t_{rec}	$\overline{CLR}$ Recovery Time	12.0			ns	3-11

54F/74F845

8-Bit Transparent Latch

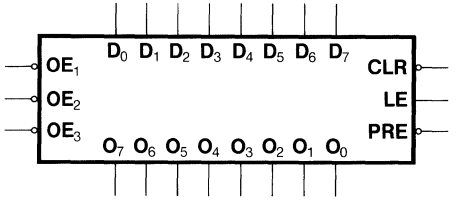
Description

The 'F845 bus interface latch is designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity.

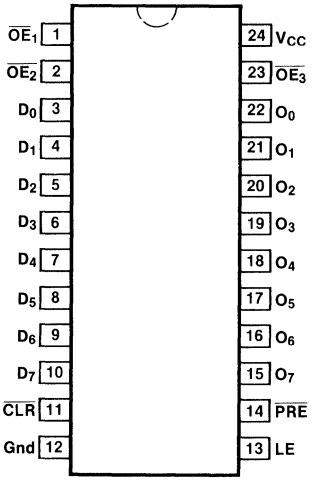
The 'F845 is functionally and pin compatible with AMD's AM29845.

Ordering Code: See Section 5

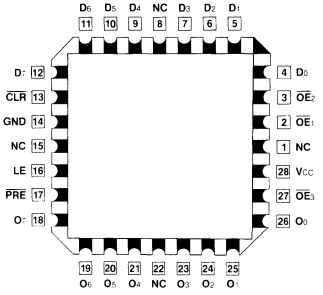
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
D_0-D_7	Data Inputs	0.5/0.375
O_0-O_7	Data Outputs	75/15 (12.5)
$\overline{OE}_1$-$\overline{OE}_3$	Output Enables	0.5/0.375
LE	Latch Enable	0.5/0.375
$\overline{CLR}$	Clear	0.5/0.375
$\overline{PRE}$	Preset	0.5/0.375

Functional Description

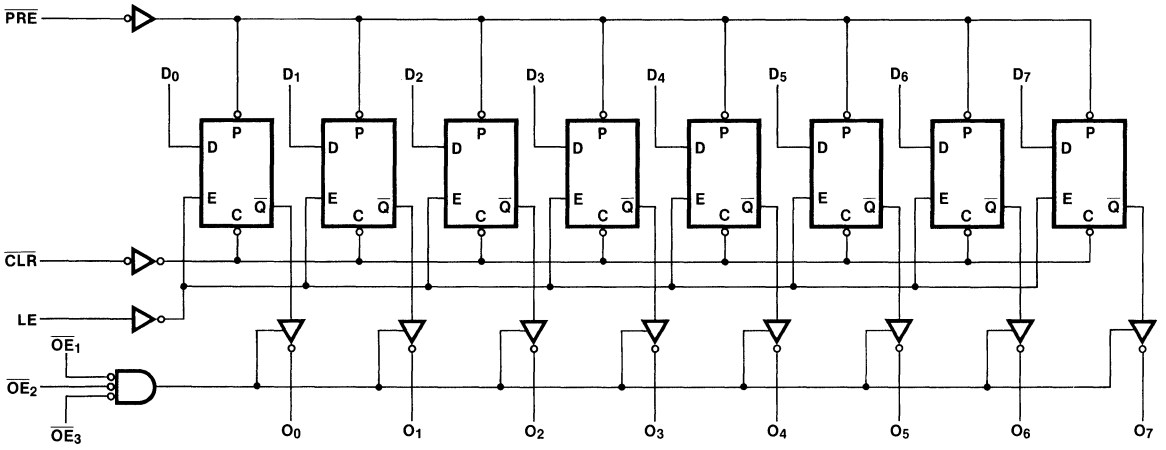
The 'F845 consists of eight D-type latches with 3-state outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. This allows asynchronous operation as the output transition follows the data in transition. On the LE HIGH-to-LOW transition the data that meets the setup times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state.

Function Table

Inputs					Internal	Output	Function
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	LE	D	Q	O	
H	H	H	X	X	X	Z	High Z
H	H	H	H	L	L	Z	High Z
H	H	H	H	H	H	Z	High Z
H	H	H	L	X	NC	Z	Latched
H	H	L	H	L	L	L	Transparent
H	H	L	H	H	H	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Latched
H	L	H	L	X	H	Z	Latched

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
NC = No Change

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		50	75	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$	T_A, V_{CC} = Mil $C_L = 50\ pF$	T_A, V_{CC} = Com $C_L = 50\ pF$		
		Min Typ Max	Min Max	Min Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to O_n	8.0 6.0			ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay LE to O_n	13.0 8.0			ns	3-1 3-7
t_{PLH}	Propagation Delay $\overline{PRE}$ to O	9.0			ns	3-1 3-7
t_{PHL}	Propagation Delay $\overline{CLR}$ to O	18.0			ns	3-1 3-9
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	11.0 8.0			ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n	7.0 5.0				

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$ $t_s(L)$	Setup Time, High or LOW D_n to LE	3.0 3.0			ns	3-15
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D_n to LE	3.0 3.0				
$t_w(H)$	LE Pulse Width, HIGH	4.0			ns	3-7
$t_w(L)$	$\overline{PRE}$ Pulse Width, LOW	5.0			ns	3-9
$t_w(L)$	$\overline{CLR}$ Pulse Width, LOW	6.0			ns	3-9
t_{rec}	$\overline{PRE}$ Recovery Time	12.0			ns	3-11
t_{rec}	$\overline{CLR}$ Recovery Time	12.0			ns	3-11

29F01

4-Bit Bipolar Microprocessor Slice

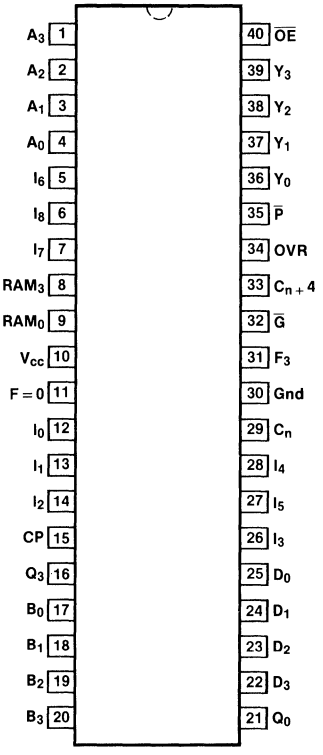
Description

The 29F01 is a 4-bit high-speed bipolar microprocessor slice. It features a 16-word by 4-bit dual-port Random Access Memory (RAM), a high-speed 8-function Arithmetic Logic Unit (ALU) and associated shifting, decoding and multiplexing circuitry. The microinstruction word consists of three groups of three bits that respectively control ALU operand source, ALU function and ALU result destination. Width of the data path may be increased by cascading with either ripple or full lookahead carry. Data outputs are 3-state for maximum versatility. Four status flag signals, carry, overflow, zero and sign, are provided by the ALU. The microprocessor slice is compatible with Fairchild Advanced Schottky TTL (FAST) devices and can be used along with FAST parts in microprogrammed systems to minimize cycle times.

- **Isoplanar FAST Technology**
- **Plug-In Replacement for Standard 2901 C Version**
- **20% to 30% Faster than Standard 2901 in Most System Configurations**

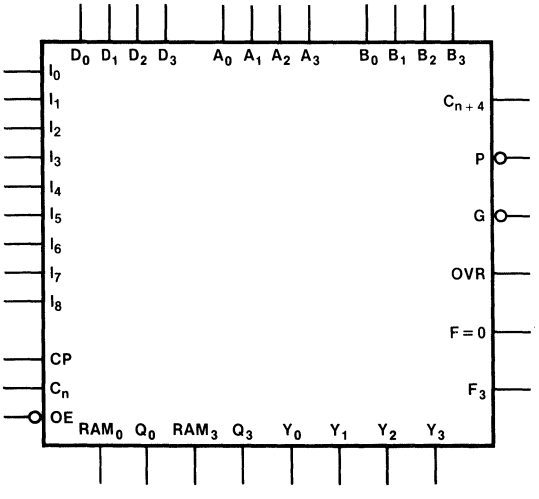
Ordering Code: See Section 5

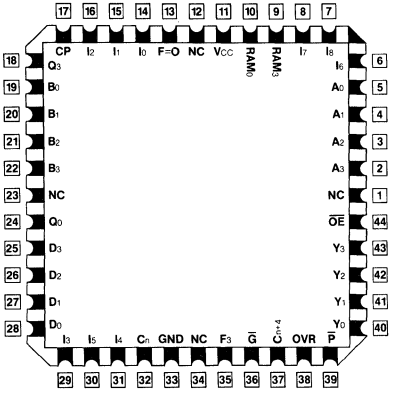
Connection Diagrams



Pin Assignment for DIP

Logic Symbol





Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	29F(U.L.) HIGH/LOW
A_0-A_3	A Address Inputs	0.5/0.375
B_0-B_3	B Address Inputs	0.5/0.375
I_0-I_8	Instruction Control Lines	0.5/0.375
Q_0, Q_3	Shift Lines	0.5/0.375
RAM_0, RAM_3	Shift Lines	0.5/0.375
D_0-D_3	Direct Data Field	0.5/0.375
Y_0-Y_3	Data Outputs	25/12.5
$\overline{OE}$	Output Enable	0.5/0.375
$\overline{P}$	Carry Propagate Output	25/12.5
$\overline{G}$	Carry Generate Output	25/12.5
OVR	Overflow	0.5/0.375
F = 0	ALU Operation Output	25/12.5
F_3	Most Significant ALU Output Bit	25/12.5
C_n	Carry-In	0.5/0.375
C_{n+4}	Carry-Out	0.5/0.375
CP	Clock	0.5/0.375

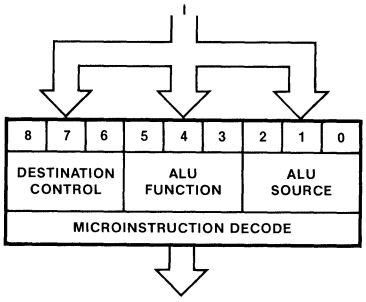
4

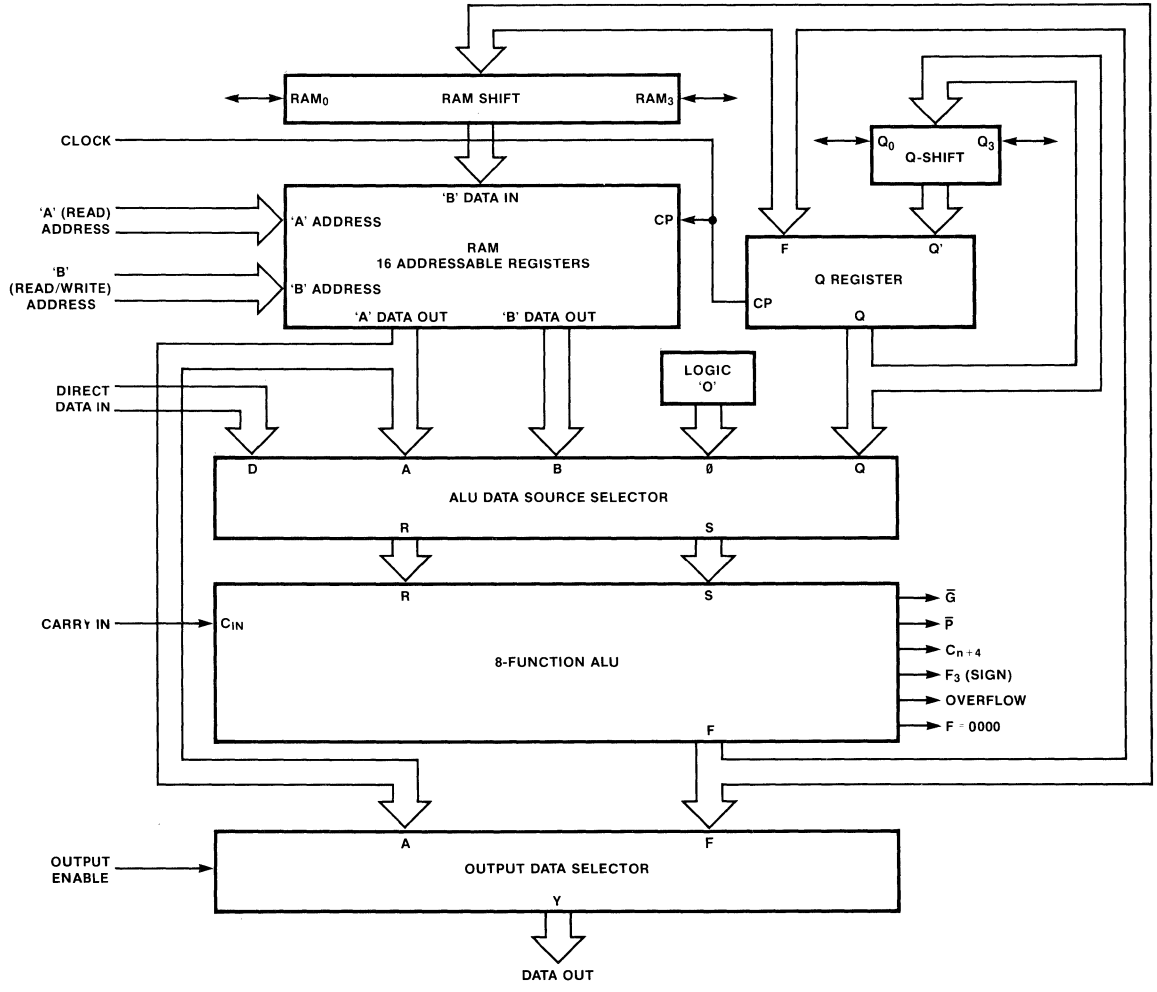
ALU Logic Functions

I_{543}	Function	$\overline{P}$	$\overline{G}$	C_{n+4}	OVR
0	R+S	$\overline{P_3P_2P_1P_0}$	$\overline{G_3+P_3G_2+P_3P_2G_1+P_3P_2P_1G_0}$	C_4	$C_3 \veebar C_4$
1	S-R	← Same as R+S equations, but substitute $\overline{R_i}$ for R_i in definitions →			
2	R-S	← Same as R+S equations, but substitute $\overline{S_i}$ for S_i in definitions →			
3	R V S	LOW	$P_3P_2P_1P_0$	$\overline{P_3P_2P_1P_0}+C_n$	$\overline{P_3P_2P_1P_0}+C_n$
4	R Λ S	LOW	$\overline{G_3+G_2+G_1+G_0}$	$G_3+G_2+G_1+G_0+C_n$	$G_3+G_2+G_1+G_0+C_n$
5	$\overline{R}$ Λ S	LOW	Same as R Λ S equations, but substitute $\overline{R_i}$ for R in definitions		
6	R ⊻ S	← Same as $R \veebar S$, but substitute $\overline{R_i}$ for R_i in definitions →			
7	$\overline{R \veebar S}$	$G_3+G_2+G_1+G_0$	$G_3+P_3G_2+P_3P_2G_1+P_3P_2P_1P_0$	$\overline{\overline{G_3+P_3G_2+P_3P_2G_1}+P_3P_2P_1P_0\,(G_0+\overline{C_n})}$	See note

Note: $\lceil \overline{P_2+\overline{G_2}P_1+\overline{G_2}\,\overline{G_1}P_0+\overline{G_2}\,\overline{G_1}\,\overline{G_0}C_n} \rfloor \veebar \lceil \overline{P_3+\overline{G_3}P_2+\overline{G_3}\,\overline{G_2}P_1+\overline{G_3}\,\overline{G_2}\,\overline{G_1}P_0+\overline{G_3}\,\overline{G_2}\,\overline{G_1}\,\overline{G_0}C_n} \rfloor$ + = OR

Block Diagram





Source Operand and ALU Function Matrix

Octal $I_{5,4,3}$ / $I_{2,1,0}$ Octal	0	1	2	3	4	5	6	7
ALU Function \ ALU Source	A, Q	A, B	O, Q	O, B	O, A	D, A	D, Q	D, O
0 $C_n = L$ R Plus S	A+Q	A+B	Q	B	A	D+A	D+Q	D
0 $C_n = H$	A+Q+1	A+B+1	Q+1	B+1	A+1	D+A+1	D+Q+1	D+1
1 $C_n = L$ S Minus R	Q−A−1	B−A−1	Q−1	B−1	A−1	A−D−1	Q−D−1	−D−1
1 $C_n = H$	Q−A	B−A	Q	B	A	A−D	Q−D	−D
2 $C_n = L$ R Minus S	A−Q−1	A−B−1	−Q−1	−B−1	−A−1	D−A−1	D−Q−1	D−1
2 $C_n = H$	A−Q	A−B	−Q	−B	−A	D−A	D−Q	D
3 R OR S	A V Q	A V B	Q	B	A	D V A	D V Q	D
4 R AND S	A ∧ Q	A ∧ B	0	0	0	D ∧ A	D ∧ Q	0
5 $\overline{R}$ AND S	$\overline{A}$ ∧ Q	$\overline{A}$ ∧ B	Q	B	A	$\overline{D}$ ∧ A	$\overline{D}$ ∧ Q	0
6 R EX-OR S	A ⊻ Q	A ⊻ B	Q	B	A	D ⊻ A	D ⊻ Q	D
7 R EX-NOR S	$\overline{A \veebar Q}$	$\overline{A \veebar B}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D \veebar A}$	$\overline{D \veebar Q}$	$\overline{D}$

+ = Plus; − = Minus; V = OR; ∧ = AND; ⊻ = EX-OR

ALU Function Control

Mnemonic	Micro Code I_5	I_4	I_3	Octal Code	ALU Function	Symbol
ADD	L	L	L	0	R Plus S	R + S
SUBR	L	L	H	1	S Minus R	S − R
SUBS	L	H	L	2	R Minus S	R − S
OR	L	H	H	3	R OR S	R v S
AND	H	L	L	4	R AND S	R ∧ S
NOTRS	H	L	H	5	$\overline{R}$ AND S	$\overline{R}$ ∧ S
EXOR	H	H	L	6	R EX-OR S	R ⊻ S
EXNOR	H	H	H	7	R EX-NOR S	$\overline{R \veebar S}$

Definitions (+ = OR)

$P_0 = R_0 + S_0$ $\quad G_0 = R_0 S_0$
$P_1 = R_1 + S_1$ $\quad G_1 = R_1 S_1$
$P_2 = R_2 + S_2$ $\quad G_2 = R_2 S_2$
$P_3 = R_3 + S_3$ $\quad G_3 = R_3 S_3$
$C_4 = G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0 + P_3 P_2 P_1 P_0 C_n$
$C_3 = G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_n$

ALU Source Operand Control

Mnemonic	Micro Code I_2	I_1	I_0	Octal Code	ALU Source Operands R	S
AQ	L	L	L	0	A	Q
AB	L	L	H	1	A	B
ZQ	L	H	L	2	O	Q
ZB	L	H	H	3	O	B
ZA	H	L	L	4	O	A
DA	H	L	H	5	D	A
DQ	H	H	L	6	D	Q
DZ	H	H	H	7	D	O

Logic Functions for $\overline{G}$, $\overline{P}$, C_{n+4}, and OVR

The four signals $\overline{G}$, $\overline{P}$, C_{n+4}, and OVR are designed to indicate carry and overflow conditions when the 29F01 is in the add or subtract mode. The table below indicates the logic equations for these four signals for each of the eight ALU functions. The R and S inputs are the two inputs selected according to the ALU source operand code.

ALU Destination Control

Mnemonic	Micro Code				RAM Function		Q-Reg. Function		Y Output	RAM Shifter		Q Shifter	
	I_8	I_7	I_6	Octal Code	Shift	Load	Shift	Load		RAM_0	RAM_3	Q_0	Q_3
QREG	L	L	L	0	X	None	None	F → Q	F	X	X	X	X
NOP	L	L	H	1	X	None	X	None	F	X	X	X	X
RAMA	L	H	L	2	None	F → B	X	None	A	X	X	X	X
RAMF	L	H	H	3	None	F → B	X	None	F	X	X	X	X
RAMQD	H	L	L	4	Down	F/2 → B	Down	Q/2 → Q	F	F_0	IN_3	Q_0	IN_3
RAMD	H	L	H	5	Down	F/2 → B	X	None	F	F_0	IN_3	Q_0	X
RAMQU	H	H	L	6	Up	2F → B	Up	2Q → Q	F	IN_0	F_3	IN_0	Q_3
RAMU	H	H	H	7	Up	2F → B	X	None	F	IN_0	F_3	X	Q_3

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

B = Register addressed by B inputs
Up is toward MSB
Down is toward LSB

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	29F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current			250	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	29F			Military 29F		Commercial 29F		Units
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency	25					25		MHz
t_{PLH} t_{PHL}	Propagation Delay A or B to Y		45.0 45.0					45.0 45.0	ns
t_{PLH} t_{PHL}	Propagation Delay A or B to F_3		46.0 46.0					46.0 46.0	ns
t_{PLH} t_{PHL}	Propagation Delay A or B to C_{n+4}		47.0 47.0					47.0 47.0	ns
t_{PLH} t_{PHL}	Propagation Delay A or B to $\overline{G}$ or $\overline{P}$		43.0 43.0					43.0 43.0	ns

AC Characteristics (Cont'd)

Symbol	Parameter	29F	Military 29F	Commercial 29F	Units
		$T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$	T_A, V_{CC} = Mil $C_L = 50\ pF$	T_A, V_{CC} = Com $C_L = 50\ pF$	
		Min Typ Max	Min Max	Min Max	
t_{PLH} t_{PHL}	Propagation Delay A or B to F = 0	55.0 55.0		55.0 55.0	ns
t_{PLH} t_{PHL}	Propagation Delay A or B to OVR	50.0 50.0		50.0 50.0	ns
t_{PLH} t_{PHL}	Propagation Delay A or B to RAM	48.0 48.0		48.0 48.0	ns
t_{PLH} t_{PHL}	Propagation Delay D to Y	34.0 34.0		34.0 34.0	ns
t_{PLH} t_{PHL}	Propagation Delay D to F_3	40.0 40.0		40.0 40.0	ns
t_{PLH} t_{PHL}	Propagation Delay D to C_{n+4}	34.0 34.0		34.0 34.0	ns
t_{PLH} t_{PHL}	Propagation Delay D to $\overline{G}$ or $\overline{P}$	32.0 32.0		32.0 32.0	ns
t_{PLH} t_{PHL}	Propagation Delay D to F = 0	42.0 42.0		42.0 42.0	ns
t_{PLH} t_{PHL}	Propagation Delay D to OVR	35.0 35.0		35.0 35.0	ns
t_{PLH} t_{PHL}	Propagation Delay D to RAM	31.0 31.0		31.0 31.0	ns
t_{PLH} t_{PHL}	Propagation Delay C_n to Y	24.0 24.0		24.0 24.0	ns
t_{PLH} t_{PHL}	Propagation Delay C_n to F_3	34.0 34.0		34.0 34.0	ns
t_{PLH} t_{PHL}	Propagation Delay C_n to C_{n+4}	24.0 24.0		24.0 24.0	ns
t_{PLH} t_{PHL}	Propagation Delay C_n to F = 0	38.0 38.0		38.0 38.0	ns
t_{PLH} t_{PHL}	Propagation Delay C_n to OVR	26.0 26.0		26.0 26.0	ns
t_{PLH} t_{PHL}	Propagation Delay C_n to RAM	29.0 29.0		29.0 29.0	ns

AC Characteristics (Cont'd)

Symbol	Parameter	29F			Military 29F		Commercial 29F		Units
		$T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$			T_A, V_{CC} = Mil $C_L = 50\ pF$		T_A, V_{CC} = Com $C_L = 50\ pF$		
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay $I_{0,1,2}$ to Y			39.0 39.0				39.0 39.0	ns
t_{PLH} t_{PHL}	Propagation Delay $I_{0,1,2}$ to F_3			43.0 43.0				43.0 43.0	ns
t_{PLH} t_{PHL}	Propagation Delay $I_{0,1,2}$ to C_{n+4}			39.0 39.0				39.0 39.0	ns
t_{PLH} t_{PHL}	Propagation Delay $I_{0,1,2}$ to $\overline{G}$ or $\overline{P}$			44.0 44.0				44.0 44.0	ns
t_{PLH} t_{PHL}	Propagation Delay $I_{0,1,2}$ to F = 0			49.0 49.0				49.0 49.0	ns
t_{PLH} t_{PHL}	Propagation Delay $I_{0,1,2}$ to OVR			44.0 44.0				44.0 44.0	ns
t_{PLH} t_{PHL}	Propagation Delay $I_{0,1,2}$ to RAM			40.0 40.0				40.0 40.0	ns
t_{PLH} t_{PHL}	Propagation Delay $I_{3,4,5}$ to Y			41.0 41.0				41.0 41.0	ns
t_{PLH} t_{PHL}	Propagation Delay $I_{3,4,5}$ to F_3			39.0 39.0				39.0 39.0	ns
t_{PLH} t_{PHL}	Propagation Delay $I_{3,4,5}$ to C_{n+4}			45.0 45.0				45.0 45.0	ns
t_{PLH} t_{PHL}	Propagation Delay $I_{3,4,5}$ to $\overline{G}$ or $\overline{P}$			42.0 42.0				42.0 42.0	ns
t_{PLH} t_{PHL}	Propagation Delay $I_{3,4,5}$ to F = 0			48.0 48.0				48.0 48.0	ns
t_{PLH} t_{PHL}	Propagation Delay $I_{3,4,5}$ to OVR			50.0 50.0				50.0 50.0	ns
t_{PLH} t_{PHL}	Propagation Delay $I_{3,4,5}$ to RAM			38.0 38.0				38.0 38.0	ns
t_{PLH} t_{PHL}	Propagation Delay $I_{6,7,8}$ to Y			24.0 24.0				24.0 24.0	ns

AC Characteristics (Cont'd)

Symbol	Parameter	29F			Military 29F		Commercial 29F		Units
		$T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$			T_A, V_{CC} = Mil $C_L = 50\ pF$		T_A, V_{CC} = Com $C_L = 50\ pF$		
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay $I_{6,7,8}$ to RAM			30.0 30.0				30.0 30.0	ns
t_{PLH} t_{PHL}	Propagation Delay $I_{6,7,8}$ to Q			32.0 32.0				32.0 32.0	ns
t_{PLH} t_{PHL}	Propagation Delay CP to Y			37.0 37.0				37.0 37.0	ns
t_{PLH} t_{PHL}	Propagation Delay CP to F_3			41.0 41.0				41.0 41.0	ns
t_{PLH} t_{PHL}	Propagation Delay CP to C_{n+4}			39.0 39.0				39.0 39.0	ns
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{G}$ or $\overline{P}$			42.0 42.0				42.0 42.0	ns
t_{PLH} t_{PHL}	Propagation Delay CP to F = 0			51.0 51.0				51.0 51.0	ns
t_{PLH} t_{PHL}	Propagation Delay CP to OVR			45.0 45.0				45.0 45.0	ns
t_{PLH} t_{PHL}	Propagation Delay CP to RAM			37.0 37.0				37.0 37.0	ns
t_{PLH} t_{PHL}	Propagation Delay CP to Q			23.0 23.0				23.0 23.0	ns
t_{PLH} t_{PHL}	Propagation Delay A to Y Bypassing ALU			28.0 28.0				28.0 28.0	ns
t_{PHZ} t_{PLZ}	Output Enable Time $\overline{OE}$ to Y			15.0 15.0				15.0 15.0	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Y, $C_L = 5\ pF$			13.0 13.0				13.0 13.0	ns
t_{PZH} t_{PZL}	Output Disable Time $\overline{OE}$ to Y			38.0 38.0				38.0 38.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to Y, $C_L = 5\ pF$			19.0 19.0				19.0 19.0	ns

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	29F	Military 29F	Commercial 29F	Units
		$T_A = +25°C$ $V_{CC} = +5.0\,V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com	
		Min Typ Max	Min Max	Min Max	
t_s Before HL	Setup Time A or B Source to CP	11.0		11.0	ns
t_h After LH	Hold Time A or B Source to CP	0		0	
t_s Before HL t_s Before LH	Setup Time B Destinations to CP	11.0 Do not change*		11.0 Do not change*	ns
t_h After HL t_h After LH	Hold Time B Destinations to CP	Do not change* 0		Do not change* 0	
t_s Before LH	Setup Time D to CP	23.0		23.0	ns
t_h After LH	Hold Time D to CP	0		0	
t_s Before LH	Setup Time C_n to CP	15.0		15.0	ns
t_h After LH	Hold Time C_n to CP	0		0	
t_s Before LH	Setup Time $I_{0,1,2}$ to CP	25.0		25.0	ns
t_h After LH	Hold Time $I_{0,1,2}$ to CP	0		0	
t_s Before LH	Setup Time $I_{3,4,5}$ to CP	37.0		37.0	ns
t_h After LH	Hold Time $I_{3,4,5}$ to CP	0		0	
t_s Before HL t_s Before LH	Setup Time $I_{6,7,8}$ to CP	4.0 Do not change*		4.0 Do not change*	ns
t_h After HL t_h After LH	Hold Time $I_{6,7,8}$ to CP	Do not change* 1.0		Do not change* 1.0	

*Once the HIGH-to-LOW CP transition occurs, no change is allowed until the CP is again HIGH.

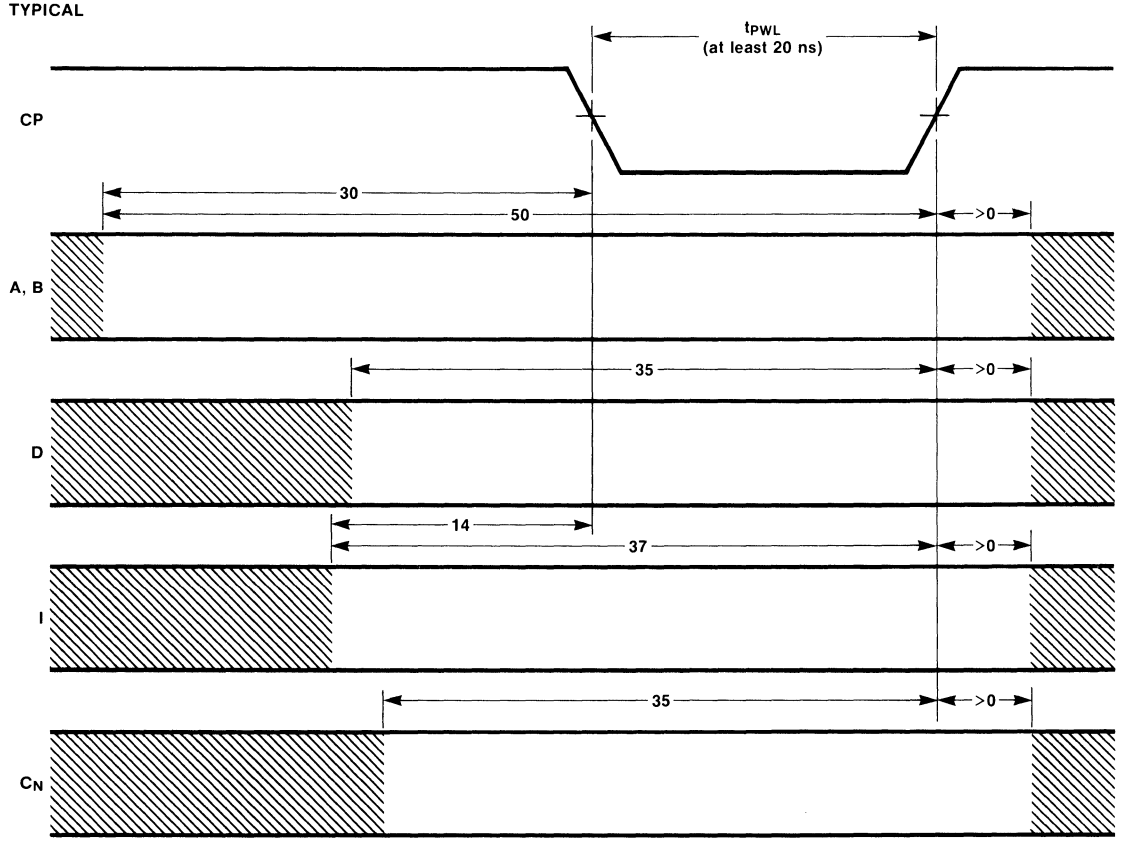
AC Operating Requirements (Cont'd)

Symbol	Parameter	29F	Military 29F	Commercial 29F	Units
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com	
		Min Typ Max	Min Max	Min Max	
t_s Before LH	Setup Time RAM or Q to CP	6.0		6.0	ns
t_h After LH	Hold Time RAM or Q to CP	2.0		2.0	
$t_w(H)$ $t_w(L)$	CP Pulse Width HIGH or LOW	11.0 9.0		11.0 9.0	ns

4

Timing Waveforms

TYPICAL



29F10

Microprogram Controller

Description

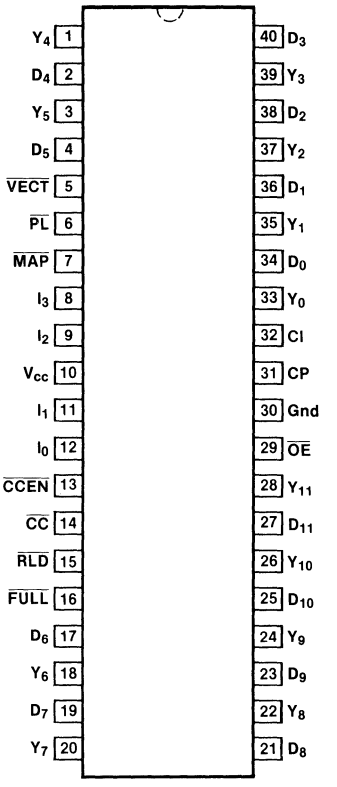
The 29F10 is a high-speed bipolar microprogram controller. It is intended for use in controlling the sequence of execution of microinstructions stored in microprogram memory. The 29F10 provides a 12-bit address during each clock cycle. This address comes from one of four sources: 1) Direct input from D_0-D_{11}; 2) A register/counter; 3) A microprogram counter; or 4) A five-deep LIFO stack. Address outputs are 3-state for maximum versatility.

The microprogram controller is compatible with FAST (Fairchild Advanced Schottky TTL) devices and can be used along with FAST parts in microprogrammed systems to minimize cycle times.

- **Addresses up to 4096 Words of Microcode**
- **Directly Loadable Down-Counter for Counting Loop Iterations**
- **Provides Count Capacity of 4096**
- **An Up Counter Providing Sequential Microinstruction Execution**
- **A 5-Deep Push/Pop LIFO Stack Providing Subroutine Linkage and Branch Capabilities**
- **Registers are all Positive Edge-Triggered**
- **Plug-in Replacement for Standard 2910**

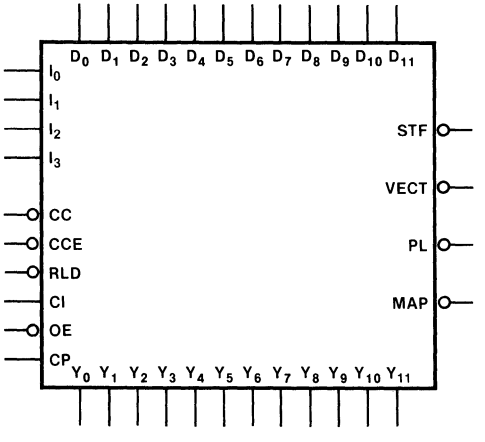
Ordering Code: See Section 5

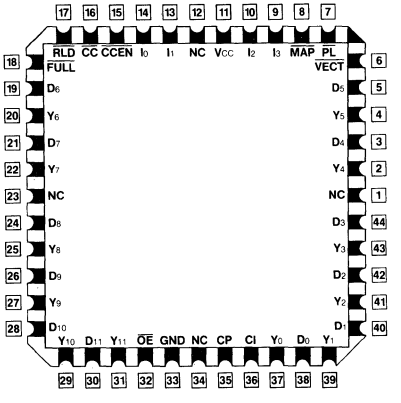
Connection Diagrams



Pin Assignment for DIP

Logic Symbol





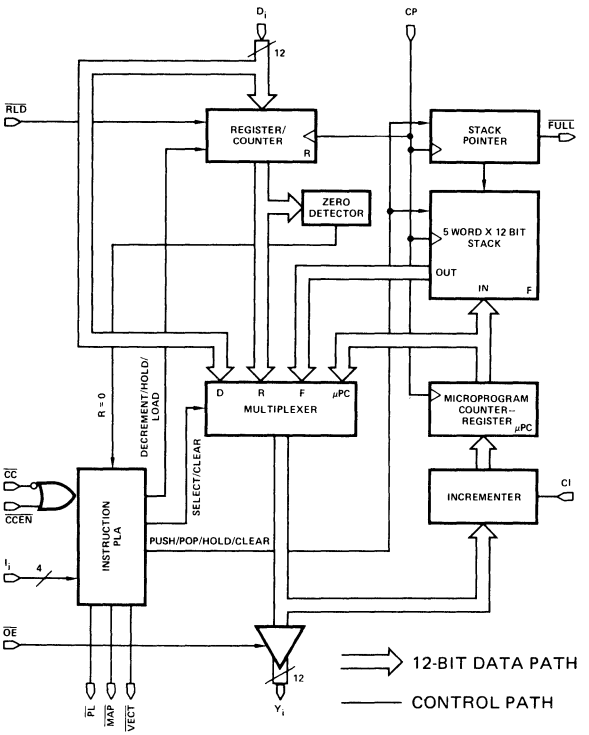
Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	29F(U.L.) HIGH/LOW
D_i	Direct Input	0.5/0.225
I_i	Instruct Bit	0.5/0.225
$\overline{CC}$	Condition Code	0.5/0.225
$\overline{CCEN}$	Condition Code Enable	0.5/0.225
$\overline{CI}$	Carry-In	0.5/0.225
$\overline{RLD}$	Register Load	0.5/0.225
$\overline{OE}$	Output Enable	0.5/0.450
CP	Clock Pulse	1.0/0.788
Y_0-Y_{11}	Microprogram Address Bits	0.5/0.225
$\overline{FULL}$	Status Full	0.5/0.225
$\overline{PL}$	Pipeline Address Enable	0.5/0.225
$\overline{MAP}$	Map Address Enable	0.5/0.225
$\overline{VECT}$	Vector Address Enable	0.5/0.225

4

Block Diagram



Instruction Set

The 29F10 provides sixteen instructions which select the address of the next microinstruction to be executed. Four of the instructions are unconditional—their effect depends only on the instruction. Ten of the instructions have an effect which is partially controlled by an external, data-dependent condition. Three of the instructions have an effect which is partially controlled by the contents of the internal register/counter. The instruction set is shown in Table 1. In this discussion it is assumed that CI is tied HIGH.

In the ten conditional instructions, the result of the data-dependent test is applied to $\overline{CC}$. If the $\overline{CC}$ input is LOW, the test is considered to have been passed and the action specified in the name occurs; otherwise, the test has failed and an alternate operation (often simply the execution of the next sequential microinstruction) occurs. Testing of $\overline{CC}$ may be disabled for a specific microinstruction by setting $\overline{CCEN}$ HIGH, which unconditionally forces the action specified in the name; that is, it forces a pass. Other ways of using $\overline{CCEN}$ include (1) tying it HIGH, which is useful if no microinstruction is data-dependent; (2) tying it LOW if data-dependent instructions are never forced unconditionally; or (3) tying it to the source of 29F10 instruction bit I_0, which leaves instructions 4, 6, and 10 as data-dependent but makes others unconditional. All of these tricks save one bit of microcode width.

The effect of three instructions depends on the contents of the register/counter. Unless the counter holds a value of zero, it is decremented; if it does hold zero, it is held and a different microprogram next address is selected. These instructions are useful for executing a microinstruction loop a known number of times. Instruction 15 is affected both by the external condition code and the internal register/counter.

Perhaps the best technique for understanding the 29F10 is to simply take each instruction and review its operation. In order to provide some feel for the actual execution of these instructions, Figure a is included and depicts examples of all sixteen instructions.

The examples given in Figure a should be interpreted in the following manner: The intent is to show microprogram flow as various microprogram memory words are executed. For example, the CONTINUE instruction, instruction number 14, as shown in Figure a, simply means that the contents of microprogram memory word 50 are executed, then the contents of word 51 are executed. This is followed by the contents of microprogram memory word 52 and the contents of microprogram memory word 53. The microprogram addresses used in the examples were arbitrarily chosen and have no meaning other than to show instruction flow. The exception to this is the first example, JUMP ZERO, which forces the microprogram location counter to address ZERO. Each dot refers to the time that the contents of the microprogram memory word are in the pipeline register. While no special symbology is used for the conditional instructions, the text to follow will explain what the conditional choices are in each example.

Instruction 0, JZ (JUMP and ZERO, or RESET) unconditionally specifies that the address of the next microinstruction is zero. Many designs use this feature for power-up sequences and provide the power-up firmware beginning at microprogram memory word location 0.

Instruction 1 is a CONDITIONAL JUMP-TO-SUBROUTING via the address provided in the pipeline register. As shown in Figure a, the machine might have executed words at address 50, 51, and 52. When the contents of address 52 are in the pipeline register, the next address control function is the CONDITIONAL JUMP-TO-SUBROUTINE. Here, if the test is passed, the next instruction executed will be the contents of microprogram memory location 90. If the test has failed, the JUMP-TO-SUBROUTINE will not be executed; the contents of microprogram memory location 53 will be executed instead. Thus, the CONDITIONAL JUMP-TO-SUBROUTINE instruction at location 52 will cause the instruction either in location 90 or in location 53 to be executed next. If the TEST input is such that location 90 is selected, value 53 will be pushed onto the internal stack. This provides the return linkage for the machine when the subroutine beginning at location 90 is completed. In this example, the subroutine was completed at location 93 and a RETURN-FROM-SUBROUTINE would be found at location 93.

Instruction 2 is the JUMP MAP instruction. This is an unconditional instruction which causes the $\overline{MAP}$ output to be enabled so that the next

microinstruction location is determined by the address supplied via the mapping PROMs. Normally, the JUMP MAP instruction is used at the end of the instruction fetch sequence for the machine. In the example of Figure a, microinstructions at locations 50, 51, 52, and 53 might have been the fetch sequence and at its completion at location 53, the jump map function would be contained the pipeline register. This example shows the mapping PROM outputs to be 90; therefore, an unconditional jump to microprogram memory address 90 is performed.

Instruction 3, CONDITIONAL JUMP PIPELINE, derives its branch address from the pipeline register branch address value. This instruction provides a technique for branching to various microprogram sequences depending upon the test condition inputs. Quite often, state machines are designed which simply execute tests on various inputs waiting for the condition to come true. When the true condition is reached, the machine then branches and executes a set of microinstructions to perform some function. This usually has the effect of resetting the input being tested until some point in the future. Figure a shows the conditional jump via the pipeline register address at location 52. When the contents of microprogram memory word 52 are in the pipeline register, the next address will be either location 53 or location 30 in this example. If the test is passed, the value currently in the pipeline register (30) will be selected. If the test fails, the next address selected will be contained in the microprogram counter which, in this example, is 53.

Instruction 4 is the PUSH/CONDITIONAL LOAD COUNTER instruction and is used primarily for setting up loops in microprogram firmware. In Figure a, when instruction 52 is in the pipeline register, a PUSH will be made onto the stack and the counter will be loaded based on the condition. When a PUSH occurs, the value pushed is always the next sequential instruction address. In this case, the address is 53. If the test fails, the counter is not loaded; if it is passed, the counter is loaded with the value contained in the pipeline register branch address field. Thus, a single microinstruction can be used to set up a loop to be executed a specific number of times. Instruction 8 will describe how to use the pushed value and the register/counter for looping.

Instruction 5 is a CONDITIONAL JUMP-TO-SUBROUTINE via the register/counter or the contents of the PIPELINE register. As shown in Figure a, a PUSH is always performed and one of two subroutines executed. In this example, either the subroutine beginning at address 80 or the subroutine beginning at address 90 will be performed. A return-from-subroutine (instruction number 10) returns the microprogram flow to address 55. In order for this microinstruction control sequence to operate correctly, both the next address fields of instruction 53 and the next address fields of instruction 54 would have to contain the proper value. Let's assume that the branch address fields of instruction 53 contain the value 90 so that it will be in the 29F10 register/counter when the contents of address 54 are in the pipeline register. This requires that the instruction at address 53 load the register/counter. Now, during the execution of instruction 5 (at address 54), if the test failed, the contents of the register (value = 90) will select the address of the next microinstruction. If the test input passes, the pipeline register contents (value = 80) will determine the address of the next microinstruction. Therefore, this instruction provides the ability to select one of two subroutines to be executed based on a test condition.

Instruction 6 is a CONDITIONAL JUMP VECTOR instruction which provides the capability to take the branch address from a third source heretofore not discussed. In order for this instruction to be useful, the 29F10 output, $\overline{\text{VECT}}$ is used to control a 3-state control input of a register, buffer, or PROM containing the next microprogram address. This instruction provides one technique for performing interrupt type branching at the microprogram level. Since this instruction is conditional, a pass causes the next address to be taken from the vector source, while failure causes the next address to be taken from the microprogram counter. In the example of Figure a, if the CONDITIONAL JUMP VECTOR instruction is contained at location 52, execution will continue at vector address 20 if the $\overline{\text{CC}}$ input is LOW and the microinstruction at address 53 will be executed if the $\overline{\text{CC}}$ input is HIGH.

Instruction 7 is a CONDITIONAL JUMP via the contents of the 29F10 REGISTER/COUNTER or the contents of the PIPELINE register. This instruction is very similar to instruction 5; the conditional

jump-to-subroutine via R or PL. The major difference between instruction 5 and instruction 7 is that no push onto the stack is perfomed with instruction 7. Figure a depicts this instruction as a branch to one of two locations depending on the test condition. The example assumes the pipeline register contains the value 70 when the contents of address 52 are being executed. As the contents of address 53 are clocked into the pipeline register, the value 70 is loaded into the register/counter in the 29F10. The value 80 is available when the contents of address 53 are in the pipeline register. Thus, control is transferred to either address 70 or address 80 depending on the test condition.

Instruction 8 is the REPEAT LOOP, COUNTER ZERO instruction. This microinstruction makes use of the decrementing capability of the register/counter. To be useful, some previous instruction, such as 4, must have loaded a count value into the register/counter. This instruction checks to see whether the register/counter contains a non-zero value. If so, the register/counter is decremented, and the address of the next microinstruction is taken from the top of the stack. If the register counter contains zero, the loop exit condition is occuring; control falls through to the next sequential microinstruction by selecting μPC; the stack is POPed by decrementing the stack pointer, but the contents of the top of the stack are thrown away.

An example of the REPEAT LOOP, COUNTER ZERO instruction is shown in Figure a. In this example, location 50 most likely would contain a PUSH/CONDITIONAL LOAD COUNTER instruction which would have caused address 51 to be PUSHed on the stack and the counter to be loaded with the proper value for looping the desired number of times.

In this example, since the loop test is made at the end of the instructions to be repeated (microaddress 54), the proper value to be loaded by the instructions at address 50 is one less than the desired number of passes through the loop. This method allows a loop to be executed 1 to 4096 times. If it is desired to execute the loop from 0 to 4095 times, the firmware should be written to make the loop exit test immediately after loop entry.

Single-microinstruction loops provide a highly efficient capability for executing a specific microinstruction a fixed number of times. Examples include fixed rotates, byte swap, fixed point multiply, and fixed point divide.

Instruction 9 is the REPEAT PIPELINE REGISTER, COUNTER ZERO instruction. This instruction is similar to instruction 8 except that the branch address now comes from the pipeline register rather than the file. In some cases, this instruction may be thought of as a one-word file extension; that is, by using this instruction, a loop with the counter can still be performed when subroutines are nested five deep. This instruction's operation is very similar to that of instruction 8. The differences are that on this instruction a failed test condition causes the source of the next microinstruction address to be the D inputs, and when the test condition is passed, this instruction does not perform a POP because the stack is not being used.

In the example of Figure a, the REPEAT PIPELINE, COUNTER ZERO instruction is instruction 52 and is shown as a single microinstruction loop. The address in the pipeline register would be 52. Instruction 51 in this example could be the LOAD COUNTER AND CONTINUE instruction (number 12). While the example shows a single microinstruction loop, by simply changing the address in a pipeline register, multi-instruction loops can be performed in this manner for a fixed number of times as determined by the counter.

Instruction 10 is the conditional RETURN-FROM-SUBROUTINE instruction. As the name implies, this instruction is used to branch from the subroutine back to the next microinstruction address following the subroutine call. Since this instruction is conditional, the return is performed only if the test is passed. If the test is failed, the next sequential microinstruction is performed. The example in Figure a depicts the use of the conditional RETURN-FROM-SUBROUTINE instruction in both the conditional and the unconditional modes. This example first shows a jump-to-subroutine at instruction location 52 where control is transferred to location 90. At location 93, a conditional RETURN-FROM-SUBROUTINE instruction is performed. If the test is passed, the stack is accessed and the program will transfer to the next instruction at address 53. If the test if failed, the next microinstruction at address 94 will be executed. The program will continue to address

97 where the subroutine is complete. To perform an unconditional RETURN-FROM-SUBROUTINE, the conditional RETURN-FROM-SUBROUTINE instruction is executed unconditionally; the microinstruction at address 97 is programmed to force $\overline{CCEN}$ HIGH, disabling the test and the forced PASS causes an unconditional return.

Instruction 11 is the CONDITIONAL JUMP PIPELINE register address and POP stack instruction. This instruction provides another technique for loop termination and stack maintenance. The example in Figure a shows a loop being performed from address 55 back to address 51. The instructions at location 52, 53, and 54 are all conditional JUMP and POP instructions. At address 52, if the $\overline{CC}$ input is LOW, a branch will be made to address 70 and the stack will be properly maintained via a POP. Should the test fail, the instruction at location 53 (the next sequential instruction) will be executed. Likewise, at address 53, either the instruction at 90 or 54 will be subsequently executed, respective to the test being passed or failed. The instruction at 54 follows the same rules, going to either 80 or 55. An instruction sequence as described here, using the CONDITIONAL JUMP PIPELINE and POP instruction, is very useful when several inputs are being tested and the microprogram is looping waiting for any of the inputs being tested to occur before proceeding to another sequence of instructions. This provides the powerful jump-table programming technique at the firmware level.

Instruction 12 is the LOAD COUNTER AND CONTINUE instruction, which simply enables the counter to be loaded with the value at its parallel inputs. These inputs are normally connected to the pipeline branch address field which (in the architecture being described here) serves to supply either a branch address or a counter value depending upon the microinstruction being executed. There are altogether three ways of loading the counter—the explicit load by this instruction 12; the conditional load included as part of instruction 4; and the use of the $\overline{RDL}$ input along with any instruction. The use of $\overline{RDL}$ with any instruction overrides any counting or decrementation specified in the instruction, calling for a load instead. Its use provides additional microinstruction power, at the expense of one bit of microinstruction width. This instruction 12 is exactly equivalent to the combination of instruction 14 and $\overline{RLD}$ LOW. Its purpose is to provide a simple capability to load the register/counter in those implementations which do not provide microprogrammed control for $\overline{RDL}$.

Instruction 13 is the TEST END-OF-LOOP instruction, which provides the capability of conditionally exiting a loop at the bottom; that is, this is a conditional instruction that will cause the microprogram to loop, via the file, if the test is failed else to continue to the next sequential instruction. The example in Figure a shows the TEST END-OF-LOOP microinstruction at address 56. If the test fails, the microprogram will branch to address 52. Address 52 is on the stack because a PUSH instruction had been executed at address 51. If the test is passed at instruction 56, the loop is terminated and the next sequential microinstruction at address 57 is executed, which also causes the stack to be POPed, thus accomplishing the required stack maintenance.

Instruction 14 is the CONTINUE instruction, which simply causes the microprogram counter to increment so that the next sequential microinstruction is executed. This is the simplest microinstruction of all and should be the default instruction which the firmware requests whenever no other instruction is being executed.

Instruction 15, THREE-WAY BRANCH, is the most complex. It provides for testing of both a data-dependent condition and the counter during one microinstruction and provides for selecting among one of three microinstruction addresses as the next microinstruction to be performed. Like instruction 8, a previous instruction will have loaded a count into the register/counter while pushing a microbranch address onto the stack. Instruction 15 performs a decrement-and-branch-until-zero function similar to intruction 8. The next address is taken from the top of the stack until the count reaches zero; then the next address comes from the pipeline register. The above action continues as long as the test condition fails. If at any execution of instruction 15 the test condition is passed, no branch is taken; the microprogram counter register furnishes the next address. When the loop is ended, either by the count becoming zero or by passing the conditional test, the stack is POPed by decrementing the stack pointer, since interest in the value contained at the top of the stack is then complete.

The application of instruction 15 can enhance performance of a variety of machine-level instructions. For instance, (1) a memory search instruction to be terminated either by finding a desired memory content or by reaching the search limit; (2) variable-field-length arithmetic terminated early upon finding that the content of the portion of the field still unprocessed is all zeroes; (3) key search in a disc controller processing variable length records; (4) normalization of a floating point number.

As one example, consider the case of a memory search instruction. As shown in Figure a, the instruction at microprogram address 63 can be Instruction 4 (PUSH), which will push the value 64 onto the microprogram stack and load the number N, which is one less than the number of memory locations to be searched before giving up. Location 64 contains a microinstruction which fetches the next operand from the memory area to be searched and compares it with the search key. Location 65 contains a microinstruction which tests the result of the comparison and also is a THREE-WAY BRANCH for microprogram control. If no match is found, the test fails and the microprogram goes back to location 64 for the next operand address. When the count becomes zero, the microprogram branches to location 72, which does whatever is necessary if no match is found. If a match occurs on any execution of the THREE-WAY BRANCH at location 65, control falls through to location 66 which handles this case. Whether the instruction ends by finding a match or not, the stack will have been POPed once, removing the value 64 from the top of the stack.

Table 1 Instruction Set

				Fail $\overline{CCEN}$ = LOW and $\overline{CC}$ = HIGH		Pass $\overline{CCEN}$ = HIGH or $\overline{CC}$ = LOW			
I_3-I_0	Mnemonic	Name	Reg/ Cntr Contents	Y	Stack	Y	Stack	Reg/ Cntr	Enable
0	JZ	JUMP ZERO	X	0	CLEAR	0	CLEAR	HOLD	PL
1	CJS	COND JSB PL	X	PC	HOLD	D	PUSH	HOLD	PL
2	JMAP	JUMP MAP	X	D	HOLD	D	HOLD	HOLD	MAP
3	CJP	COND JUMP PL	X	PC	HOLD	D	HOLD	HOLD	PL
4	PUSH	PUSH/COND LD CNTR	X	PC	PUSH	PC	PUSH	Note 1	PL
5	JSRP	COND JSB R/PL	X	R	PUSH	D	PUSH	HOLD	PL
6	CJV	COND JUMP VECTOR	X	PC	HOLD	D	HOLD	HOLD	VECT
7	JRP	COND JUMP R/PL	X	R	HOLD	D	HOLD	HOLD	PL
8	RFCT	REPEAT LOOP, CNTR ≠ 0	≠ 0	F	HOLD	F	HOLD	DEC	PL
			= 0	PC	POP	PC	POP	HOLD	PL
9	RPCT	REPEAT PL, CNTR ≠ 0	≠ 0	D	HOLD	D	HOLD	DEC	PL
			= 0	PC	HOLD	PC	HOLD	HOLD	PL
10	CRTN	COND RTN	X	PC	HOLD	F	POP	HOLD	PL
11	CJPP	COND JUMP PL & POP	X	PC	HOLD	D	POP	HOLD	PL
12	LDCT	LD CNTR & CONTINUE	X	PC	HOLD	PC	HOLD	LOAD	PL
13	LOOP	TEST END LOOP	X	F	HOLD	PC	POP	HOLD	PL
14	CONT	CONTINUE	X	PC	HOLD	PC	HOLD	HOLD	PL
15	TWB	THREE-WAY BRANCH	≠ 0	F	HOLD	PC	POP	DEC	PL
			= 0	D	POP	PC	POP	HOLD	PL

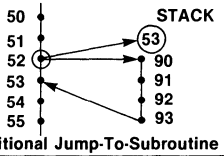
Note 1: If $\overline{CCEN}$ = LOW and $\overline{CC}$ = HIGH, hold: else load. X = Don't Care

Fig. a Execution Examples

INSTRUCTION 0

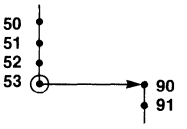
Jump Zero (JZ)

INSTRUCTION 1



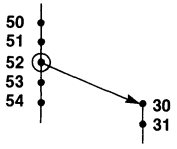
Conditional Jump-To-Subroutine (CJS)

INSTRUCTION 2



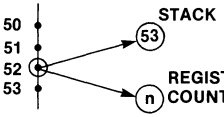
Jump Map (JMAP)

INSTRUCTION 3



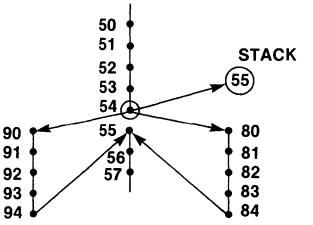
Conditional Jump Pipeline (CJP)

INSTRUCTION 4



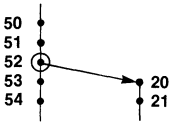
Push/Conditional Load Counter (PUSH)

INSTRUCTION 5



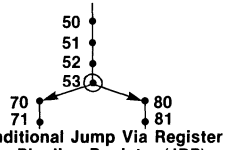
Conditional Jump-To-Subroutine Via Register or Pipeline Register (COND JSB R/PL)

INSTRUCTION 6



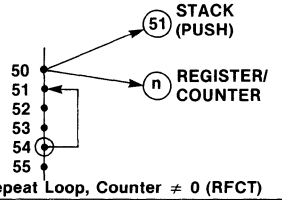
Conditional Jump Vector (CJV)

INSTRUCTION 7



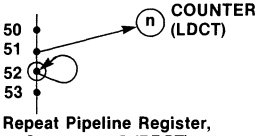
Conditional Jump Via Register or Pipeline Register (JRP)

INSTRUCTION 8



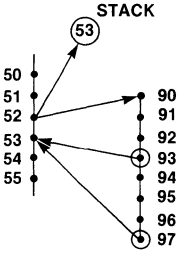
Repeat Loop, Counter ≠ 0 (RFCT)

INSTRUCTION 9



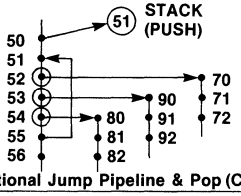
Repeat Pipeline Register, Counter ≠ 0 (RPCT)

INSTRUCTION 10



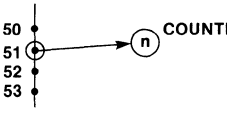
Return From Subroutine (CRTN)

INSTRUCTION 11



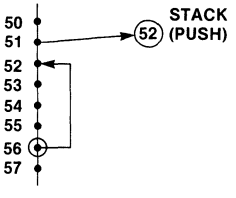
Conditional Jump Pipeline & Pop (CJPP)

INSTRUCTION 12



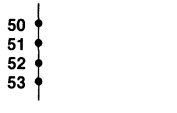
Load Counter and Continue (LDCT)

INSTRUCTION 13



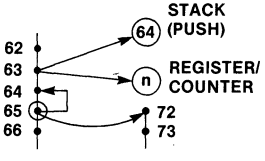
Test End-Of-Loop (LOOP)

INSTRUCTION 14



Continue (CONT)

INSTRUCTION 15



Three-Way Branch (TWB)

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	29F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		195	295	mA	V_{CC} = Max

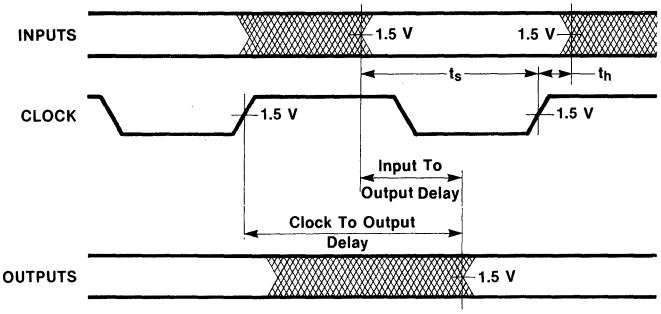
AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	29F T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			Military 29F T_A, V_{CC} = Mil C_L = 50 pF		Commercial 29F T_A, V_{CC} = Com C_L = 50 pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay D_n to Y			26.0 26.0					ns
t_{PLH} t_{PHL}	Propagation Delay I_n to Y			40.0 40.0					ns
t_{PLH} t_{PHL}	Propagation Delay I_n to PL, VECT, MAP			30.0 30.0					ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{CC}$ to Y			35.0 35.0					ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{CCEN}$ to Y			35.0 35.0					ns
t_{PLH} t_{PHL}	Propagation Delay CP to Y			30.0 30.0					ns
t_{PLH} t_{PHL}	Propagation Delay CP (I = 8, 9, 15) to Y			55.0 55.0					ns
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{FULL}$			40.0 40.0					ns
t_{PLH} t_{PHL}	Propagation Delay CP (I = 8, 9, 15) to $\overline{FULL}$			40.0 40.0					ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Y			17.0 17.0					ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to Y			21.0 21.0					ns

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	29F	Military 29F	Commercial 29F	Units
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com	
		Min Typ Max	Min Max	Min Max	
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW D (RC) to CP	7.0 7.0			ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D (RC) to CP	0 0			ns
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW D (PC) to CP	9.0 9.0			ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D (PC) to CP	0 0			ns
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW I_0-I_3 to CP	20.0 20.0			ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW I_0-I_3 to CP	6.0 0			ns
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{CC}$ to CP	21.0 21.0			ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{CC}$ to CP	0 0			ns
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{CCEN}$ to CP	18.0 18.0			ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{CCEN}$ to CP	0 0			ns
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{CI}$ to CP	12.0 12.0			ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{CI}$ to CP	0 0			ns
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{RLD}$ to CP	24.0 24.0			ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{RLD}$ to CP	0 0			ns
$t_w(H)$ $t_w(L)$	Clock Pulse Width HIGH or LOW	8.0 12.0			ns

Fig. b Switching Waveforms



29F52/29F53

8-Bit Registered Transceiver

Description

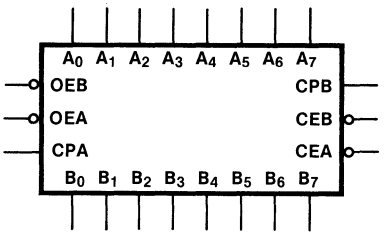
The 29F52 and 29F53 are 8-bit registered transceivers. Two 8-bit back to back registers store data flowing in both directions between two bidirectional buses. Separate clock, clock enable and 3-state output enable signals are provided for each register. The A outputs are guaranteed to sink 20 mA while the B outputs are designed for 64 mA.

The 29F53 is an inverting option of the 29F52. Both transceivers are AM2952/2953 functional equivalents.

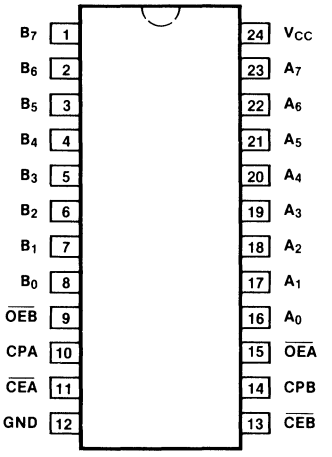
- **Eight Bit Registered Transceivers**
- **Separate Clock, Clock Enable and 3-State Output Enable Provided for Each Register**
- **AM2952/2953 Functional Equivalents**
- **Both Inverting and Non-Inverting Options Available**
- **24-Pin Slim Package**

Ordering Code: See Section 5

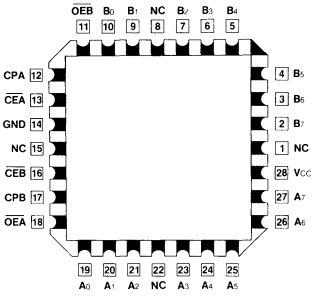
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	29F(U.L.) HIGH/LOW
A_0-A_7	A-Register Inputs	1.75/0.406
	B-Register Outputs	75/40 (30)
B_0-B_7	B-Register Inputs	1.75/0.406
	A-Register Outputs	25/12.5
$\overline{OEA}$	Output Enable A-Register	0.5/0.375
CPA	A-Register Clock	0.5/0.375
$\overline{CEA}$	A-Register Clock Enable	0.5/0.375
$\overline{OEB}$	Output Enable B-Register	0.5/0.375
CPB	B-Register Clock	0.5/0.375
$\overline{CEB}$	B-Register Clock Enable	0.5/0.375

Functional Description

Data applied to the A inputs is entered and stored on the rising edge of the A Clock Pulse (CPA), provided that the A Clock Enable ($\overline{CEA}$) is LOW; simultaneously, the status flip-flop is set and the A-to-B flag (FAB) output goes HIGH. Data thus entered from the A inputs is present at the inputs to the B output buffers, but only appears on the B I/O pins when the B Output Enable ($\overline{OEB}$) signal is made LOW. Data flow from B-to-A proceeds in the same manner as described for A-to-B flow.

Register Function Table

(Applies to A or B Register)

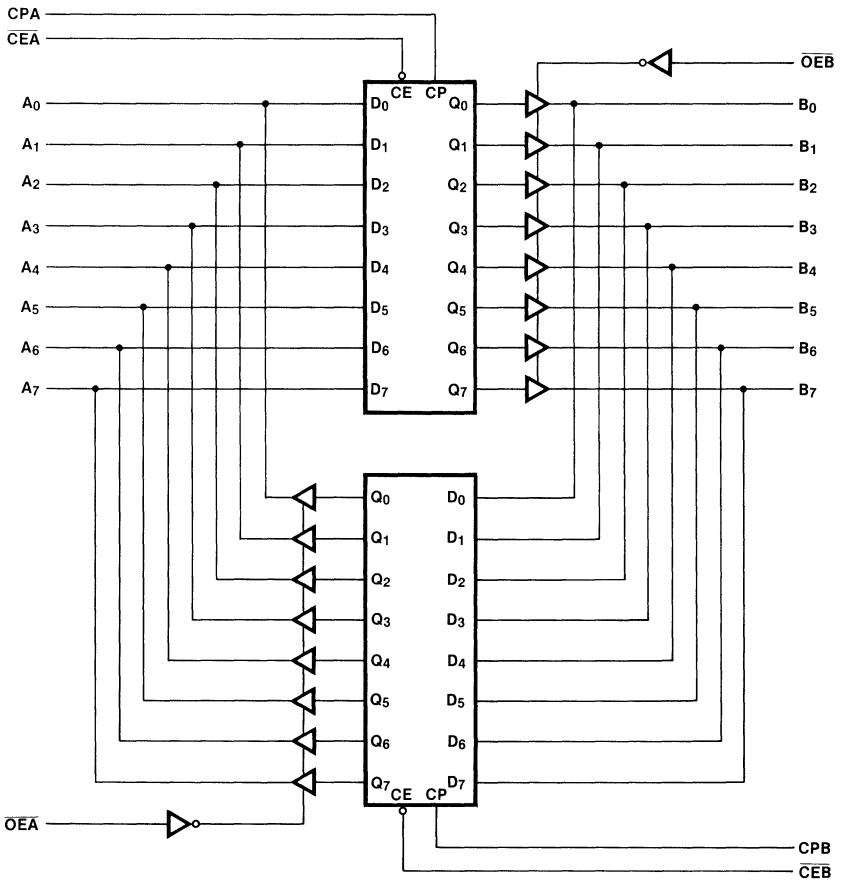
Inputs			Internal	Function
D	CP	$\overline{CE}$	Q	
X	X	H	NC	Hold Data
L	↑	L	L	Load Data
H	↑	L	H	

Output Control

$\overline{OE}$	Internal Q	A or B Outputs		Function
		29F52	29F53	
H	X	Z	Z	Disable Outputs
L	L	L	H	Enable Outputs
L	H	H	L	

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
↑ = LOW-to-HIGH Transition
NC = No Change

Block Diagram



4

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	29F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		130	190	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	29F			Military 29F		Commercial 29F		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$			T_A, V_{CC} = Mil $C_L = 50\ pF$		T_A, V_{CC} = Com $C_L = 50\ pF$			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay CPA, CPB to B_n, A_n	3.0 4.0	5.5 7.0	7.5 9.0			2.5 3.5	8.5 10.0	ns	3-1 3-7
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEA}$ or $\overline{OEB}$ to A_n or B_n	2.5 3.5	5.5 7.0	7.5 9.5			2.0 3.0	8.5 10.5	ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEA}$ or $\overline{OEB}$ to A_n or B_n	3.0 2.5	6.5 5.5	9.0 7.5			2.5 2.0	10.0 8.5		

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	29F			Military 29F		Commercial 29F		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW A_n, B_n to CPA, CPB	4.0 4.0					4.0 4.0		ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW A_n, B_n to CPA, CPB	2.0 2.0					2.0 2.0			
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{CEA}$, $\overline{CEB}$ to CPA, CPB	1.0 4.0					1.0 4.0		ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{CEA}$ or $\overline{CEB}$ to CPA or CPB	2.0 2.0					2.0 2.0			
$t_w(H)$ $t_w(L)$	Pulse Width, HIGH or LOW CPA or CPB	3.0 3.0					3.0 3.0		ns	3-7

29F68

Dynamic RAM Controller

Description

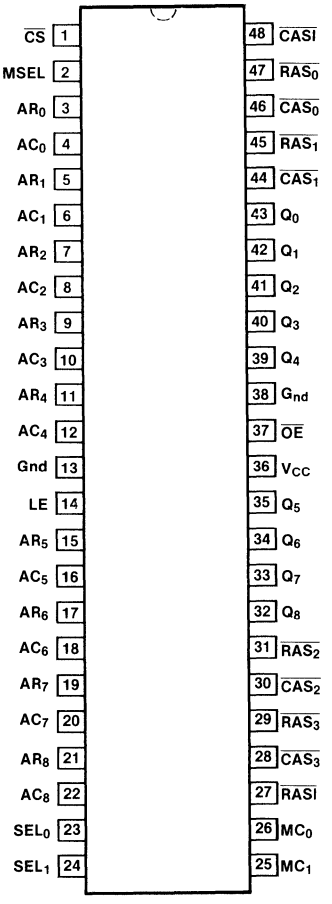
The 29F68 is a high-performance memory controller, replacing many SSI and MSI devices by grouping several unique functions. It provides two 9-bit address latches and two 9-bit counters for row and column address generation during refresh. A 2-bit bank select latch for row and column address generation during refresh, and a 2-bit bank select latch for the two high order address bits are provided to select one of the four RAS and CAS outputs.

The 29F68 is functionally equivalent to AMD's Am2968 and Motorola's MC74F2968.

- **High-Performance Memory Controller**
- **Replaces Many SSI and MSI Devices by Grouping Several Unique Functions**
- **Functionally Equivalent to AMD's Am2968 and Motorola's MC74F2968**
- **Provides Control for 16K, 64K, or 256K Dynamic RAM Systems**
- **Outputs Directly Drive up to 88 DRAMs**
- **Highest Order Two Address Bits Select One of Four Banks of RAMs**
- **Chip Select for Easy Expansion**
- **Provides Memory Scrubbing Refresh Function**

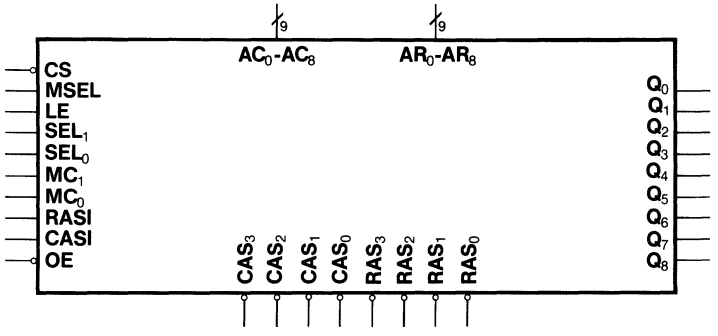
Ordering Code: See Section 5

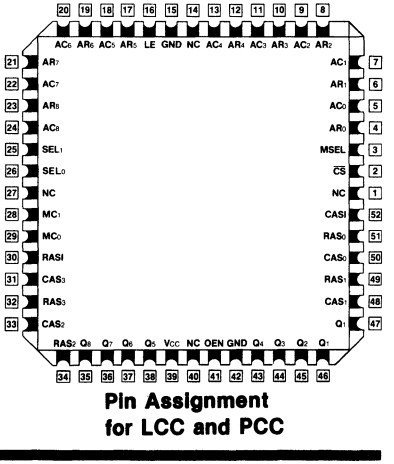
Connection Diagrams



Pin Assignment for DIP

Logic Symbol





Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	29F(U.L.) HIGH/LOW
AC_0-AC_8	Column Address	0.5/0.375
AR_0-AR_8	Row Address	0.5/0.375
Q_0-Q_8	Address Output	25/12.5
MC_0,MC_1	Memory Cycle	0.5/0.375
$\overline{CS}$	Chip Select Input	0.5/0.375
MSEL	Memory Select Input	0.5/0.375
LE	Latch Enable Input	0.5/0.375
SEL_0,SEL_1	Select Inputs	0.5/0.375
RASI	Row Address Strobe In	0.5/0.375
CASI	Column Address Strobe In	0.5/0.375
$\overline{RAS_0}$-$\overline{RAS_3}$	Row Address Strobe Output	25/12.5
$\overline{CAS_0}$-$\overline{CAS_3}$	Column Address Strobe Output	25/12.5
$\overline{OE}$	Output Enable	0.5/0.375

Functional Description

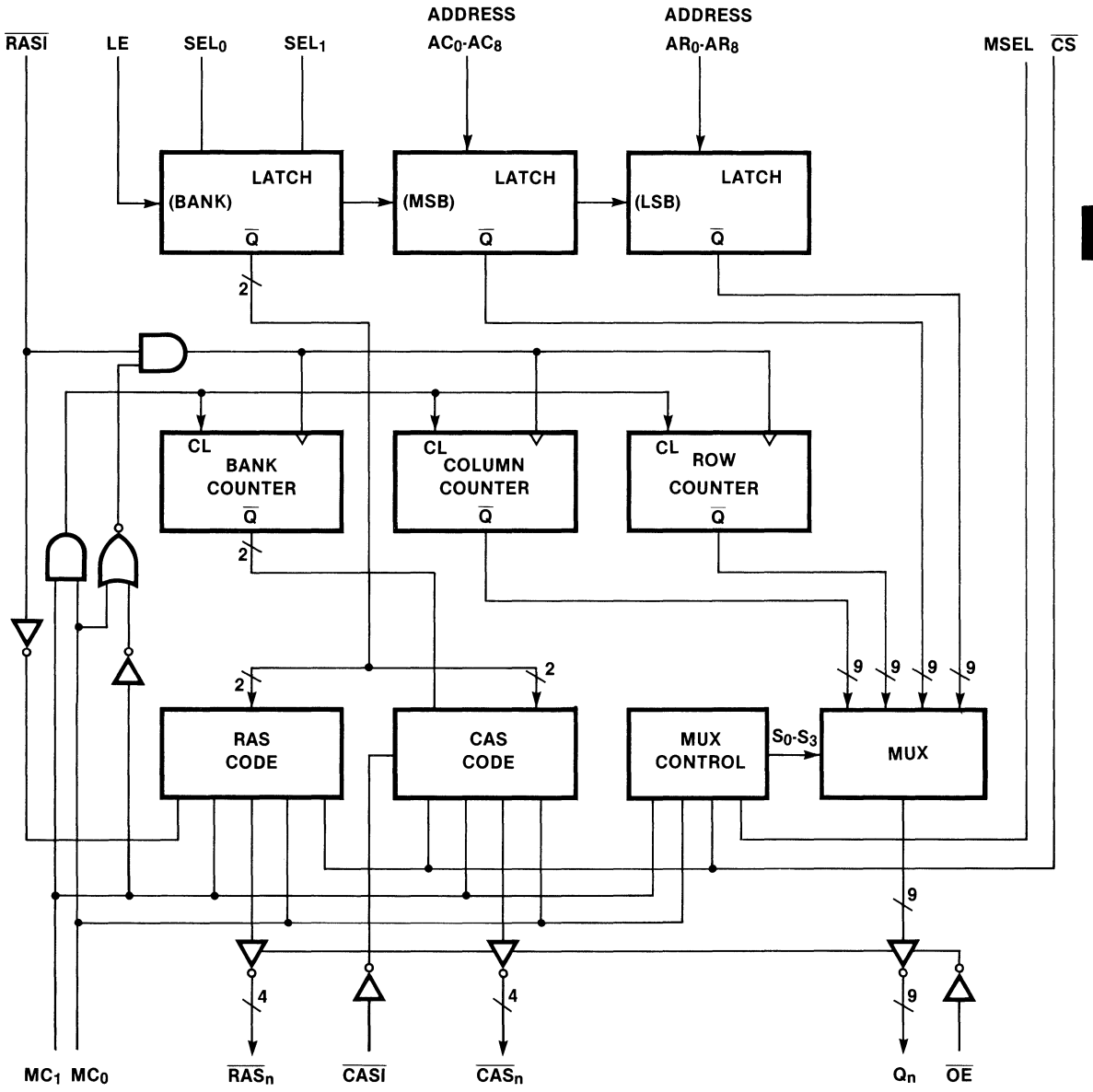
The 29F68 is designed to be used with 16K, 64K or 256K dynamic RAMs. The two 9-bit address latches are used to store row and column addresses provided by the I/O processor while the 2-bit latch is used to select one each of the four RAS and CAS outputs.

In the refresh mode, two counters cycle through the refresh address. Only the row address is used for normal 'RAS-only' refreshing or refresh without scrubbing, generating up to 512 addresses to refresh 512-cycle-refresh dynamic RAM. The column counter is used only for refresh with scrubbing. In this mode all RAS outputs are generated with only one CAS output.

Mode Control Function Table

MC_1	MC_0	Operating Mode
0	0	**Refresh without Scrubbing**—Refresh cycles are performed with only the Row Counter being used to generate addresses. In this mode, all four $\overline{RAS_i}$ outputs are active while the four $\overline{CAS_i}$ signals are kept HIGH.
0	1	**Refresh with Scrubbing/Initialize**—During this mode, refresh cycles are done with both the Row and Column counters generating the addresses. MSEL is used to select between the Row and Column counter. All four $\overline{RAS_i}$ go active in response to RASI, while only one $\overline{CAS_i}$ output goes LOW in response to CASI. The Bank Counter keeps track of which $\overline{CAS_i}$ output will go active. This mode is also used on system power-up so that the memory can be written with a known data pattern.
1	0	**Read/Write**—This mode is used to perform Read/Write cycles. Both the Row and Column addresses are latched and multiplexed to the address output lines using MSEL; SEL_0 and SEL_1 are decoded to determine which $\overline{RAS_i}$ and $\overline{CAS_i}$ will be active.
1	1	**Clear Refresh Counter**—This mode will clear the three refresh counters (Row, Column, and Bank) on the HIGH-to-LOW transition of RASI, putting them at the start of the refresh sequence. In this mode, all four $\overline{RAS_i}$ are driven LOW upon receipt of RASI so that DRAM wake-up cycles may be performed.

Block Diagram



Address Output Function Table

$\overline{CS}$	MC_1	MC_0	MSEL	Mode	MUX Output
0	0	0	X	Refresh without Scrubbing	Row Counter Address
	0	1	1	Refresh with Scrubbing	Column Counter Address
			0		Row Counter Address
	1	0	1	Read/Write	Column Address Latch
			0		Row Address Latch
	1	1	X	Clear Refresh Counter	Zero
1	0	0	X	Refresh without Scrubbing	Row Counter Address
	0	1	1	Refresh with Scrubbing	Column Counter Address
			0		Row Counter Address
	1	0	X	Read/Write	Zero
	1	1	X	Clear Refresh Counter	Zero

$\overline{RAS}$ Output Function Table

RASI	$\overline{CS}$	MC_1	MC_0	SEL_1	SEL_0		Mode	$\overline{RAS_0}$	$\overline{RAS_1}$	$\overline{RAS_2}$
0	X	X	X	X	X		X	1	1	1
1	0	0	0	X	X	Refresh without Scrubbing	0	0	0	0
		0	1	X	X	Refresh with Scrubbing	0	0	0	0
		1	0	0	0	Read/Write		0	1	1
				0	1			1	0	1
				1	0			1	1	0
				1	1			1	1	1
		1	1	X	X	Clear Refresh Counter	0	0	0	0
	1	0	0	X	X	Refresh without Scrubbing	0	0	0	0
		0	1			Refresh with Scrubbing	0	0	0	0
		1	0			Read/Write		1	1	1
		1	1			Clear Refresh Counter	0	0	0	0

$\overline{CAS}$ Output Function Table

CASI	$\overline{CS}$	MC_1	MC_0	$CNTR_1$	$CNTR_0$	SEL_1	SEL_0	$\overline{CAS_0}$	$\overline{CAS_1}$	$\overline{CAS_2}$	$\overline{CAS_3}$
		0	0	X	X	X	X	1	1	1	1
				0	0			0	1	1	1
				0	1			1	0	1	1
		0	1			X	X				
				1	0			1	1	0	1
				1	1			1	1	1	0
	0					0	0	0	1	1	1
		1	0	X	X	0	1	1	0	1	1
						1	0	1	1	0	1
1						1	1	1	1	1	0
		1	1	X	X	X	X	1	1	1	1
		0	0	X	X	X	X	1	1	1	1
				0	0			0	1	1	1
				0	1			1	0	1	1
		0	1			X	X				
	1			1	0			1	1	0	1
				1	1			1	1	1	0
		1	0	X	X	X	X	1	1	1	1
		1	1								
0	X	X	X	X	X	X	X	1	1	1	1

4

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	29F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current				mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	29F	Military 29F	Commercial 29F	Units
		$T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$	T_A, V_{CC} = Mil $C_L = 50\ pF$	T_A, V_{CC} = Com $C_L = 50\ pF$	
		Min Typ Max	Min Max	Min Max	
t_{PLH} t_{PHL}	Propagation Delay A_n to Q_n	11.0 11.0			ns
t_{PLH} t_{PHL}	Propagation Delay RASI to $\overline{RAS}_i$	9.0 9.0			ns
t_{PLH} t_{PHL}	Propagation Delay CASI to $\overline{CAS}_i$	9.0 9.0			ns
t_{PLH} t_{PHL}	Propagation Delay MSEL to Q	9.0 9.0			ns
t_{PLH} t_{PHL}	Propagation Delay MC_i to Q	12.0 12.0			ns
t_{PLH} t_{PHL}	Propagation Delay LE to $\overline{RAS}_i$	12.0 12.0			ns
t_{PLH} t_{PHL}	Propagation Delay LE to $\overline{CAS}_i$	12.0 12.0			ns
t_{PLH} t_{PHL}	Propagation Delay MC_i to $\overline{RAS}_i$	9.0 9.0			ns
t_{PLH} t_{PHL}	Propagation Delay MC_i to $\overline{CAS}_i$	9.0 9.0			ns
t_{PLH} t_{PHL}	Propagation Delay LE to Q_n	11.0 11.0			ns
t_{PHZ} t_{PLZ}	Output Enable Time $\overline{OE}$ to Q_n, $\overline{RAS}_i$ or $\overline{CAS}_i$	5.0 5.0			ns
t_{PZH} t_{PZL}	Output Disable Time $\overline{OE}$ to Q_n, $\overline{RAS}_i$ or $\overline{CAS}_i$	10.0 10.0			ns
$t_w(H)$ $t_w(L)$	$\overline{RAS}_i$ or $\overline{CAS}_i$ Pulse Width HIGH or LOW				ns

AC Characteristics (Cont'd)

Symbol	Parameter	29F	Military 29F	Commercial 29F	Units
		$T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$	T_A, V_{CC} = Mil $C_L = 50\ pF$	T_A, V_{CC} = Com $C_L = 50\ pF$	
		Min Typ Max	Min Max	Min Max	
t_{DHL} t_{DLH}	Skew Q_n to $\overline{RAS}_i$ MC = 10				ns
t_{DHL} t_{DLH}	Skew Q_n to $\overline{RAS}_i$ MC = 00, 01				ns
t_{DHL} t_{DLH}	Skew Q_n to $\overline{RAS}_i$				ns
t_{DHL} t_{DLH}	Skew Q_n to $\overline{CAS}_i$				ns

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	29F	Military 29F	Commercial 29F	Units
		$T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 500\ pF$	T_A, V_{CC} = Mil $C_L = 500\ pF$	T_A, V_{CC} = Com $C_L = 500\ pF$	
		Min Typ Max	Min Max	Min Max	
t_{PLH} t_{PHL}	Propagation Delay A_n to Q_n	14.0 14.0			ns
t_{PLH} t_{PHL}	Propagation Delay RASI to $\overline{RAS}_i$	12.0 12.0			ns
t_{PLH} t_{PHL}	Propagation Delay CASI to $\overline{CAS}_i$	12.0 12.0			ns
t_{PLH} t_{PHL}	Propagation Delay MSEL to Q	12.0 12.0			ns
t_{PLH} t_{PHL}	Propagation Delay MC_i to Q	15.0 15.0			ns
t_{PLH} t_{PHL}	Propagation Delay LE to $\overline{RAS}_i$	15.0 15.0			ns
t_{PLH} t_{PHL}	Propagation Delay LE to $\overline{CAS}_i$	15.0 15.0			ns

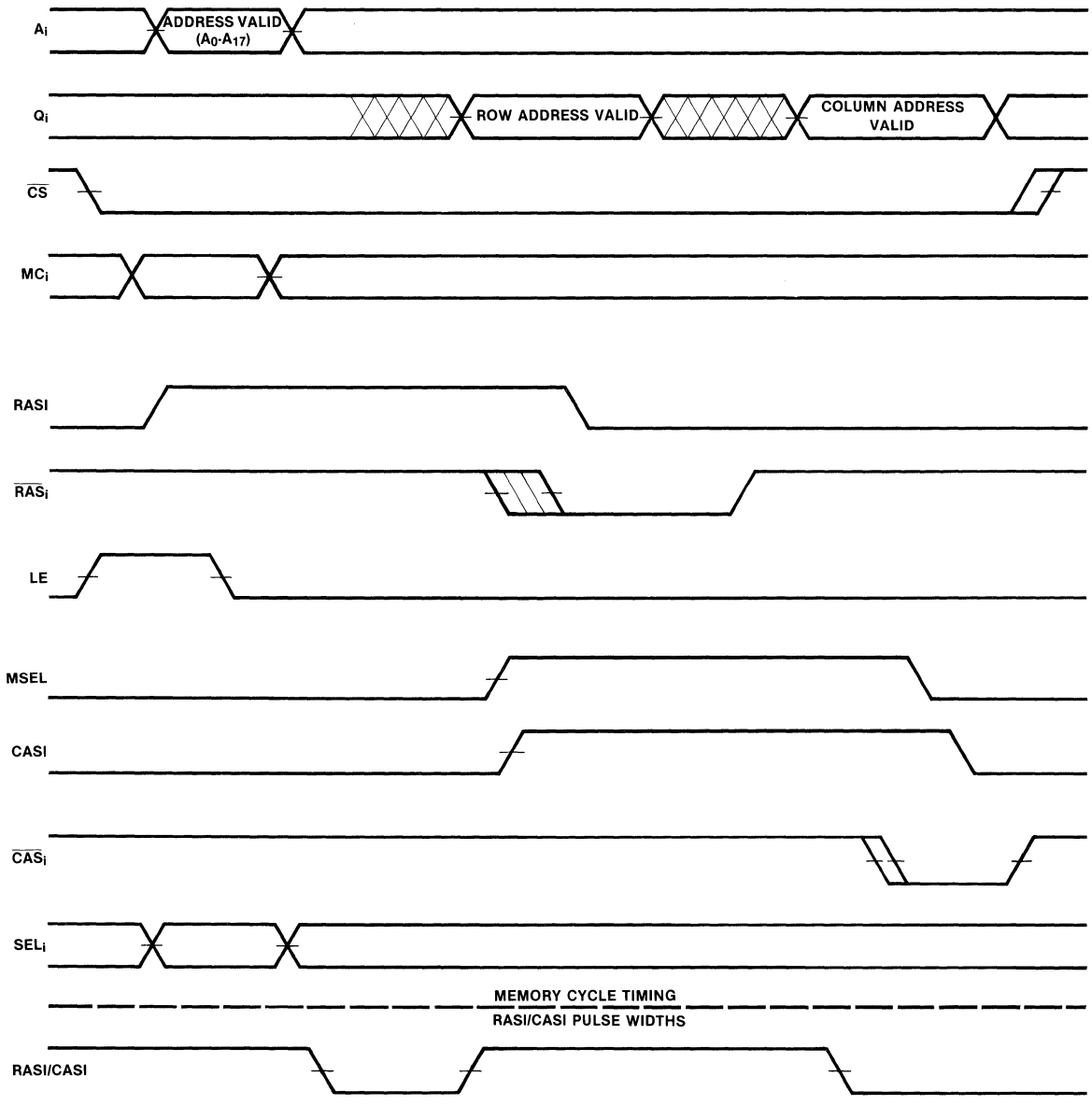
AC Characteristics (Cont'd)

Symbol	Parameter	29F	Military 29F	Commercial 29F	Units
		$T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 500\ pF$	T_A, V_{CC} = Mil $C_L = 500\ pF$	T_A, V_{CC} = Com $C_L = 500\ pF$	
		Min Typ Max	Min Max	Min Max	
t_{PLH} t_{PHL}	Propagation Delay MC_i to $\overline{RAS}_i$	12.0 12.0			ns
t_{PLH} t_{PHL}	Propagation Delay MC_i to $\overline{CAS}_i$	12.0 12.0			ns
t_{PLH} t_{PHL}	Propagation Delay LE to Q_n	14.0 14.0			ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to Q_n, $\overline{RAS}_i$ or $\overline{CAS}_i$				ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Q_n, $\overline{RAS}_i$ or $\overline{CAS}_i$	13.0 13.0			ns
$t_w(H)$ $t_w(L)$	$\overline{RAS}_i$ or $\overline{CAS}_i$ Pulse Width HIGH or LOW				ns
t_{DHL} t_{DLH}	Skew Q_n to $\overline{RAS}_i$ MC = 10				ns
t_{DHL} t_{DLH}	Skew Q_n to $\overline{RAS}_i$ MC = 00, 01				ns
t_{DHL} t_{DLH}	Skew Q_n to $\overline{RAS}_i$				ns
t_{DHL} t_{DLH}	Skew Q_n to $\overline{CAS}_i$				ns

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	29F			Military 29F		Commercial 29F		Units
		$T_A = +25°C$ $V_{CC} = +5.0\,V$			T_A, V_{CC} = Mil		T_A, V_{CC} = Com		
		Min	Typ	Max	Min	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW A_n to LE		5.0 5.0						ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW A_n to LE		5.0 5.0						ns
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW MC_i to $\overline{RAS_i}$		10.0 10.0						ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW MC_i to $\overline{RAS_i}$		10.0 10.0						ns
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW SEL to LE		5.0 5.0						ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW SEL to LE		5.0 5.0						ns
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{CS}$ to MC_i								ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{CS}$ to $\overline{CAS_i}$								ns

Fig. 68-a Dynamic Memory Controller Timing



Memory Cycle Timing

Fig. 68-b Specifications Applicable to Memory Cycle Timing

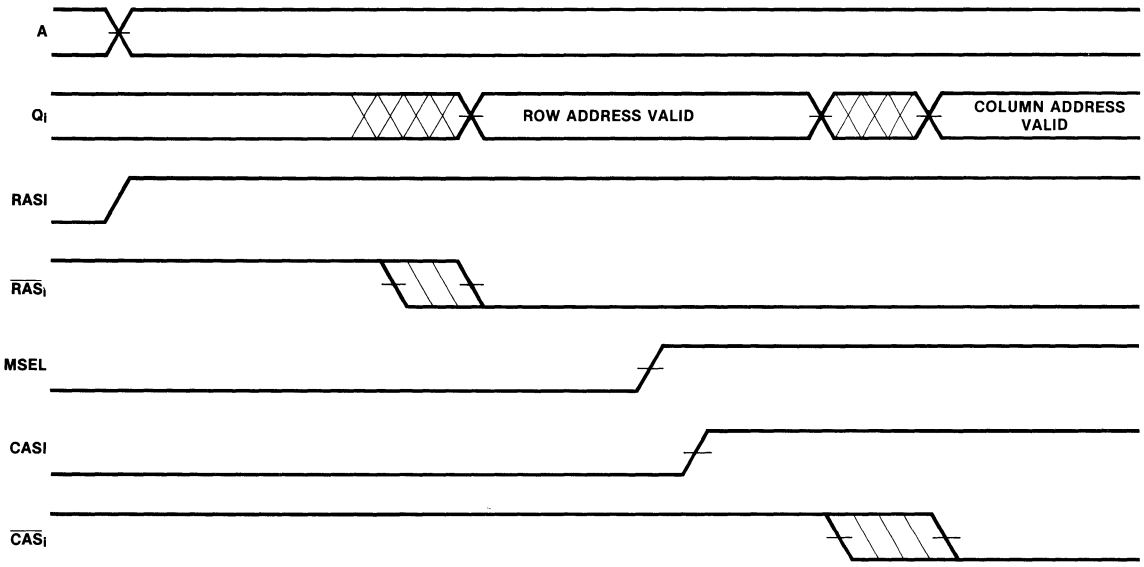
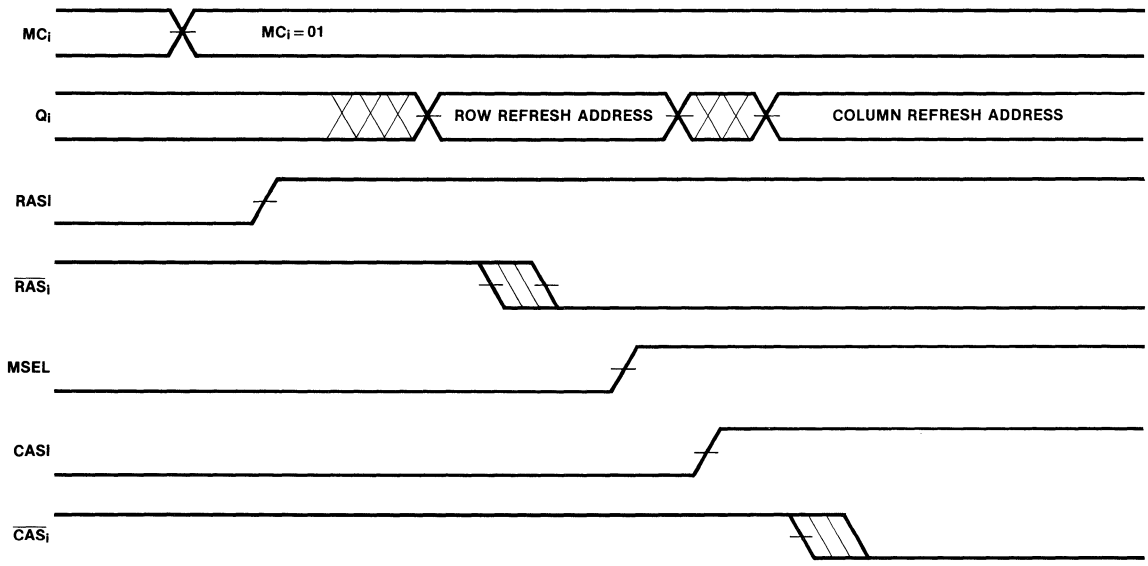


Fig. 68-c Desired System Timing



Refresh Cycle Timing

Fig. 68-d Specifications Applicable to Refresh Cycle Timing

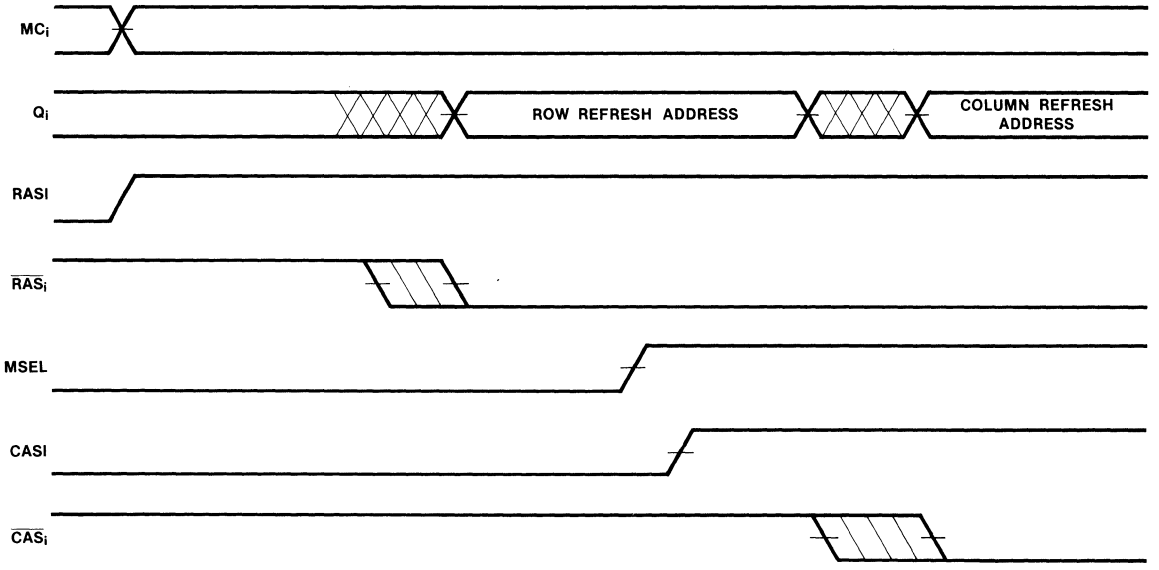


Fig. 68-e Desired Timing: Refresh w/Scrubbing

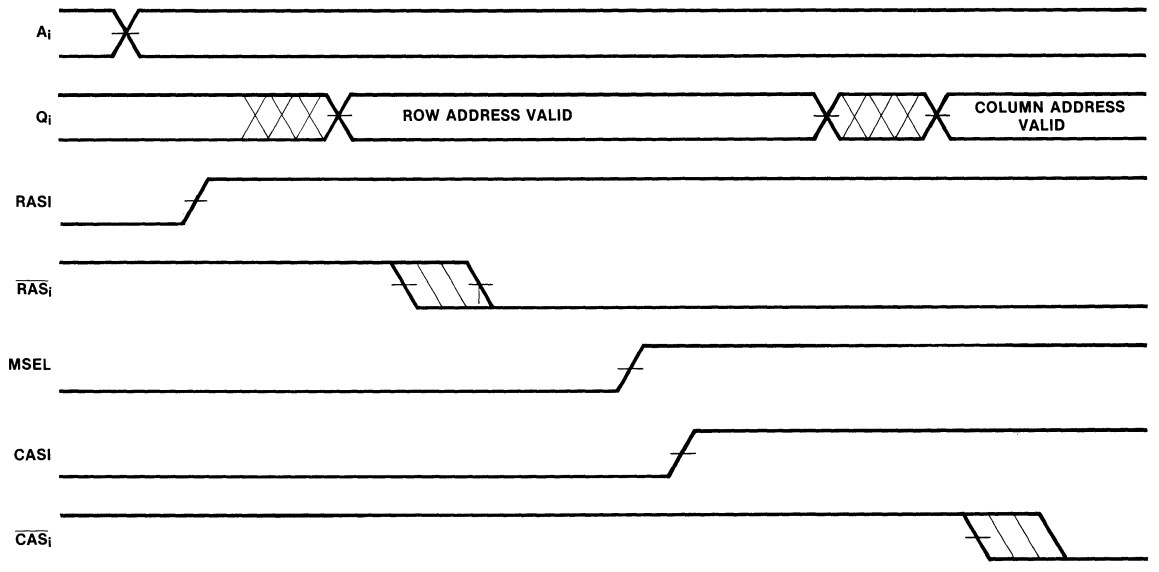
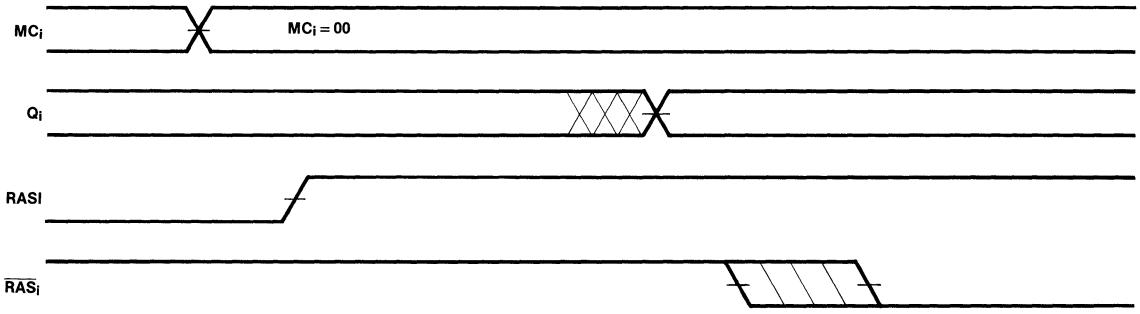
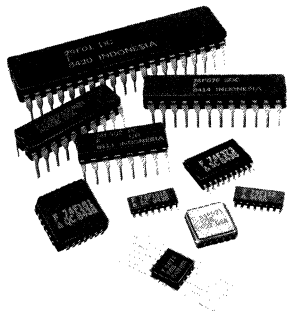


Fig. 68-f Desired Timing: Refresh w/Scrubbing





FAIRCHILD
A Schlumberger Company

Ordering Information/ Package Outlines

The Product Index and Selection Guide in Section 1 lists only the basic device numbers. This basic number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

74F **402** **P** **C** **QR**

Temperature Range Family
74F = Commercial FAST
54F = Military FAST
29F = Commercial or Military FAST

Device Type

Package Code
P = Plastic DIP
SP = Slim Plastic DIP
D = Ceramic DIP
SD = Slim Ceramic DIP
F = Flatpak
L1 = Ceramic Leadless Chip Carrier (LCC)
Q = Plastic Chip Carriers (PCC)
S = Small Outline Package (SOIC)

Temperature Range
C = Commercial
M = Military

Special Variations
QR = Commercial grade device with burn-in
QB = Military grade device with environmental and burn-in processing

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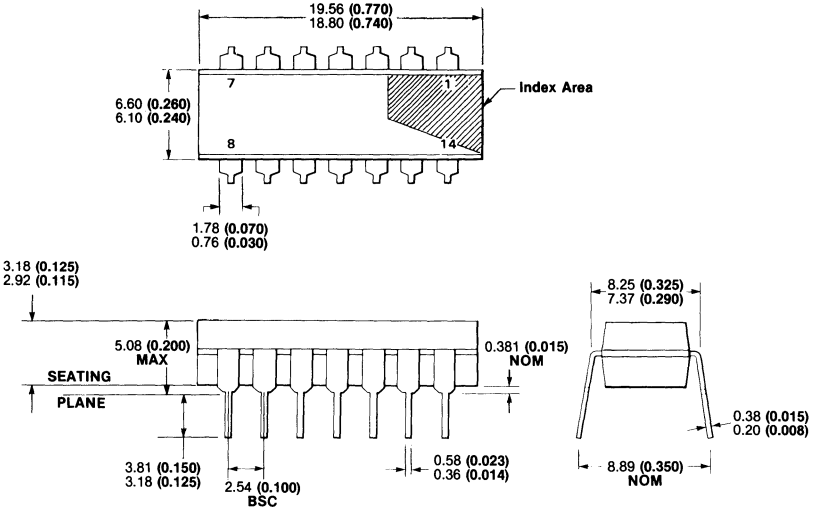
Package	Package Code
Plastic DIP	P
Slim Pastic DIP	SP
Ceramic DIP	D
Slim Ceramic DIP	SD
Flatpak	F
Ceramic Leadless Chip Carrier (LCC)	L1
Plastic Chip Carrier (PCC)	Q
Small Outline, 150 mils (SOIC)	S
Small Outline, 300 mils (SOIC)	V

Temperature Range	Temperature Code
Commercial 0°C to +70°C	C
Military −55°C to +125°C	M

Package Outlines
The package outlines indicated above are shown in the detailed outline drawings in this section.

14 Lead Plastic Dual In-Line

Ordering Code: 74FXXXPC



Notes

Index area: a notch or Lead One identification mark shall be located adjacent to Lead One and shall be located within the shaded area shown.

Leads are intended for insertion in hole rows on 7.620 **(0.300)** centers. They are purposely shipped with positive misalignment to facilitate insertion.

Leads are copper alloy, either tin plated or solder coated.

Package plastic material is novolac epoxy.

Package weight is 0.9 gram.

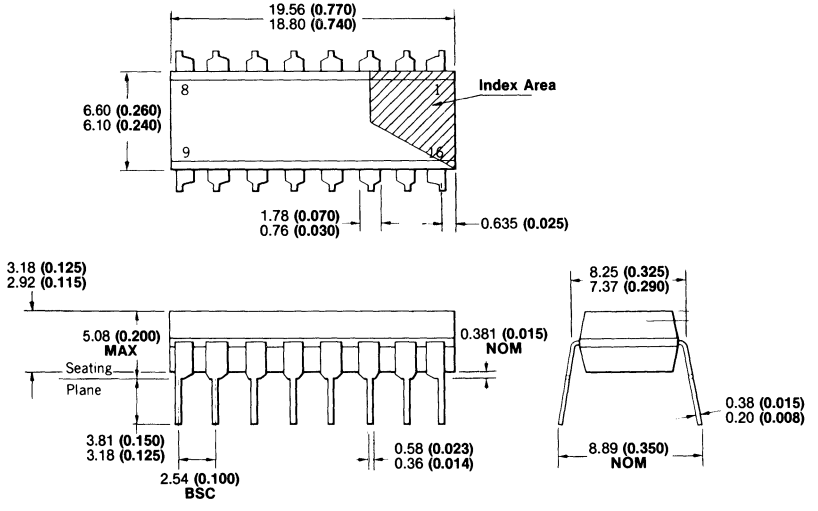
All dimensions are typical unless otherwise specified.

Controlling dimensions are inch dimensions.

Metric dimensions appear first, followed by **inch** dimensions.

16 Lead Plastic Dual In-Line

Ordering Code: 74FXXXPC



Notes

Index area: a notch or Lead One identification mark shall be located adjacent to Lead One and shall be located within the shaded area shown.

Leads are intended for insertion in hole rows on 7.620 **(0.300)** centers. They are purposely shipped with positive misalignment to facilitate insertion.

Leads are copper alloy, either tin plated or solder coated.

Package plastic material is novolac epoxy.

Package weight is 0.9 gram.

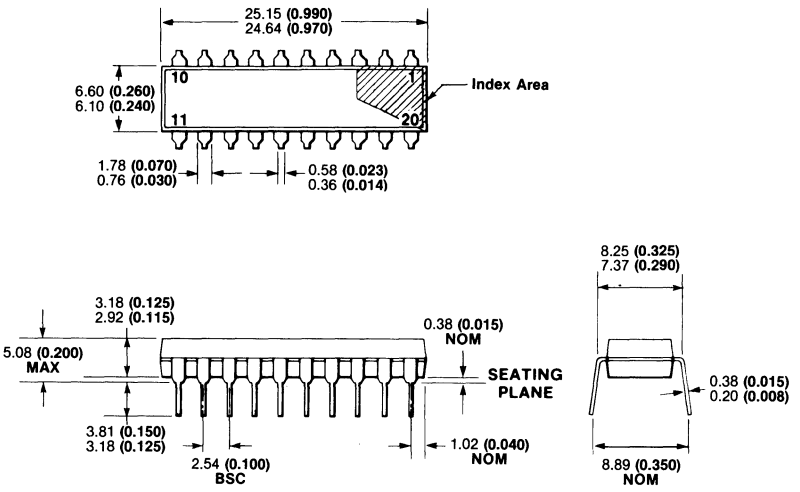
All dimensions are typical unless otherwise specified.

Controlling dimensions are inch dimensions.

Metric dimensions appear first, followed by **inch** dimensions.

20 Lead Plastic Dual In-Line

Ordering Code: 74FXXXPC



Notes

Index area: a notch or Lead One identification mark shall be located adjacent to Lead One and shall be located within the shaded area shown.

Leads are intended for insertion in hole rows on 7.620 **(0.300)** centers. They are purposely shipped with positive misalignment to facilitate insertion.

Leads are copper alloy, either tin plated or solder coated.

Package plastic material is novolac epoxy.

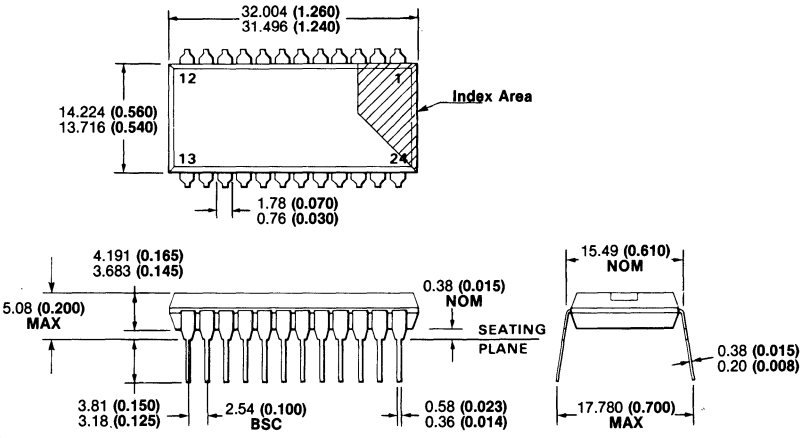
Package weight is 1.2 grams.

Controlling dimensions are inch dimensions.

Metric dimensions appear first, followed by **inch** dimensions.

24 Lead Plastic Dual In-Line

Ordering Code: 74FXXXPC



Notes

Index area: a notch or Lead One identification mark shall be located adjacent to Lead One and shall be located within the shaded area shown.

Leads are intended for insertion in hole rows on 7.620 **(0.300)** centers. They are purposely shipped with positive misalignment to facilitate insertion.

Leads are alloy 42, either tin plated or solder coated.

Package plastic material is novolac epoxy.

Package weight is 4.2 grams.

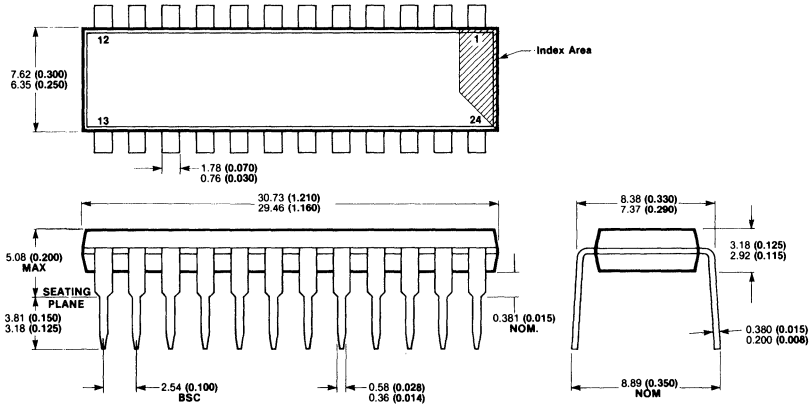
All dimensions are typical unless otherwise specified.

Controlling dimensions are inch dimensions.

Metric dimensions appear first, followed by **inch** dimensions.

24 Lead Slim (0.300" Wide) Plastic Dual In-Line

Ordering Code: 74FXXXSPC



Notes

Index area: a notch or Lead One identification mark shall be located adjacent to Lead One and shall be located within the shaded area shown.

Leads are intended for insertion in hole rows on 7.620 **(0.300)** centers. They are purposely shipped with positive misalignment to facilitate insertion.

Leads are copper alloy, either tin plated or solder coated.

Package plastic material is novolac epoxy.

All dimensions are typical unless otherwise specified.

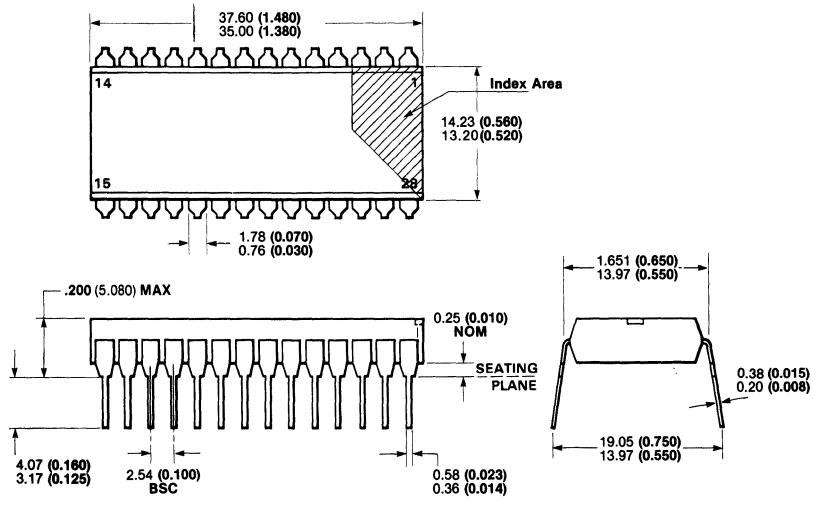
Controlling dimensions are inch dimensions.

ADVANCE INFORMATION

Metric dimensions appear first, followed by **inch** dimensions.

28 Lead Plastic Dual In-Line

Ordering Code: 74FXXXPC



Notes

Index area: a notch or Lead One identification mark shall be located adjacent to Lead One and shall be located within the shaded area shown.

Leads are intended for insertion in hole rows on 15.400 **(0.600)** centers. They are purposely shipped with positive misalignment to facilitate insertion.

Leads are copper alloy, either tin plated or solder coated.

Package plastic material is novolac epoxy.

All dimensions are typical unless otherwise specified.

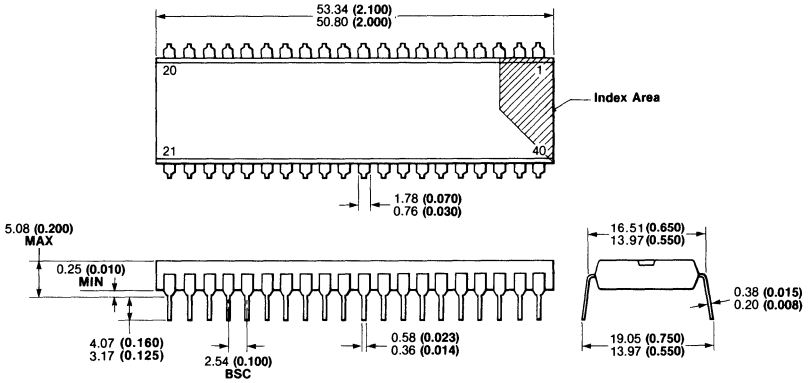
Controlling dimensions are inch dimensions.

ADVANCE INFORMATION

Metric dimensions appear first, followed by **inch** dimensions.

40 Lead Plastic Dual In-Line

Ordering Code: 74FXXXPC



Notes

Index area: a notch or Lead One identification mark shall be located adjacent to Lead One and shall be located within the shaded area shown.

Leads are intended for insertion in hole rows on 15.240 **(0.600)** centers. They are purposely shipped with positive misalignment to facilitate insertion.

Leads are copper alloy, either tin plated or solder coated.

Package plastic material is novolac epoxy.

All dimensions are typical unless otherwise specified.

Controlling dimensions are inch dimensions.

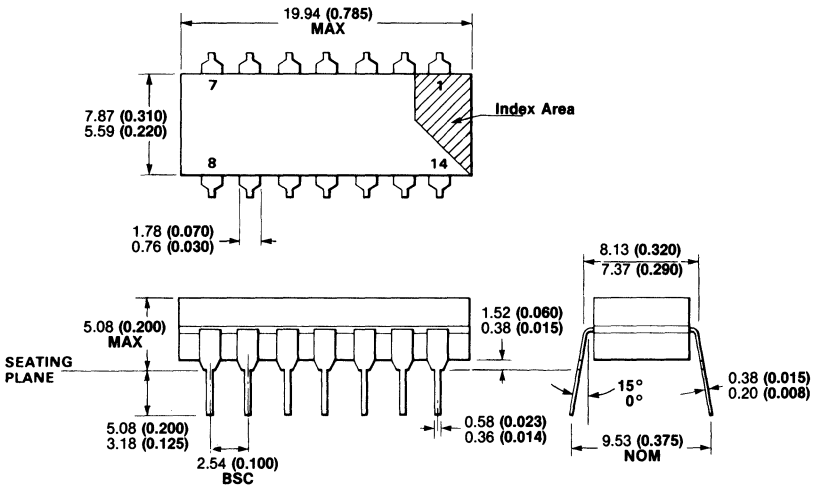
5

ADVANCE INFORMATION

Metric dimensions appear first, followed by **inch** dimensions.

14 Lead Ceramic Dual In-Line

Ordering Codes: 74FXXXDC
54FXXXDM



Notes

Index area: a notch or Lead One identification mark shall be located adjacent to Lead One and shall be located within the shaded area shown.

Leads are intended for insertion in hole rows on 7.620 **(0.300)** centers. They are purposely shipped with positive misalignment to facilitate insertion.

Leads are alloy 42, either tin plated or solder coated.

Package is hermetically sealed alumina (black).

Package weight is 2.0 grams.

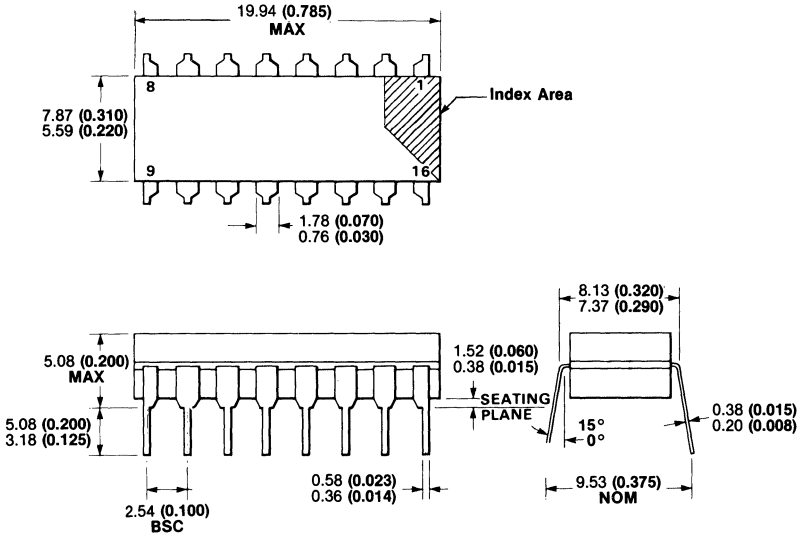
All dimensions are typical unless otherwise specified.

Controlling dimensions are inch dimensions.

Metric dimensions appear first, followed by **inch** dimensions.

16 Lead Ceramic Dual In-Line

Ordering Codes: 74FXXXDC
54FXXXDM



Notes

Index area: a notch or Lead One identification mark shall be located adjacent to Lead One and shall be located within the shaded area shown.

Leads are intended for insertion in hole rows on 7.620 **(0.300)** centers. They are purposely shipped with positive misalignment to facilitate insertion.

Leads are alloy 42, either tin plated or solder coated.

Package is hermetically sealed alumina (black).

Package weight is 2.2 grams.

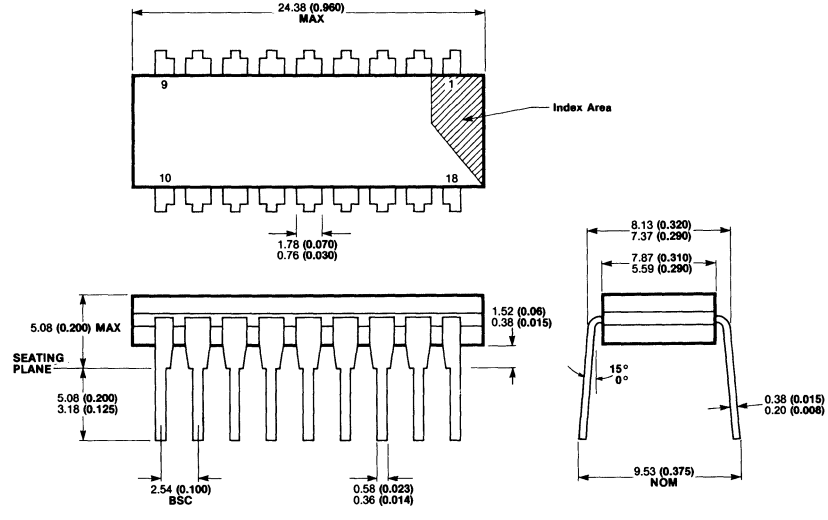
All dimensions are typical unless otherwise specified.

Controlling dimensions are inch dimensions.

Metric dimensions appear first, followed by **inch** dimensions.

18 Lead Ceramic Dual In-Line

Ordering Codes: 74FXXXDC
54FXXXDM



Notes

Index area: a notch or Lead One identification mark shall be located adjacent to Lead One and shall be located within the shaded area shown.

Leads are intended for insertion in hole rows on 7.620 **(0.300)** centers. They are purposely shipped with positive misalignment to facilitate insertion.

Leads are alloy 42, either tin plated or solder coated.

Package is hermetically sealed alumina (black).

Package weight is 2.7 grams.

All dimensions are typical unless otherwise specified.

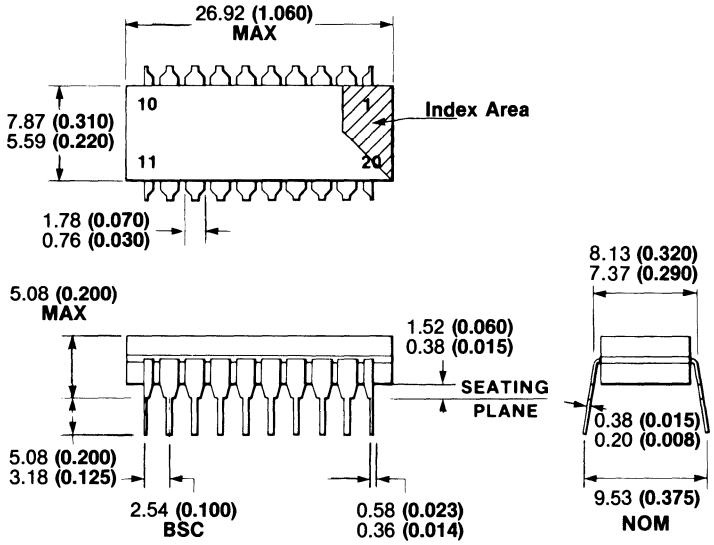
Controlling dimensions are inch dimensions.

ADVANCE INFORMATION

Metric dimensions appear first, followed by **inch** dimensions.

20 Lead Ceramic Dual In-Line

Ordering Codes: 74FXXXDC
54FXXXDM



Notes

Index area: a notch or Lead One identification mark shall be located adjacent to Lead One and shall be located within the shaded area shown.

Leads are intended for insertion in hole rows on 7.620 **(0.300)** centers. They are purposely shipped with positive misalignment to facilitate insertion.

Leads are alloy 42, either tin plated or solder coated.

Package is hermetically sealed alumina (black).

Package weight is 2.4 grams.

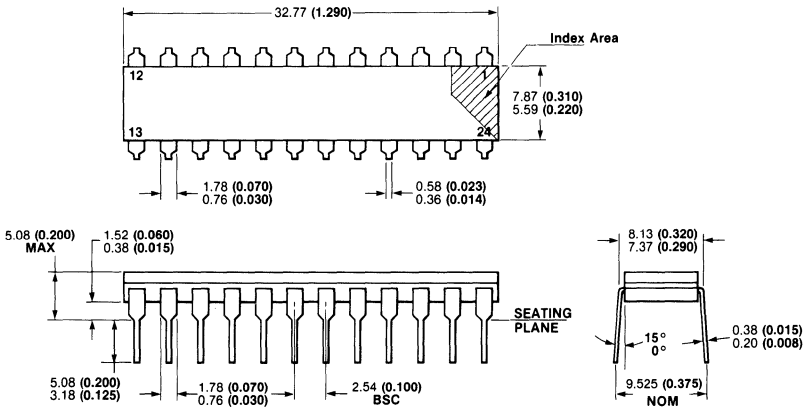
All dimensions are typical unless otherwise specified.

Controlling dimensions are inch dimensions.

Metric dimensions appear first, followed by **inch** dimensions.

24 Lead Slim (0.300" Wide) Ceramic Dual In-Line

Ordering Codes: 74FXXXSDC
54FXXXSDM



Notes

Index area: a notch or Lead One identification mark shall be located adjacent to Lead One and shall be located within the shaded area shown.

Leads are intended for insertion in hole rows on 7.620 **(0.300)** centers. They are purposely shipped with positive misalignment to facilitate insertion.

Leads are alloy 42, either tin plated or solder coated.

Package is hermetically sealed alumina (black).

Package weight is 3.9 grams.

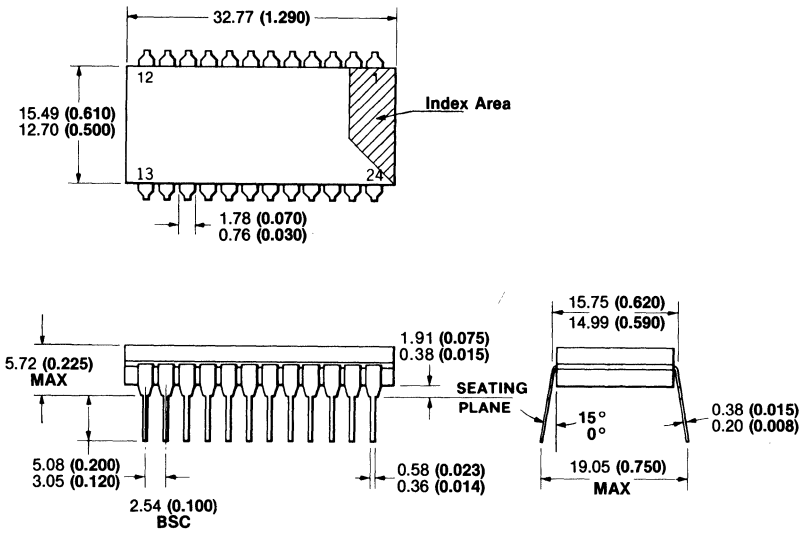
All dimensions are typical unless otherwise specified.

Controlling dimensions are inch dimensions.

Metric dimensions appear first, followed by **inch** dimensions.

24 Lead Ceramic Dual In-Line

Ordering Codes: 74FXXXDC
54FXXXDM



Notes

Index area: a notch or Lead One identification mark shall be located adjacent to Lead One and shall be located within the shaded area shown.

Leads are intended for insertion in hole rows on 15.24 **(0.600)** centers. They are purposely shipped with positive misalignment to facilitate insertion.

Leads are alloy 42, either tin plated or solder coated.

Package is hermetically sealed alumina (black).

Package weight is 6.5 grams.

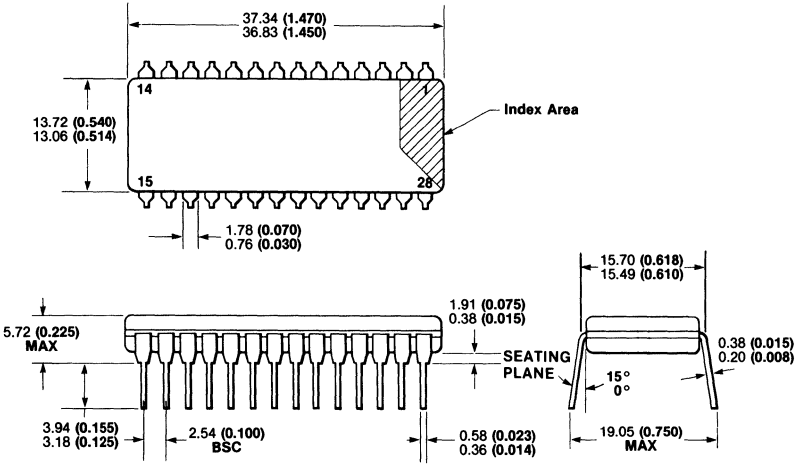
All dimensions are typical unless otherwise specified.

Controlling dimensions are inch dimensions.

Metric dimensions appear first, followed by **inch** dimensions.

28 Lead Ceramic Dual In-Line

Ordering Codes: 74FXXXDC
54FXXXDM



Notes

Index area: a notch or Lead One identification mark shall be located adjacent to Lead One and shall be located within the shaded area shown.

Leads are intended for insertion in hole rows on 15.240 **(0.600)** centers. They are purposely shipped with positive misalignment to facilitate insertion.

Leads are alloy 42, either tin plated or solder coated.

Package is hermetically sealed alumina (black).

Package weight is 7.5 grams.

All dimensions are typical unless otherwise specified.

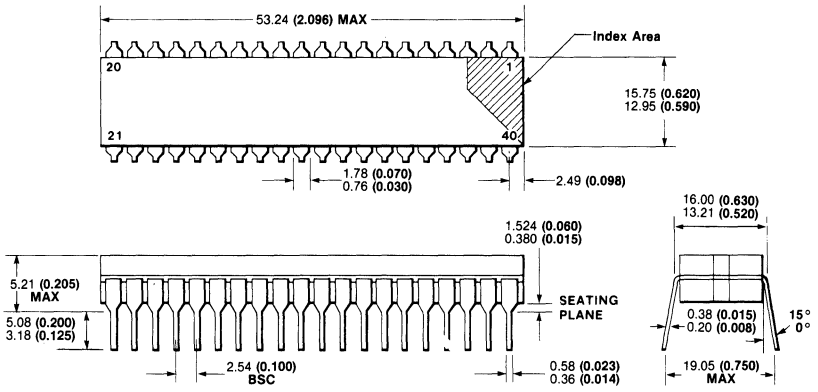
Controlling dimensions are inch dimensions.

Metric dimensions appear first, followed by **inch** dimensions.

ADVANCE INFORMATION

40 Lead Ceramic Dual In-Line

Ordering Codes: 74FXXXDC
54FXXXDM



Notes

Index area: a notch or Lead One identification mark shall be located adjacent to Lead One and shall be located within the shaded area shown.

Leads are intended for insertion in hole rows on 15.240 **(0.600)** centers. They are purposely shipped with positive misalignment to facilitate insertion.

Leads are alloy 42, either tin plated or solder coated.

Package is hermetically sealed alumina (black).

Package weight is 12.0 grams.

All dimensions are typical unless otherwise specified.

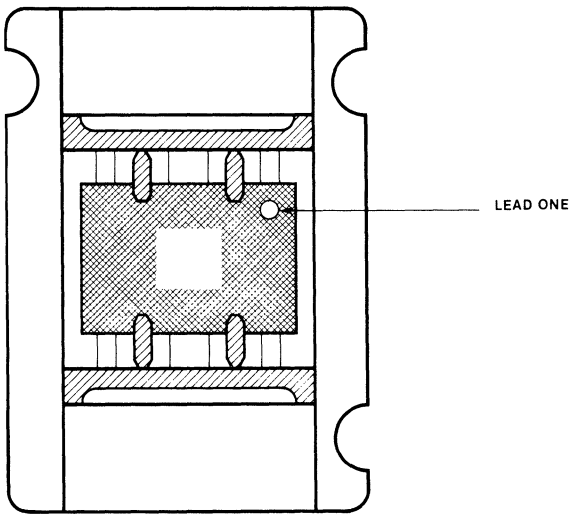
Controlling dimensions are inch dimensions.

Metric dimensions appear first, followed by **inch** dimensions.

5

ADVANCE INFORMATION

Cerpak



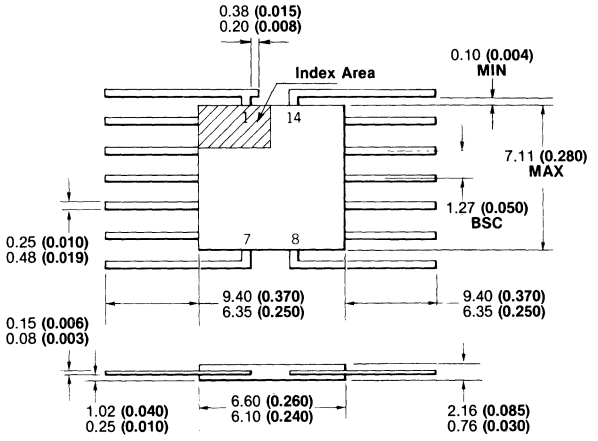
Standard carrier loading locates Lead One of the device adjacent to the side with the double notch, mark side up.

Standard carriers are one-piece designs for 14, 16, 20 and 24 lead Cerpaks.

Carriers are molded of polysulfone, capable of withstanding normal IC handling over the temperature range of −55°C to +150°C.

14 Lead Ceramic Flatpak

Ordering Code: 54FXXXFM



Notes

Index area: a notch or Lead One identification mark shall be located adjacent to Lead One and shall be located within the shaded area shown. Alternatively, a tab on the lead frame may be used to identify Lead One.

Leads are alloy 42, tin plated and/or solder coated.

Package is hermetically sealed alumina (black).

Package weight is 0.26 gram.

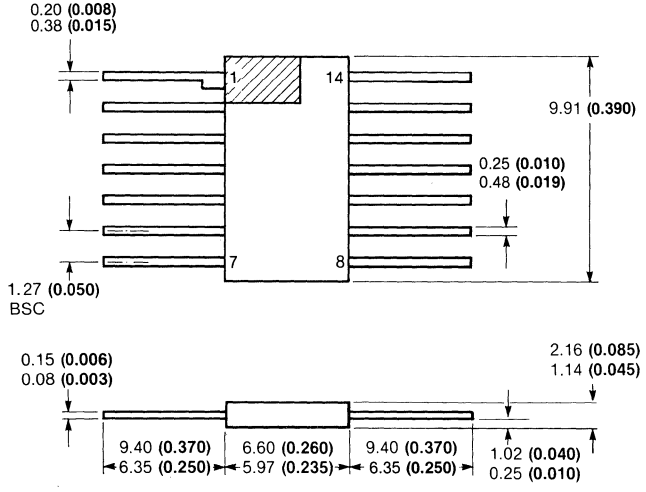
All dimensions are typical unless otherwise specified.

Controlling dimensions are inch dimensions.

Metric dimensions appear first, followed by **inch** dimensions.

14 Lead Ceramic Flatpak

Ordering Codes: 54FXXXFM



ADVANCE INFORMATION

Notes

Index area: a notch or Lead One identification mark shall be located adjacent to Lead One and shall be located within the shaded area shown. Alternatively, a tab on the lead frame may be used to identify Lead One.

Leads are alloy 42, tin plated and/or solder coated.

Package is hermetically sealed alumina (black).

Package weight is 0.4 grams.

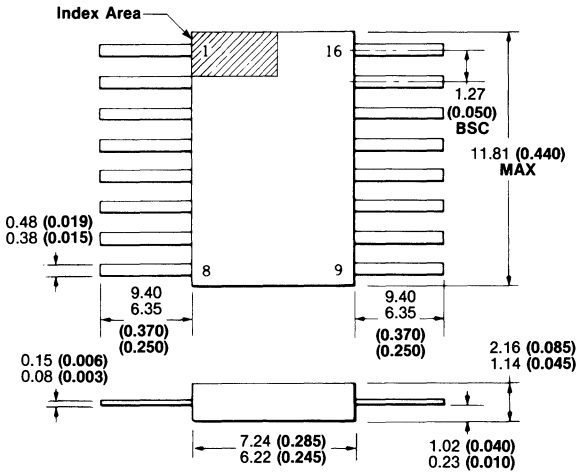
All dimensions are typical unless otherwise specified.

Controlling dimensions are inch dimensions.

Metric dimensions appear first, followed by **inch** dimensions.

16 Lead Ceramic Flatpak

Ordering Code: 54FXXXFM



Notes

Index area: a notch or Lead One identification mark shall be located adjacent to Lead One and shall be located within the shaded area shown. Alternatively, a tab on the lead frame may be used to identify Lead One.

Leads are alloy 42, either tin plated and/or solder coated.

Package is hermetically sealed alumina (black).

Package weight is 0.4 gram.

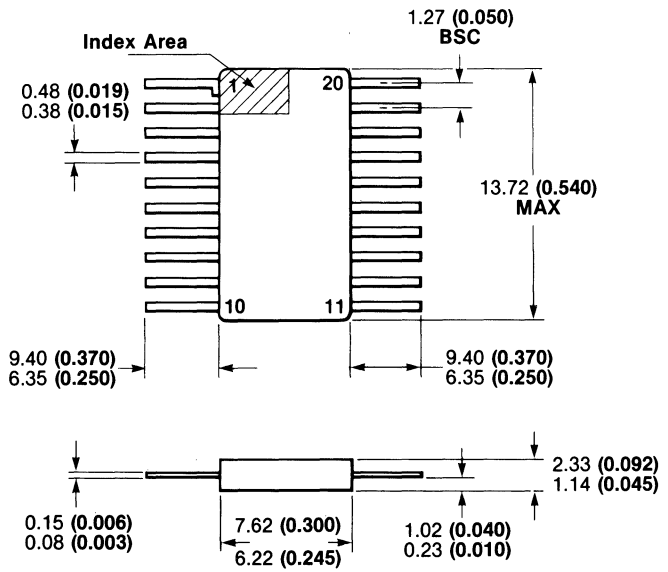
All dimensions are typical unless otherwise specified.

Controlling dimensions are inch dimensions.

Metric dimensions appear first, followed by **inch** dimensions.

20 Lead Ceramic Flatpak

Ordering Code: 54FXXXFM



Notes

Index area: a notch or Lead One identification mark shall be located adjacent to Lead One and shall be located within the shaded area shown. Alternatively, a tab on the lead frame may be used to identify Lead One.

Leads are alloy 42, tin plated and/or solder coated.

Package is hermetically sealed alumina (black).

Package weight is 0.8 gram.

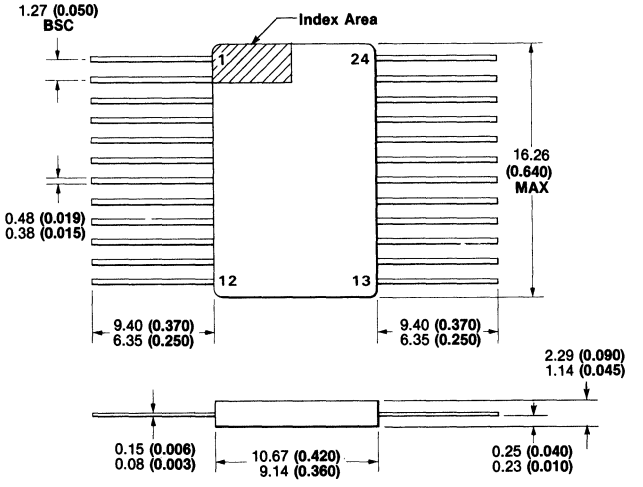
All dimensions are typical unless otherwise specified.

Controlling dimensions are inch dimensions.

Metric dimensions appear first, followed by **inch** dimensions.

24 Lead Ceramic Flatpak

Ordering Code: 54FXXXFM



Notes

Index area: a notch or Lead One identification mark shall be located adjacent to Lead One and shall be located within the shaded area shown. Alternatively, a tab on the lead frame may be used to identify Lead One.

Leads are alloy 42, either tin plated and/or solder coated.

Package is hermetically sealed alumina (black).

Package weight is 0.8 gram.

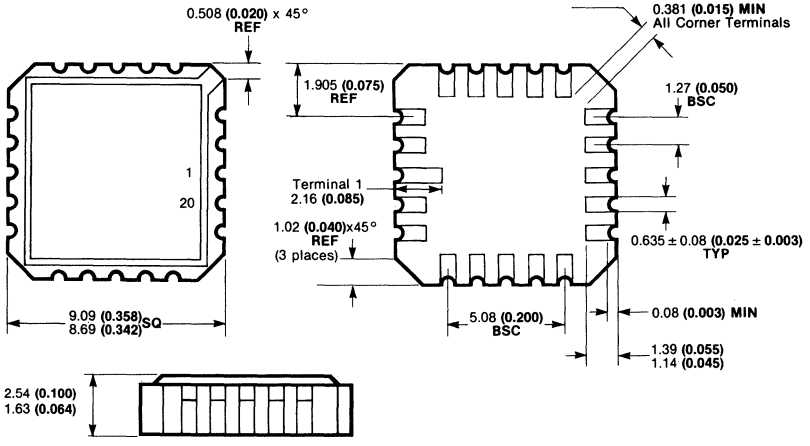
All dimensions are typical unless otherwise specified.

Controlling dimensions are inch dimensions.

Metric dimensions appear first, followed by **inch** dimensions.

20 Terminal Ceramic Leadless Chip Carrier

Ordering Codes: 74FXXXL1C
54FXXXL1M



Notes

Package construction is multilayer refractory metal (gold plated) and alumina (black).

Package is hermetic—solder seal metal lid.

Package weight is 0.5 gram.

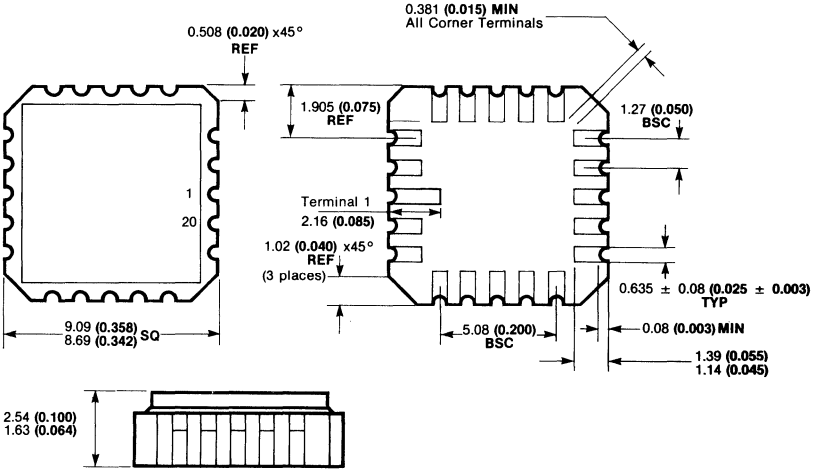
All dimensions are typical unless otherwise specified.

Controlling dimensions are inch dimensions.

Metric dimensions appear first, followed by **inch** dimensions.

20 Terminal Ceramic Leadless Chip Carrier

Ordering Codes: 74FXXXL1C
54FXXXL1M



Notes

Package construction is multilayer refractory metal (gold plated) and alumina (black).

Package is hermetic—glass seal alumina lid (black).

Package weight is 0.5 gram.

All dimensions are typical unless otherwise specified.

Controlling dimensions are inch dimensions.

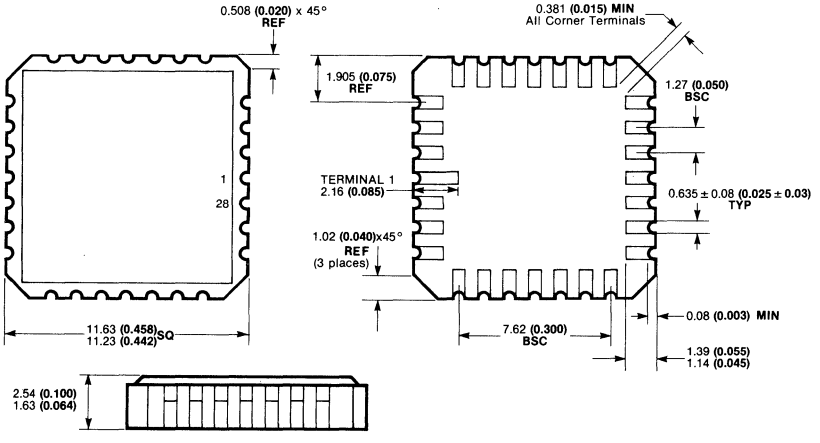
5

ADVANCE INFORMATION

Metric dimensions appear first, followed by **inch** dimensions.

28 Terminal Ceramic Leadless Chip Carrier

Ordering Codes: 74FXXXL1C
54FXXXL1M



Notes

Package construction is multilayer refractory metal (gold plated) and alumina (black).

Package is hermetic—solder seal metal lid.

Package weight is 0.8 gram.

All dimensions are typical unless otherwise specified.

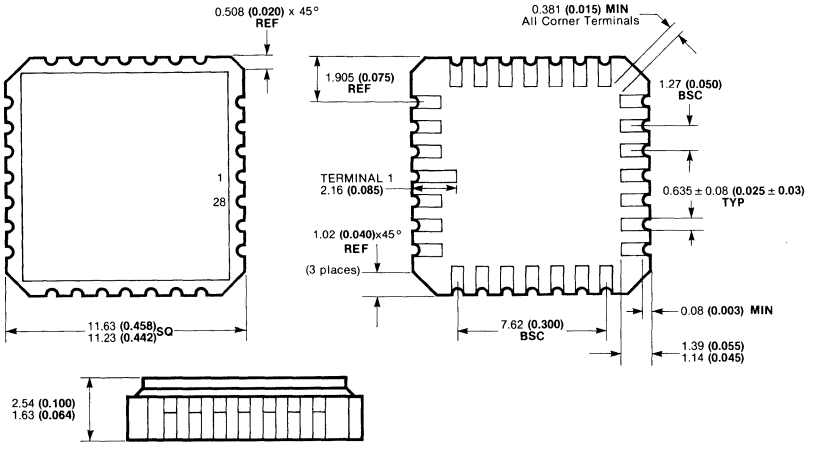
Controlling dimensions are inch dimensions.

ADVANCE INFORMATION

Metric dimensions appear first, followed by **inch** dimensions.

28 Terminal Ceramic Leadless Chip Carrier

Ordering Codes: 74FXXXL1C
54FXXXL1M



Notes

Package construction is multilayer refractory metal (gold plated) and alumina (black).

Package is hermetic—glass seal alumina lid (black).

Package weight is 0.9 gram.

All dimensions are typical unless otherwise specified.

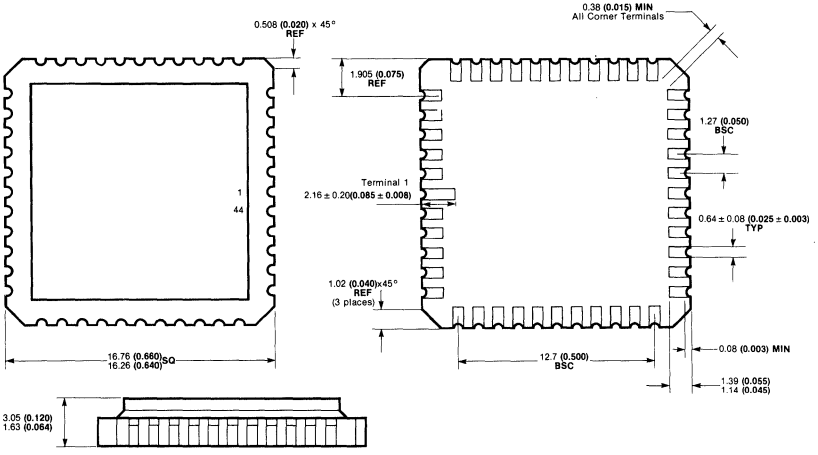
Controlling dimensions are inch dimensions.

ADVANCE INFORMATION

Metric dimensions appear first, followed by **inch** dimensions.

44 Terminal Ceramic Leadless Chip Carrier

Ordering Codes: 74FXXXL1C
54FXXXL1M



Notes

Package construction is multilayer refractory metal (gold plated) and alumina (black).

Package is hermetic—glass seal alumina lid (black).

Package weight is 1.7 grams.

All dimensions are typical unless otherwise specified.

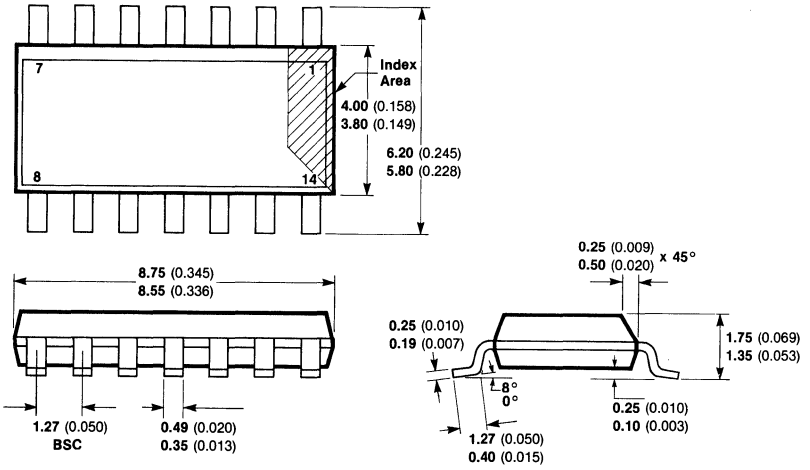
Controlling dimensions are inch dimensions.

ADVANCE INFORMATION

Metric dimensions appear first, followed by **inch** dimensions.

14 Lead Small Outline Integrated Circuit (SOIC)

Ordering Code: 74FXXXS



Notes

Index area: a notch or Lead One identification mark shall be located adjacent to Lead One and shall be located within the shaded area shown.

Leads are copper alloy, either tin plated or solder coated.

Package plastic material is novolac epoxy.

Package weight is 0.14 grams.

Total flash not to exceed **0.15** (0.006) over body dimensions.

Conforms to variation AB of JEDEC Standard Outline MS-012 for **3.75** (0.150) wide body small outline (SO) family.

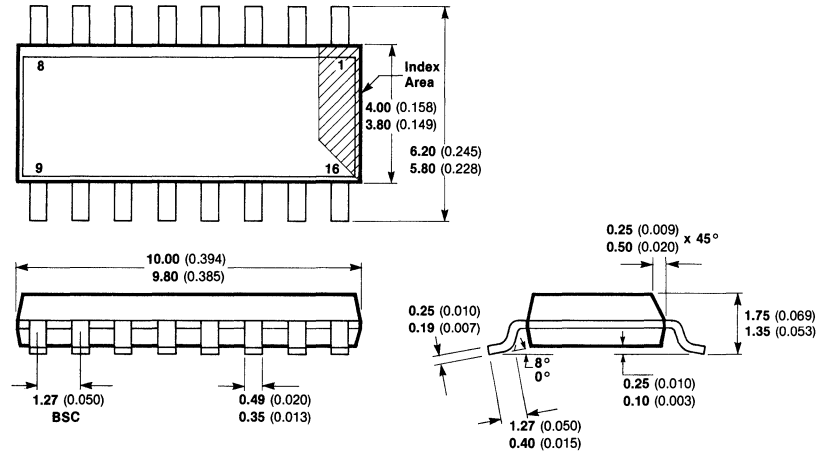
All dimensions are typical unless otherwise specified.

Controlling dimensions are metric dimensions.

Metric dimensions appear first, followed by inch dimensions.

16 Lead Small Outline Integrated Circuit (SOIC)

Ordering Code: 74FXXXS



Notes

Index area: a notch or Lead One identification mark shall be located adjacent to Lead One and shall be located within the shaded area shown.

Leads are copper alloy, either tin plated or solder coated.

Package plastic material is novolac epoxy.

Package weight is 0.16 grams.

Total flash not to exceed **0.15** (0.006) over body dimensions.

Conforms to variation AC of JEDEC Standard Outline MS-012 for **3.75** (0.150) wide body small outline (SO) family.

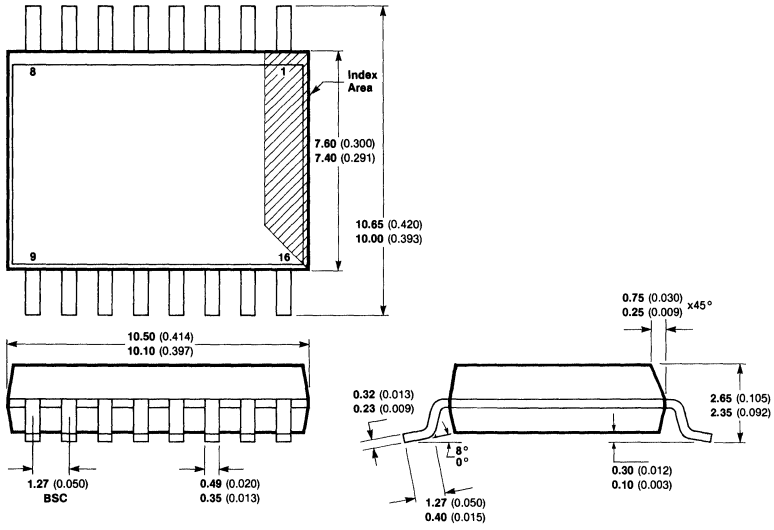
All dimensions are typical unless otherwise specified.

Controlling dimensions are metric dimensions.

Metric dimensions appear first, followed by inch dimensions.

16 Lead (0.300" Wide) Small Outline Integrated Circuit (SOIC)

Ordering Code: 74FXXXV



Notes

Index area: a notch or Lead One identification mark shall be located adjacent to Lead One and shall be located within the shaded area shown.

Leads are copper alloy, either tin plated or solder coated.

Package plastic material is novolac epoxy.

Package weight is 0.46 grams.

Total flash not to exceed **0.15** (0.006) over body dimensions.

Conforms to variation AA of JEDEC Standard Outline MS-013 for **7.50** (0.300) wide body small outline (SO) family.

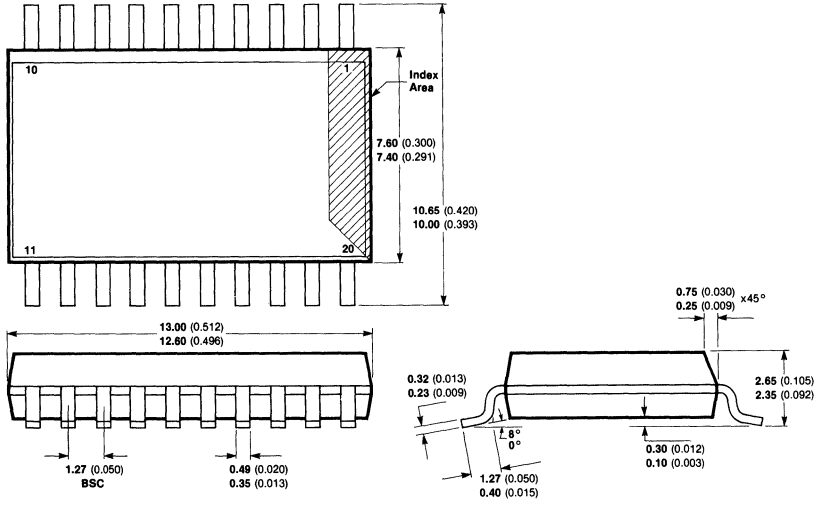
All dimensions are typical unless otherwise specified.

Controlling dimensions are metric dimensions.

Metric dimensions appear first, followed by inch dimensions.

20 Lead Small Outline Integrated Circuit (SOIC)

Ordering Code: 74FXXXV



Notes

Index area: a notch or Lead One identification mark shall be located adjacent to Lead One and shall be located within the shaded area shown.

Leads are copper alloy, either tin plated or solder coated.

Package plastic material is novolac epoxy.

Package weight is 0.55 grams.

Total flash not to exceed **0.15** (0.006) over body dimensions.

Conforms to variation AC of JEDEC Registered Outline MS-013 for **7.50** (0.300) wide body small outline (SO) family.

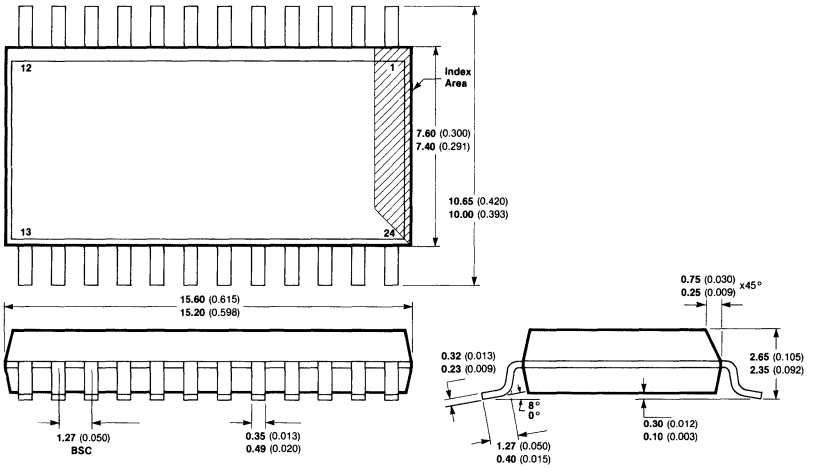
All dimensions are typical unless otherwise specified.

Controlling dimensions are metric dimensions.

Metric dimensions appear first, followed by inch dimensions.

24 Lead Small Outline Integrated Circuit (SOIC)

Ordering Code: 74FXXXV



Notes

Index area: a notch or Lead One identification mark shall be located adjacent to Lead One and shall be located within the shaded area shown.

Leads are copper alloy, either tin plated or solder coated.

Package plastic material is novolac epoxy.

Package weight is 0.66 grams.

Total flash not to exceed **0.15** (0.006) over body dimensions.

Conforms to variation AD of JEDEC Standard Outline MS-013 for **7.50** (0.300) wide body small outline (SO) family.

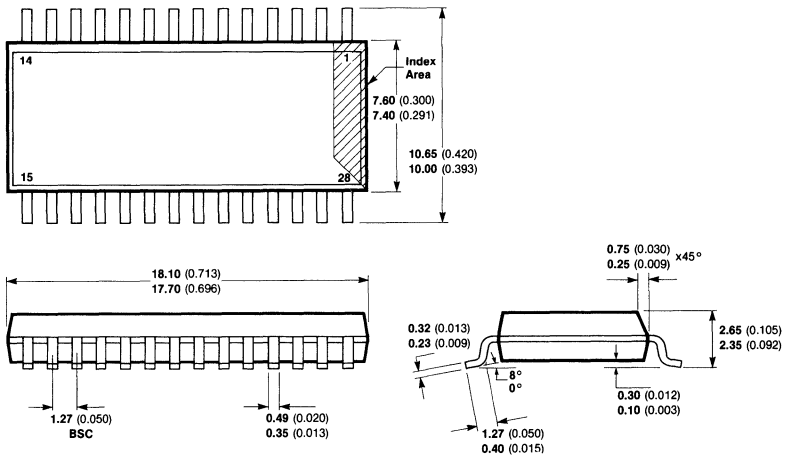
All dimensions are typical unless otherwise specified.

Controlling dimensions are metric dimensions.

Metric dimensions appear first, followed by inch dimensions.

28 Lead Small Outline Integrated Circuit (SOIC)

Ordering Code: 74FXXXV



Notes

Index area: a notch or Lead One identification mark shall be located adjacent to Lead One and shall be located within the shaded area shown.

Leads are copper alloy, either tin plated or solder coated.

Package plastic material is novolac epoxy.

Package weight is 0.77 grams.

Total flash not to exceed **0.15** (0.006) over body dimensions.

Conforms to variation AE of JEDEC Standard Outline MS-013 for **7.50** (0.300) wide body small outline (SO) family.

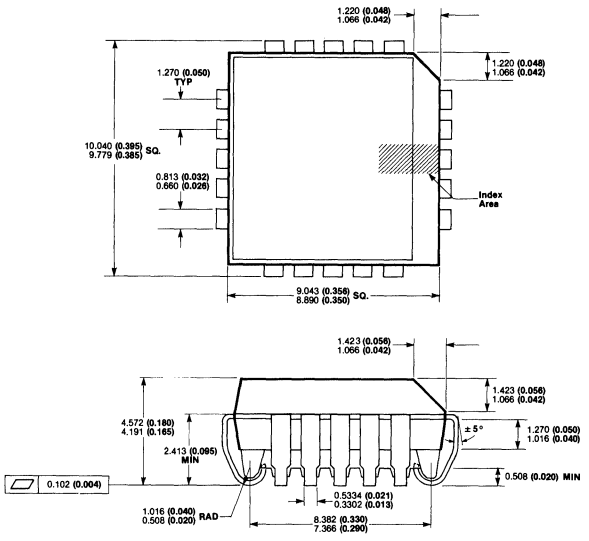
All dimensions are typical unless otherwise specified.

Controlling dimensions are metric dimensions.

Metric dimensions appear first, followed by inch dimensions.

20 Lead Plastic Chip Carrier (PCC)

Ordering Code: 74FXXXQC



ADVANCE INFORMATION

Notes

Index area: a notch or Lead One identification mark shall be located adjacent to Lead One and shall be located within the shaded area shown.

Leads are copper alloy, either tin plated or solder coated.

Package plastic material is novolac epoxy.

Total flash not to exceed 0.016 **(0.006)** over body dimensions.

Conforms to variation AA of JEDEC Registered Outline MO-047 for Plastic Chip Carrier package.

All dimensions are typical unless otherwise specified.

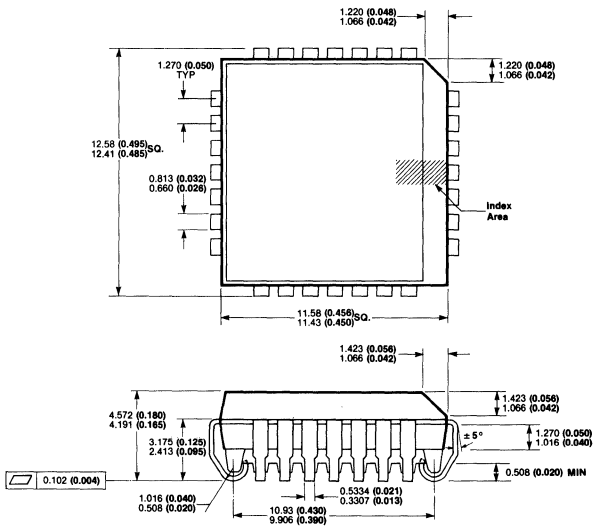
Controlling dimensions are inch dimensions.

This package is also referred to as a Plastic Leaded Chip Carrier (PLCC) or Plastic Quadpak.

Metric dimensions appear first, followed by **inch** dimensions.

28 Lead Plastic Chip Carrier (PCC)

Ordering Code: 74FXXXQC



ADVANCE INFORMATION

Notes

Index area: a notch or Lead One identification mark shall be located adjacent to Lead One and shall be located within the shaded area shown.

Leads are copper alloy, either tin plated or solder coated.

Package plastic material is novolac epoxy.

Total flash not to exceed 0.016 **(0.006)** over body dimensions.

Conforms to variation AB of JEDEC Registered Outline MO-047 for Plastic Chip Carrier package.

All dimensions are typical unless otherwise specified.

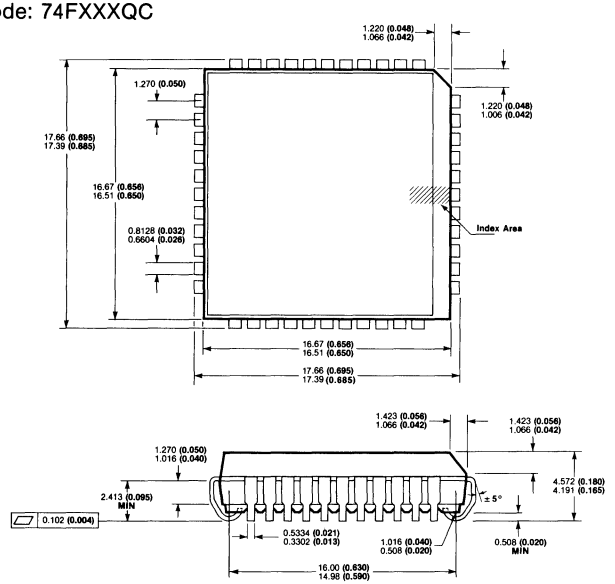
Controlling dimensions are inch dimensions.

This package is also referred to as a Plastic Leaded Chip Carrier (PLCC) or Plastic Quadpak.

Metric dimensions appear first, followed by **inch** dimensions.

44 Lead Plastic Chip Carrier (PCC)

Ordering Code: 74FXXXQC



ADVANCE INFORMATION

Notes

Index area: a notch or Lead One identification mark shall be located adjacent to Lead One and shall be located within the shaded area shown.

Leads are copper alloy, either tin plated or solder coated.

Package plastic material is novolac epoxy.

Total flash not to exceed 0.16 **(0.006)** over body dimensions.

Conforms to variation AC of JEDEC Registered Outline MO-047 for Plastic Chip Carrier package.

All dimensions are typical unless otherwise specified.

Controlling dimensions are inch dimensions.

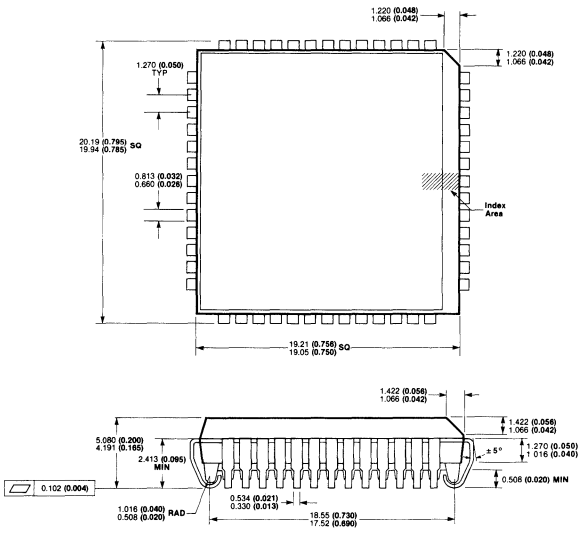
This package is also referred to as a Plastic Leaded Chip Carrier (PLCC) or Plastic Quadpak.

Metric dimensions appear first, followed by **inch** dimensions.

5

52 Lead Plastic Chip Carrier (PCC)

Ordering Code: 74FXXXQC



ADVANCE INFORMATION

Notes

Index area: a notch or Lead One identification mark shall be located adjacent to Lead One and shall be located within the shaded area shown.

Leads are copper alloy, either tin plated or solder coated.

Package plastic material is novolac epoxy.

Total flash not to exceed 0.16 **(0.006)** over body dimensions.

Conforms to variation AD of JEDEC Registered Outline MO-047 for Plastic Chip Carrier package.

All dimensions are typical unless otherwise specified.

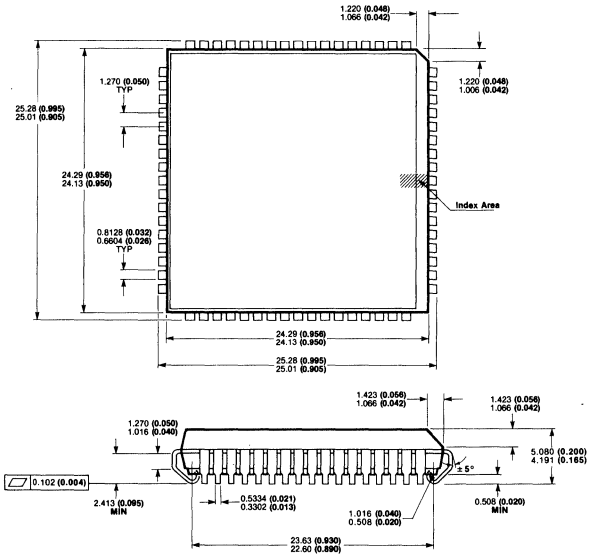
Controlling dimensions are inch dimensions.

This package is also referred to as a Plastic Leaded Chip Carrier (PLCC) or Plastic Quadpak.

Metric dimensions appear first, followed by **inch** dimensions.

68 Lead Plastic Chip Carrier (PCC)

Ordering Code: 74FXXXQC



ADVANCE INFORMATION

Notes

Index area: a notch or Lead One identification mark shall be located adjacent to Lead One and shall be located within the shaded area shown.

Leads are copper alloy, either tin plated or solder coated.

Package plastic material is novolac epoxy.

Total flash not to exceed 0.016 **(0.006)** over body dimensions.

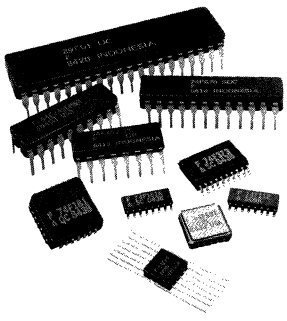
Conforms to variation AE of JEDEC Registered Outline MO-047 for Plastic Chip Carrier package.

All dimensions are typical unless otherwise specified.

Controlling dimensions are inch dimensions.

This package is also referred to as a Plastic Leaded Chip Carrier (PLCC) or Plastic Quadpak.

Metric dimensions appear first, followed by **inch** dimensions.



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Utah
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801-266-0773

Washington
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Canada
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Dollard des Ormeaux, Quebec H9B 2T6
Canada
Tel: 514-683-0883

Ottawa Office
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Canada
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Toronto Office
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Canada
Tel: 416-665-5903

Fairchild Semiconductor Sales Offices International

Australia
Fairchild Australia Pty Ltd.
366 White Horse Road
Nunawading 3131, Victoria
Australia
Tel: 03-877-5444

Austria and Eastern Europe
Fairchild Semiconductor GmbH
Assmayergasse 60
A-1120 Wien
Austria
Tel: (0222) 85.86.82

Benelux
Fairchild Semiconductor
Ruysdaelbaan 35
NL-5613 DX Eindhoven
The Netherlands
Tel: (040) 44.69.09

Brazil
Fairchild Semicondutores Ltda.
Rua Estacio De Sa, 1144
Jardim Santa Genebra
13100 Campinas, SP
Brazil
Tel: (0192) 41-6655

France
Fairchild Semiconductor S.A.
B.P. No. 655
92542 Montrouge Cedex
France
Tel: (1) 746.61.61

Germany
Fairchild Semiconductor GmbH
Daimlerstrasse 15
D-8046 Garching b. Muenchen
West Germany
Tel: (089) 32.00.31

Fairchild Semiconductor GmbH
Flughafen Frachtz. Geb. 458
D-6000 Frankfurt am Main 75
West Germany
Tel: (069) 690.56.13

Fairchild Semiconductor GmbH
Oeltzenstrasse 14
D-3000 Hannover
West Germany
Tel: (0511) 178.44

Fairchild Semiconductor GmbH
Poststrasse 37
D-7250 Leonberg
West Germany
Tel: (07152) 410.26

Hong Kong
Fairchild Semiconductor (HK) Ltd.
12th Floor, Austin Tower
22-26A Austin Avenue
Tsimshatsui, Kowloon
Hong Kong
Tel: 3-7238321

Italy
Fairchild Semiconductor, S.p.A.
Viale Corsica 7
20133 Milano
Italy
Tel: (02) 749.12.71

Fairchild Semiconductor, S.p.A.
Via Francesco Saverio Nitti 11
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Tel: (06) 328.75.48

Japan
Fairchild Japan Corporation
Yotsubashi Chuo Bldg.
1-4-26, Shinmachi
Nishi-Ku, Osaka 550
Japan
Tel: 06-541-6138/9

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Pola Shibuya Bldg.
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Japan
Tel: 03-400-8351

Korea
Fairchild Semikor Ltd.
10th Floor, Life Bldg.
61 Yuido-Dong, Youngdongpo-Ku
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Tel: 783-3795

Scandinavia
Fairchild Semiconductor AB
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S-11620 Stockholm
Sweden
Tel: (08) 44.92.55

Singapore
Fairchild Semiconductor Pte. Ltd.
74 Bukit Timah Road #03-01/02
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Tel: 337-0511

Switzerland
Fairchild Semiconductor GmbH
Baumackerstrasse 46
CH-8050 Zuerich
Switzerland
Tel: (01) 311.42.30

Taiwan
Fairchild Electronics (Taiwan) Ltd.
Room 502, 5th Floor, Hsietsu Bldg.
47 Chung Shan N. Road, Sec. 3
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United Kingdom
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Hauppauge, New York 11788
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Hamilton/Avnet Electronics
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Rochester, New York 14623
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Buffalo, New York 14202
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Tel: 914-937-7400

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Tel: 919-878-0819

Schweber Electronics
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Raleigh, North Carolina 27604
Tel: 919-876-0000

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Arrow Electronics
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Centerville, Ohio 45459
Tel: 513-435-5563

Arrow Electronics
6238 Cochran Road
Solon, Ohio 44139
Tel: 216-248-3990

Hall-Mark Electronics
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Cincinnati, Ohio 45242
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Hall-Mark Electronics
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Solon, Ohio 44139
Tel: 216-349-4632

Hall-Mark Electronics
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Westerville, Ohio 43081
Tel: 614-891-4555

Hamilton/Avnet Electronics
954 Senate Drive
Dayton, Ohio 45459
Tel: 513-433-0610

Hamilton/Avnet Electronics
4588 Emery Industrial Parkway
Warrensville Heights, Ohio 44128
Tel: 216-831-3500

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Cleveland, Ohio 44105
Tel: 216-587-3600

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Tel: 513-236-9900

Schweber Electronics
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Beachwood, Ohio 44122
Tel: 216-464-2970

Schweber Electronics
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Dayton, Ohio 45459
Tel: 513-439-1800

Oklahoma
Arrow Electronics
4719 S. Memorial
Tulsa, Oklahoma 74145
Tel: 918-665-7700

Hall-Mark Electronics
5460 S. 103rd East Avenue
Tulsa, Oklahoma 74145
Tel: 918-665-3200

Schweber Electronics
4815 S. Sheridan Road
Tulsa, Oklahoma 74145
Tel: 918-622-8000

Oregon
Hamilton/Avnet Electronics
6024 SW Jean Road
Building C, Suite 10
Lake Oswego, Oregon 97034
Tel: 503-635-8157

Wyle Distribution Group
5289 NE Elam Young Parkway
Hillsboro, Oregon 97123
Tel: 503-640-6000

Pennsylvania
Arrow Electronics
650 Seco Road
Monroeville, Pennsylvania 15146
Tel: 412-856-7000

Pioneer Electronics
259 Kappa Drive
Pittsburgh, Pennsylvania 15238
Tel: 412-782-2300

Schweber Electronics
231 Gibraltor
Horsham, Pennsylvania 19044
Tel: 215-441-0600

Texas
Arrow Electronics
10125 Metropolitan Drive
Austin, Texas 78758
Tel: 512-835-4180

Arrow Electronics
13715 Gamma Road
Dallas, Texas 75234
Tel: 214-386-7500

Arrow Electronics
10899 Kinghurst, Suite 100
Houston, Texas 77099
Tel: 713-530-4700

Hall-Mark Electronics
12211 Technology Blvd.
Austin, Texas 78759
Tel: 512-258-8848

Hall-Mark Electronics
11333 Page Mill Drive
Dallas, Texas 75243
Tel: 214-343-5000

Hall-Mark Electronics
10375 Brockwood Road
Dallas, Texas 75238
Tel: 214-343-5000

Hall-Mark Electronics
8000 Westglen
Houston, Texas 77063
Tel: 713-781-6100

Hamilton/Avnet Electronics
2401 Rutland Drive
Austin, Texas 78757
Tel: 512-837-8911

Hamilton/Avnet Electronics
8750 Westpark
Houston, Texas 77063
Tel: 713-780-1771

Hamilton/Avnet Electronics
2111 W. Walnut Hill Lane
Irving, Texas 75062
Tel: 214-659-4111

Schweber Electronics
6300 La Calma Drive
Suite 240
Austin, Texas 78752
Tel: 512-458-8253

Schweber Electronics
4202 Beltway Drive
Dallas, Texas 75234
Tel: 214-661-5010

Schweber Electronics
10625 Richmond, Suite 100
Houston, Texas 77042
Tel: 713-784-3600

Sterling Electronics
23358 Kramer Lane
Austin, Texas 78758
Tel: 512-836-1341

Fairchild Semiconductor Authorized Distributors United States and Canada

Sterling Electronics
11090 Stemmons Freeway
Dallas, Texas 75229
Tel: 214-243-1600

Sterling Electronics
4201 Southwest Freeway
Houston, Texas 77027
Tel: 713-627-9800

Wyle Distribution Group
1810 N. Greenville
Richardson, Texas 75081
Tel: 214-235-9953

Wyle Labs
2120 West Braker
Suite F
Austin, Texas 78757

Zeus Components, Inc.
14001 Goldmark, Suite 250
Dallas, Texas 75240
Tel: 214-783-7010

Utah
Arrow Electronics
4980 Amelia Earhart Drive
Salt Lake City, Utah 84116
Tel: 801-539-1135

Bell Industries
3639 West 2150 South
Salt Lake City, Utah 84120
Tel: 801-972-6969

Hamilton/Avnet Electronics
1585 West 2100 South
Salt Lake City, Utah 84119
Tel: 801-972-2800

Wyle Distribution Group
1959 South 4130 West, Unit B
Salt Lake City, Utah 84104
Tel: 801-974-9953

Virginia
Arrow Electronics
8002 Discovery Drive
Richmond, Virginia 23285
Tel: 804-282-0413

Washington
Arrow Electronics
14320 NE 21st Street
Bellevue, Washington 98005
Tel: 206-643-4800

Hamilton/Avnet Electronics
14212 NE 21st Street
Bellevue, Washington 98005
Tel: 206-453-5844

Radar Electronic Co., Inc.
168 Western Avenue W
Seattle, Washington 98119
Tel: 206-282-2511

Wyle Distribution Group
1750 132nd Avenue NE
Bellevue, Washington 98005
Tel: 206-453-8300

Wisconsin
Arrow Electronics
430 W. Rawson Avenue
Oak Creek, Wisconsin 53154
Tel: 414-764-6600

Hall-Mark Electronics
9657 South 20th Street
Oak Creek, Wisconsin 53154
Tel: 414-761-3000

Hamilton/Avnet Electronics
2975 South Moorland Road
New Berlin, Wisconsin 53151
Tel: 414-784-4510

Schweber Electronics
150 Sunnyslope Road, Suite 120
Brookfield, Wisconsin 53005
Tel: 414-784-9020

Canada
Future Electronics Corporation
5809 MacLeod Trail S, Unit 109
Calgary, Alberta, T24 0J9, Canada
Tel: 403-259-6437

Future Electronics, Inc.
82 St. Regis Crescent North
Downsview, Ontario, M3J 1Z3, Canada
Tel: 416-638-4771

Future Electronics, Inc.
Baxter Center
1050 Baxter Road
Ottawa, Ontario, K2C 3P2, Canada
Tel: 613-820-8313

Future Electronics, Inc.
237 Hymus Blvd.
Pointe Claire, Quebec, H9R 5C7, Canada
Tel: 514-694-7710

Future Electronics Corporation
3070 Kingsway
Vancouver, B.C., B5R 5J7, Canada
Tel: 604-438-5545

Hamilton/Avnet Canada, Ltd.
6845 Rexwood Road, Units 3-4-5
Mississauga, Ontario, L4V 1R2, Canada
Tel: 416-677-7432

Hamilton/Avnet Canada, Ltd.
190 Colonnade Road
Nepean, Ontario, K2E 7J5, Canada
Tel: 613-226-1700

Hamilton/Avnet Canada, Ltd.
2670 Sabourin Street
St. Laurent, Quebec, H4S 1M2, Canada
Tel: 514-335-1000

Semad Electronics, Ltd.
9045 Cote De Liesse, Suite 101
Dorval, Quebec, H9P 2M9, Canada
Tel: 514-636-4614

Semad Electronics, Ltd.
864 Lady Ellen Place
Ottawa, Ontario, K1Z 5M2, Canada
Tel: 613-722-6571

Semad Electronics, Ltd.
85 Spy Court
Markham, Ontario, L3R 4Z4, Canada
Tel: 416-475-8500

54F/74F DC Family Characteristics

Symbol	Parameter		Limits Min	Limits Typ	Limits Max	Units	V_{CC}	Conditions	
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal over Recommended V_{CC} and T_A Range	
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal over Recommended V_{CC} and T_A Range	
V_{CD}	Input Clamp Diode Voltage				-1.2	V	Min	$I_{IN} = -18$ mA	
V_{OH}	Output HIGH Voltage Std/3-State	Mil	2.5	3.4		V	Min	$I_{OH} = -1$ mA	
		Com	2.7	3.4					
	Output HIGH Voltage 3-State/Line Driver	Mil	2.4	3.3		V	Min	$I_{OH} = -3$ mA	
		Com	2.7	3.3					
	Output HIGH Voltage Line Driver	Mil	2.0	3.2		V	Min	$I_{OH} = -12$ mA	
		Com	2.0	3.1				$I_{OH} = -15$ mA	
V_{OL}	Output LOW Voltage Standard	Mil		0.30	0.5	V	Min	$I_{OL} = 20$ mA	
		Com		0.30	0.5				
	Output LOW Voltage 3-State	Mil		0.30	0.5	V	Min	$I_{OL} = 20$ mA	
		Com		0.35	0.5			$I_{OL} = 24$ mA	
	Output LOW Voltage Line Driver	Mil		0.38	0.55	V	Min	$I_{OL} = 48$ mA	
		Com		0.42	0.55			$I_{OL} = 64$ mA	
I_{IH}	Input HIGH Current	0.5 U.L.			20	μA	Max	$V_{IN} = 2.7$ V	$I_{IH} = 40\ \mu$A Multiplied by Input HIGH U.L. Shown on Data Sheet
		n U.L.			n(40)				
	Input HIGH Current Breakdown Test, Std Inputs				100	μA	Max	$V_{IN} = 7.0$ V	
	Input HIGH Current Breakdown Test, Transceivers				1.0	mA	Max	$V_{IN} = 5.5$ V	
I_{IL}	Input LOW Current	0.375 U.L.			-0.6	mA	Max	$I_{IL} = -1.6$ mA Multiplied by Input LOW U.L. Shown on Data Sheet, $V_{IN} = 0.5$ V	
		n U.L.			n(-1.6)				
I_{OZH}	3-State Output OFF Current HIGH				50	μA	Max	$V_{OUT} = 2.7$ V	
I_{OZL}	3-State Output OFF Current LOW				-50	μA	Max	$V_{OUT} = 0.5$ V	
I_{OH}	Open Collector Output Leakage Current				100	μA	Min	$V_{IN} = V_{IH}/V_{IL}$ $V_{OUT} = V_{CC}$	
I_{OS}	Output Short-Circuit Current	Std/3-State	-60		-150	mA	Max	$V_{OUT} = 0$ V	
		Line Driver	-100		-225				

For additional information, refer to Section 3.

FAIRCHILD

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