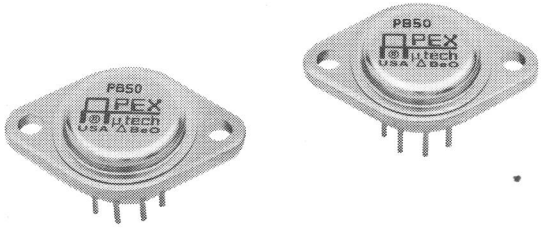
PB50
POWER BOOSTER AMPLIFIER

FEATURES

- WIDE SUPPLY RANGE — ±30V to ±100V
- HIGH OUTPUT CURRENT — Up to 2A Continuous
- VOLTAGE AND CURRENT GAIN
- HIGH SLEW — 50V/µs Minimum
- PROGRAMMABLE OUTPUT CURRENT LIMIT
- HIGH POWER BANDWIDTH — 160 kHz Minimum
- LOW QUIESCENT CURRENT — 12mA Typical



APPLICATIONS

- HIGH VOLTAGE INSTRUMENTATION
- Electrostatic TRANSDUCERS & DEFLECTION
- Programmable Power Supplies Up to 180V p-p

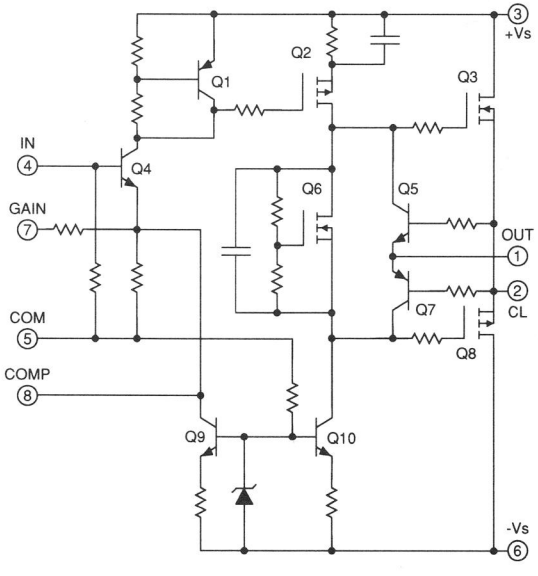
DESCRIPTION

The PB50 is a high voltage, high current amplifier designed to provide voltage and current gain for a small signal, general purpose op amp. Including the power booster within the feedback loop of the driver amplifier results in a composite amplifier with the accuracy of the driver and the extended output voltage range and current capability of the booster. The PB50 can also be used without a driver in some applications, requiring only an external current limit resistor to function properly.

The output stage utilizes complementary MOSFETs, providing symmetrical output impedance and eliminating secondary breakdown limitations imposed by Bipolar Junction Transistors. Internal feedback and gainset resistors are provided for a pin-strapable gain of 3. Additional gain can be achieved with a single external resistor. Compensation is not required for most driver/gain configurations, but can be accomplished with a single external capacitor. Although the booster can be configured quite simply, enormous flexibility is provided through the choice of driver amplifier, current limit, supply voltage, voltage gain, and compensation.

This hybrid circuit utilizes a beryllia (BeO) substrate, thick film resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8 pin TO-3 package is electrically isolated and hermetically sealed using one-shot resistance welding. The use of compressible isolation washers may void the warranty.

EQUIVALENT SCHEMATIC



TYPICAL APPLICATION

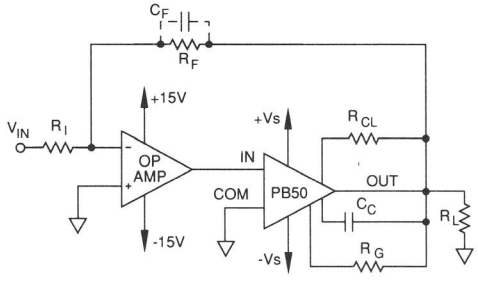
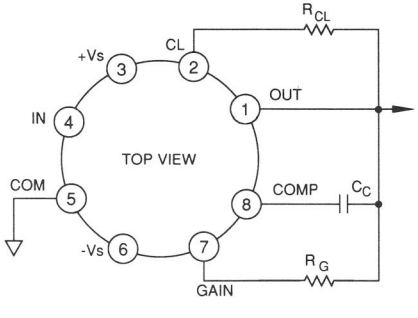


Figure 1. Inverting composite amplifier.

EXTERNAL CONNECTIONS



PB50 ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, +Vs to -Vs	200V
OUTPUT CURRENT, within SOA	2A
POWER DISSIPATION, internal at Tc = 25°C[1]	35W
INPUT VOLTAGE, referred to common	±15V
TEMPERATURE, pin solder -10 sec max	300°C
TEMPERATURE, junction[1]	150°C
TEMPERATURE, storage	-65 to +150°C
OPERATING TEMPERATURE RANGE, case	-55 to +125°C

CAUTION:
THE PB50 IS CONSTRUCTED FROM MOSFET TRANSISTORS. ESD HANDLING PROCEDURES MUST BE OBSERVED.

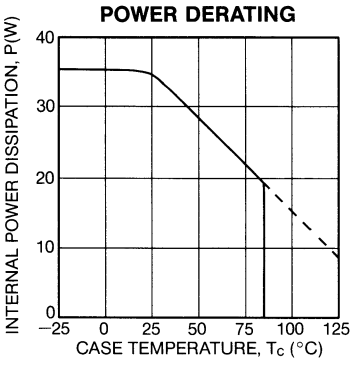
SPECIFICATIONS

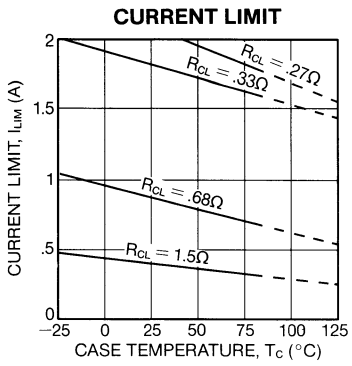
		PB58			
PARAMETER	**TEST CONDITIONS[2]**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT					
OFFSET VOLTAGE, initial			±.75	±1.75	V
OFFSET VOLTAGE, vs. temperature	Full temperature range		-4.5	-7	mV/°C
INPUT IMPEDANCE, dc		25	50		kΩ
INPUT CAPACITANCE			3		pF
INPUT VOLTAGE RANGE	Referred to common			±15	V
CLOSED LOOP GAIN RANGE		3	10	25	V/V
GAIN ACCURACY, internal Rg, Rf	AV = 3		±10	±15	%
GAIN ACCURACY, external Rf	AV = 10		±15	±25	%
PHASE SHIFT	f = 10kHz, AV_{CL} = 10, C_C = 22pF		10		°
	f = 200kHz, AV_{CL} = 10, C_C = 22pF		60		°
OUTPUT					
VOLTAGE SWING	Io = 2A	Vs -11	Vs -9		V
VOLTAGE SWING	Io = 1A	Vs -10	Vs -7		V
VOLTAGE SWING	Io = .1A	Vs -8	Vs -5		V
CURRENT, continuous		2			A
SLEW RATE	Full temperature range	50	100		V/µs
CAPACITIVE LOAD	Full temperature range		2200		pF
SETTLING TIME to .1%	R_L = 100Ω, 2V step		2		µs
POWER BANDWIDTH	Vo = 100 Vpp	160	320		kHz
SMALL SIGNAL BANDWIDTH	Cc = 22pF, A_V = 25, Vcc = ±100		100		kHz
SMALL SIGNAL BANDWIDTH	Cc = 22pF, A_V = 3, Vcc = ±30		1		MHz
POWER SUPPLY					
VOLTAGE, ±Vs[3]	Full temperature range	±30[5]	±60	±100	V
CURRENT, quiescent	Vs = ±30		9	12	mA
	Vs = ±60		12	18	mA
	Vs = ±100		17	25	mA
THERMAL					
RESISTANCE, AC, junction to case[4]	Full temp. range, F>60Hz		1.8	2.0	°C/W
RESISTANCE, DC, junction to case	Full temp. range, F<60Hz		3.2	3.5	°C/W
RESISTANCE, junction to air	Full temp. range		30		°C/W
TEMPERATURE RANGE, case	Meets full range specification	-25	25	85	°C

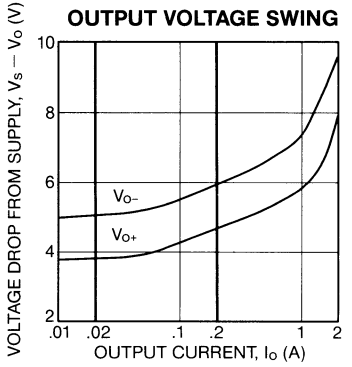
NOTES:
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF (Mean Time to Failure).
2. The power supply voltage specified under typical (TYP) applies, Tc = 25°C unless otherwise noted.
3. +Vs and -Vs denote the positive and negative supply rail respectively.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
5. -Vs must be at least 30V below COM.

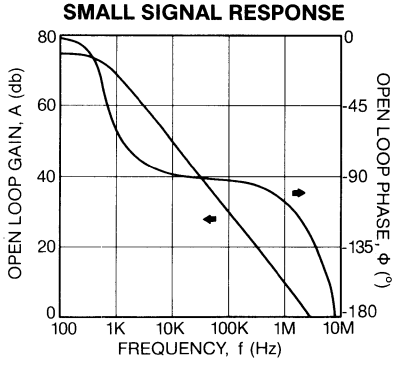
CAUTION: The internal substrate contains berylia (BeO). Do not break the seal. If broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

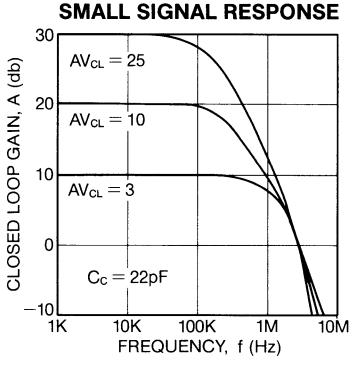
PB50 TYPICAL PERFORMANCE GRAPHS

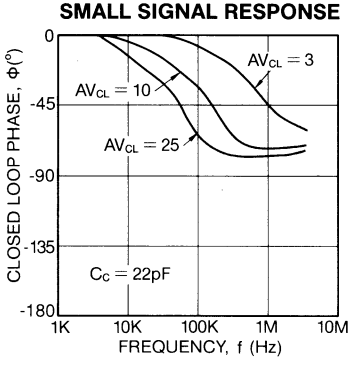


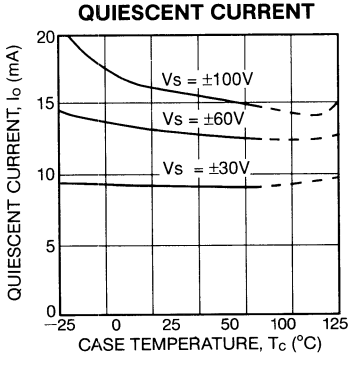


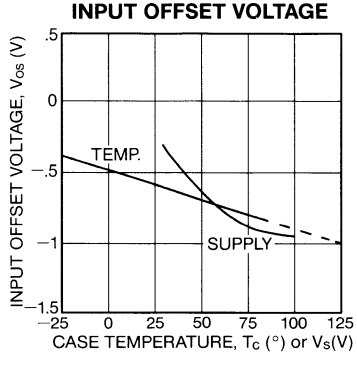


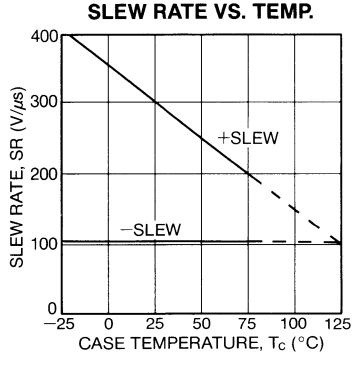


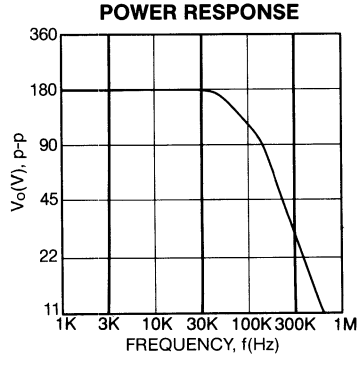


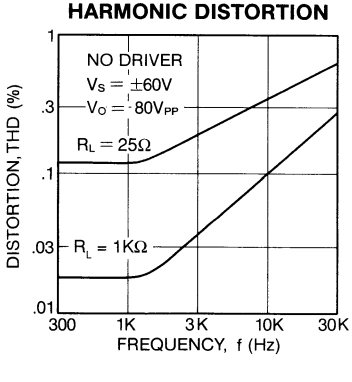


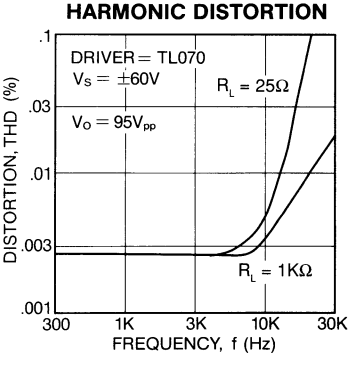












PB50 OPERATING CONSIDERATIONS

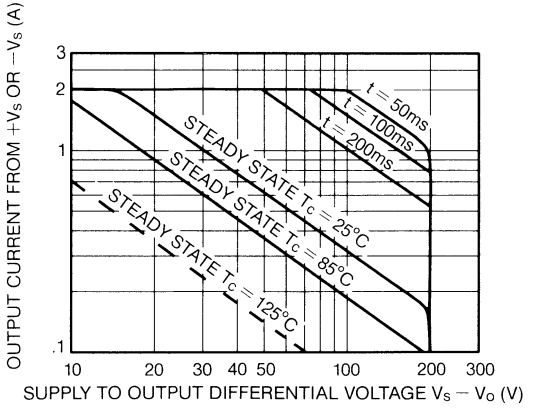
GENERAL

Please read the "General Operating Considerations" section, which covers stability, supplies, heatsinking, mounting, current limit, SOA interpretation, and specification interpretation. Additional information can be found in the applications notes. For information on the package outline, heatsinks, and mounting hardware, consult the "Accessory and Package Mechanical Data" section of the handbook.

CURRENT LIMIT

For proper operation, the current limit resistor (R_{CL}) must be connected as shown in the external connection diagram. The minimum value is 0.27Ω with a maximum practical value of 47Ω. For optimum reliability the resistor value should be set as high as possible. The value is calculated as follows: $+I_L = .65/R_{CL} + .010$, $-I_L = .65/R_{CL}$.

SAFE OPERATING AREA (SOA)



NOTE: The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

COMPOSITE AMPLIFIER CONSIDERATIONS

Cascading two amplifiers within a feedback loop has many advantages, but also requires careful consideration of several amplifier and system parameters. The most important of these are gain, stability, slew rate, and output swing of the driver. Operating the booster amplifier in higher gains results in a higher slew rate and lower output swing requirement for the driver, but makes stability more difficult to achieve.

GAIN SET

$$R_G = [\,(Av-1) * 3.1K] - 6.2K$$

$$Av = \frac{R_G + 6.2K}{3.1K} + 1$$

The booster's closed-loop gain is given by the equation above. The composite amplifier's closed loop gain is determined by the feedback network, that is: -Rf/Ri (inverting) or 1+Rf/Ri (non-inverting). The driver amplifier's "effective gain" is equal to the composite gain divided by the booster gain.

Example: Inverting configuration (figure 1) with
R i = 2K, R f = 60K, R g = 0 :
Av (booster) = (6.2K/3.2K) + 1 = 3
Av (composite) = 60K/2K = - 30
Av (driver) = - 30/3 = -10

STABILITY

Stability can be maximized by observing the following guidelines:
1. Operate the booster in the lowest practical gain.
2. Operate the driver amplifier in the highest practical effective gain.
3. Keep gain-bandwidth product of the driver lower than the closed loop bandwidth of the booster.
4. Minimize phase shift within the loop.

A good compromise for (1) and (2) is to set booster gain from 3 to 10 with total (composite) gain at least a factor of 3 times booster gain. Guideline (3) implies compensating the driver as required in low composite gain configurations. Phase shift within the loop (4) is minimized through use of booster and loop compensation capacitors Cc and Cf when required. Typical values are 5pF to 33pF.

Stability is the most difficult to achieve in a configuration where driver effective gain is unity (ie; total gain = booster gain). For this situation, Table 1 gives compensation values for optimum square wave response with the op amp drivers listed.

DRIVER	C_{CH}	C_F	C_c	FPBW	SR
OP07	-	22p	22p	4kHz	1.5
741	-	18p	10p	20kHz	7
LF155	-	4.7p	10p	60kHz	>60
LF156	-	4.7p	10p	80kHz	>60
TL070	22p	15p	10p	80kHz	>60

For: R_F = 33K, R_I = 3.3K, R_G = 22K

Table 1: Typical values for case where op amp effective gain = 1.

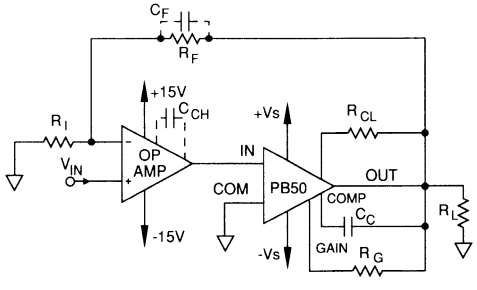


Figure 2. Non-inverting composite amplifier.

SLEW RATE

The slew rate of the composite amplifier is equal to the slew rate of the driver times the booster gain, with a maximum value equal to the booster slew rate.

OUTPUT SWING

The maximum output voltage swing required from the driver op amp is equal to the maximum output swing from the booster divided by the booster gain. The Vos of the booster must also be supplied by the driver, and should be subtracted from the available swing range of the driver. Note also that effects of Vos drift and booster gain accuracy should be considered when calculating maximum available driver swing.

EMTRON
electronic vertriebs gmbh

PB58 • PB58A

POWER BOOSTER AMPLIFIER

FEATURES

- WIDE SUPPLY RANGE — ±15V to ±150V
- HIGH OUTPUT CURRENT — 1.5A Continuous (PB58), 2.0A Continuous (PB58A)
- VOLTAGE AND CURRENT GAIN
- HIGH SLEW — 50V/µs Min (PB58), 75V/µs Min (PB58A)
- PROGRAMMABLE OUTPUT CURRENT LIMIT
- HIGH POWER BANDWIDTH — 320 kHz Typical
- LOW QUIESCENT CURRENT — 12mA Typical

APPLICATIONS

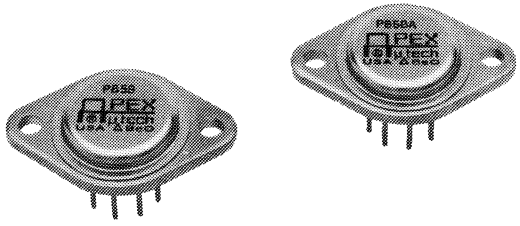
- HIGH VOLTAGE INSTRUMENTATION
- Electrostatic TRANSDUCERS & DEFLECTION
- Programmable Power Supplies Up to 280V p-p

DESCRIPTION

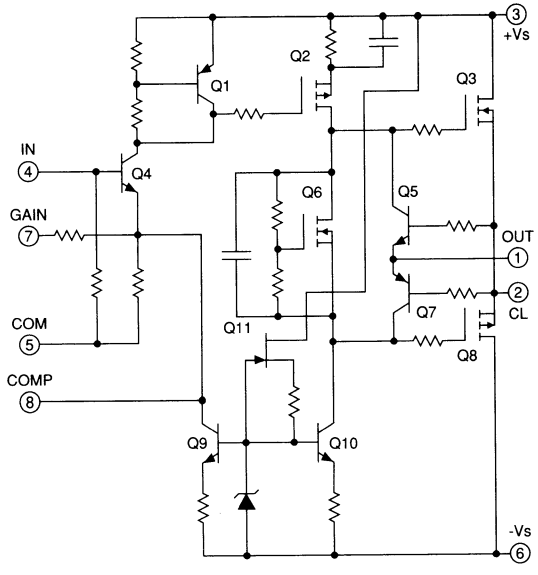
The PB58 is a high voltage, high current amplifier designed to provide voltage and current gain for a small signal, general purpose op amp. Including the power booster within the feedback loop of the driver amplifier results in a composite amplifier with the accuracy of the driver and the extended output voltage range and current capability of the booster. The PB58 can also be used without a driver in some applications, requiring only an external current limit resistor to function properly.

The output stage utilizes complementary MOSFETs, providing symmetrical output impedance and eliminating secondary breakdown limitations imposed by Bipolar Transistors. Internal feedback and gainset resistors are provided for a pin-strapable gain of 3. Additional gain can be achieved with a single external resistor. Compensation is not required for most driver/gain configurations, but can be accomplished with a single external capacitor. Enormous flexibility is provided through the choice of driver amplifier, current limit, supply voltage, voltage gain, and compensation.

This hybrid circuit utilizes a beryllia (BeO) substrate, thick film resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8 pin TO-3 package is electrically isolated and hermetically sealed using one-shot resistance welding. The use of compressible isolation washers may void the warranty.



EQUIVALENT SCHEMATIC



TYPICAL APPLICATION

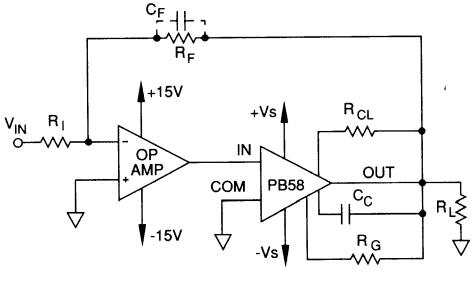
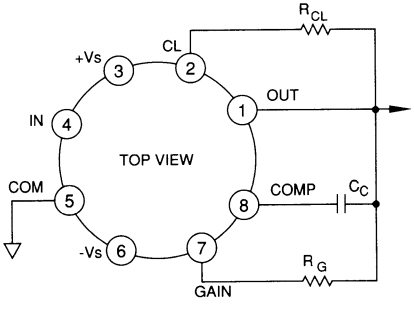


Figure 1. Inverting composite amplifier.

EXTERNAL CONNECTIONS



PB58 ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, +Vs to -Vs	300V
OUTPUT CURRENT, within SOA	2.0A
POWER DISSIPATION, internal at Tc = 25°C[1]	83W
INPUT VOLTAGE, referred to common	±15V
INPUT VOLTAGE, referred to +Vs	+Vs -6.5V
TEMPERATURE, pin solder -10 sec max	300°C
TEMPERATURE, junction[1]	175°C
TEMPERATURE, storage	-65 to +150°C
OPERATING TEMPERATURE RANGE, case	-55 to +125°C

CAUTION:
THE PB58 IS CONSTRUCTED FROM MOSFET TRANSISTORS. ESD HANDLING PROCEDURES MUST BE OBSERVED.

SPECIFICATIONS

		PB58			PB58A			
PARAMETER	**TEST CONDITIONS[2]**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT								
OFFSET VOLTAGE, initial			±.75	±1.5		*	±1.0	V
OFFSET VOLTAGE, vs. temperature	Full temperature range[3]		-4.5	-7		*	*	mV/°C
INPUT IMPEDANCE, dc		25	50		*	*		kΩ
INPUT CAPACITANCE			3			*		pF
INPUT VOLTAGE RANGE	Referred to common			±15			*	V
CLOSED LOOP GAIN RANGE		3	10	25	*	*	*	V/V
GAIN ACCURACY, internal Rg, Rf	AV = 3		±10	±15		*	*	%
GAIN ACCURACY, external Rf	AV = 10		±15	±25		*	*	%
PHASE SHIFT	f = 10kHz, AV_{CL} = 10, C_C = 22pF		10			*		°
	f = 200kHz, AV_{CL} = 10, C_C = 22pF		60			*		°
OUTPUT								
VOLTAGE SWING	Io = 1.5A (PB58), 2A (PB58A)	Vs -11	Vs -8		Vs -12	Vs -9		V
VOLTAGE SWING	Io = 1A	Vs -10	Vs -7		*	*		V
VOLTAGE SWING	Io = .1A	Vs -8	Vs -5		*	*		V
CURRENT, continuous		1.5			2.0			A
SLEW RATE	Full temperature range	50	100		75	*		V/µs
CAPACITIVE LOAD	Full temperature range		2200			*		pF
SETTLING TIME to .1%	R_L = 100Ω, 2V step		2			*		µs
POWER BANDWIDTH	Vo = 100 Vpp	160	320		240	*		kHz
SMALL SIGNAL BANDWIDTH	Cc = 22pF, A_V = 25, Vcc = ±100		100			*		kHz
SMALL SIGNAL BANDWIDTH	Cc = 22pF, A_V = 3, Vcc = ±30		1			*		MHz
POWER SUPPLY								
VOLTAGE, ±Vs[4]	Full temperature range	±15[6]	±60	±150	*	*	*	V
CURRENT, quiescent	Vs = ±15		11			*		mA
	Vs = ±60		12			*		mA
	Vs = ±150		14	18		*	*	mA
THERMAL								
RESISTANCE, AC, junction to case[5]	Full temp. range, F>60Hz		1.2	1.3		*	*	°C/W
RESISTANCE, DC, junction to case	Full temp. range, F<60Hz		1.6	1.8		*	*	°C/W
RESISTANCE, junction to air	Full temp. range		30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specification	-25	25	85	*	*	*	°C

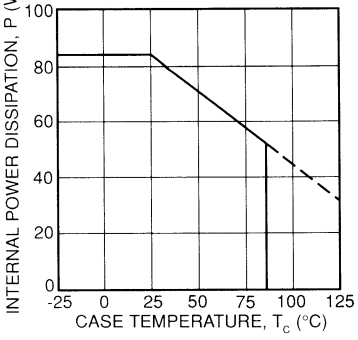
NOTES: * The specification of PB58A is identical to the specification for PB58 in applicable column to the left.

1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF (Mean Time to Failure).
2. The power supply voltage specified under typical (TYP) applies, Tc = 25°C unless otherwise noted.
3. Guaranteed by design but not tested.
4. +Vs and -Vs denote the positive and negative supply rail respectively.
5. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
6. -Vs must be at least 15V below common.

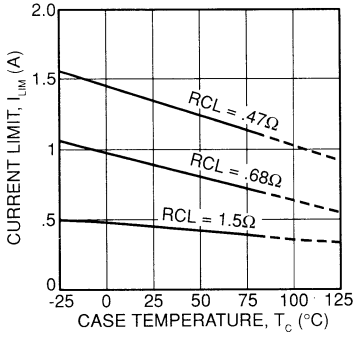
CAUTION: The internal substrate contains beryllia (BeO). Do not break the seal. If broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

PB58 TYPICAL PERFORMANCE GRAPHS

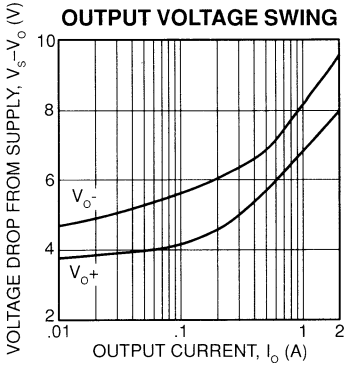
POWER DERATING



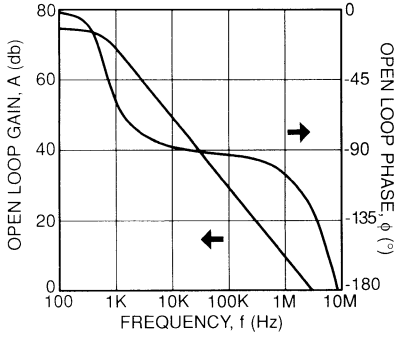
CURRENT LIMIT



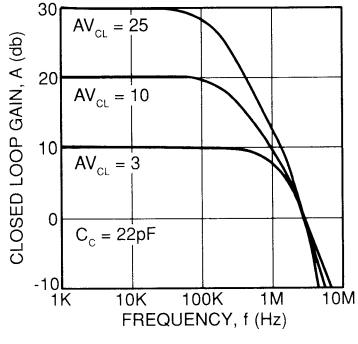
OUTPUT VOLTAGE SWING



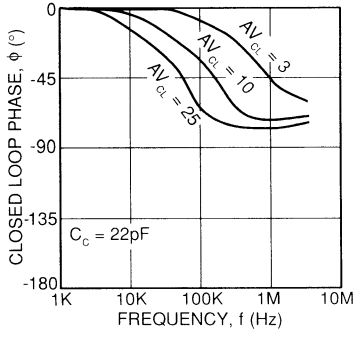
SMALL SIGNAL RESPONSE



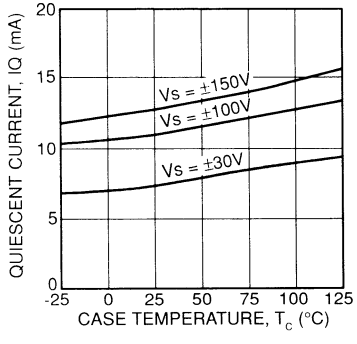
SMALL SIGNAL RESPONSE



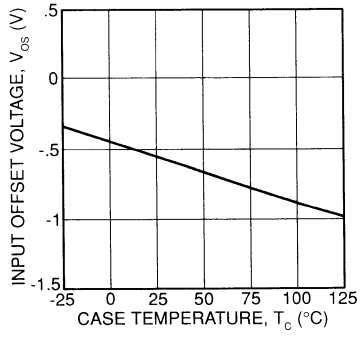
SMALL SIGNAL RESPONSE



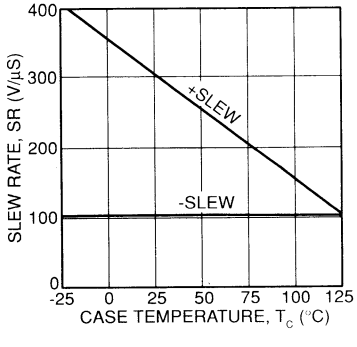
QUIESCENT CURRENT



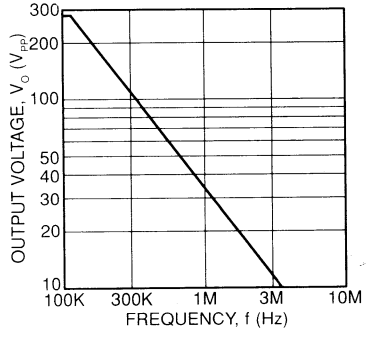
INPUT OFFSET VOLTAGE



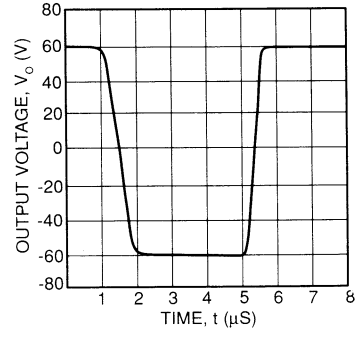
SLEW RATE Vs. TEMP.



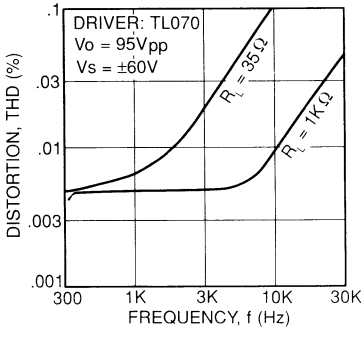
POWER RESPONSE



PULSE RESPONSE



HARMONIC DISTORTION



PB58 OPERATING CONSIDERATIONS

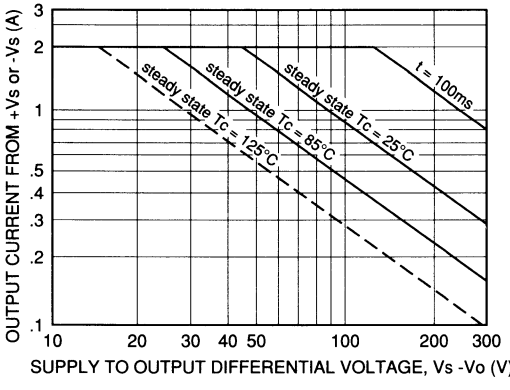
GENERAL

Please read the "General Operating Considerations" section, which covers stability, supplies, heatsinking, mounting, current limit, SOA interpretation, and specification interpretation. Additional information can be found in the applications notes. For information on the package outline, heatsinks, and mounting hardware, consult the "Accessory and Package Mechanical Data" section of the handbook.

CURRENT LIMIT

For proper operation, the current limit resistor (R_{CL}) must be connected as shown in the external connection diagram. The minimum value is 0.33Ω with a maximum practical value of 47Ω. For optimum reliability the resistor value should be set as high as possible. The value is calculated as follows: $+I_L = .65/R_{CL} + .010$, $-I_L = .65/R_{CL}$.

SAFE OPERATING AREA (SOA)



NOTE: The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

COMPOSITE AMPLIFIER CONSIDERATIONS

Cascading two amplifiers within a feedback loop has many advantages, but also requires careful consideration of several amplifier and system parameters. The most important of these are gain, stability, slew rate, and output swing of the driver. Operating the booster amplifier in higher gains results in a higher slew rate and lower output swing requirement for the driver, but makes stability more difficult to achieve.

GAIN SET

$$R_G = [\,(Av-1) * 3.1K] - 6.2K$$

$$Av = \frac{R_G + 6.2K}{3.1K} + 1$$

The booster's closed-loop gain is given by the equation above. The composite amplifier's closed loop gain is determined by the feedback network, that is: -Rf/Ri (inverting) or 1+Rf/Ri (non-inverting). The driver amplifier's "effective gain" is equal to the composite gain divided by the booster gain.

Example: Inverting configuration (figure 1) with
R i = 2K, R f = 60K, R g = 0 :
Av (booster) = (6.2K/3.2K) + 1 = 3
Av (composite) = 60K/2K = - 30
Av (driver) = - 30/3 = -10

STABILITY

Stability can be maximized by observing the following guidelines:
1. Operate the booster in the lowest practical gain.
2. Operate the driver amplifier in the highest practical effective gain.
3. Keep gain-bandwidth product of the driver lower than the closed loop bandwidth of the booster.
4. Minimize phase shift within the loop.

A good compromise for (1) and (2) is to set booster gain from 3 to 10 with total (composite) gain at least a factor of 3 times booster gain. Guideline (3) implies compensating the driver as required in low composite gain configurations. Phase shift within the loop (4) is minimized through use of booster and loop compensation capacitors Cc and Cf when required. Typical values are 5pF to 33pF.

Stability is the most difficult to achieve in a configuration where driver effective gain is unity (ie; total gain = booster gain). For this situation, Table 1 gives compensation values for optimum square wave response with the op amp drivers listed.

DRIVER	C_{CH}	C_F	C_C	FPBW	SR
OP07	-	22p	22p	4kHz	1.5
741	-	18p	10p	20kHz	7
LF155	-	4.7p	10p	60kHz	>60
LF156	-	4.7p	10p	80kHz	>60
TL070	22p	15p	10p	80kHz	>60
For: R_F = 33K, R_I = 3.3K, R_G = 22K					

Table 1: Typical values for case where op amp effective gain = 1.

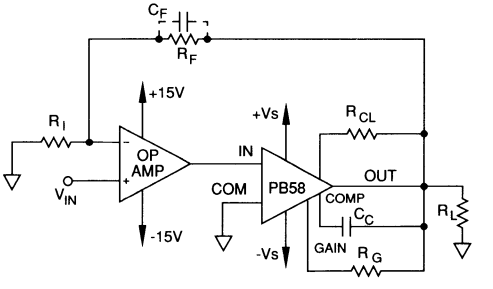


Figure 2. Non-inverting composite amplifier.

SLEW RATE

The slew rate of the composite amplifier is equal to the slew rate of the driver times the booster gain, with a maximum value equal to the booster slew rate.

OUTPUT SWING

The maximum output voltage swing required from the driver op amp is equal to the maximum output swing from the booster divided by the booster gain. The Vos of the booster must also be supplied by the driver, and should be subtracted from the available swing range of the driver. Note also that effects of Vos drift and booster gain accuracy should be considered when calculating maximum available driver swing.

EMTRON
electronic vertriebs gmbh

WB05
WIDEBAND BUFFER

FEATURES

- HIGH OUTPUT CURRENT—1A DC, 1.5A PEAK
- WIDE SUPPLY VOLTAGE RANGE—±5 TO ±15V
- SEPARATE FRONT-END AND OUTPUT SUPPLIES
- LOW SATURATION VOLTAGE—3.5V
- HIGH SLEW RATE— 10,000 V/µs @ 1A
  15,000 V/µs @ 0.5A
- LOW QUIESCENT CURRENT—30mA
- SLEEP MODE CONTROL—2.5mA
- HIGH FULL POWER BANDWIDTH—70MHz

APPLICATIONS

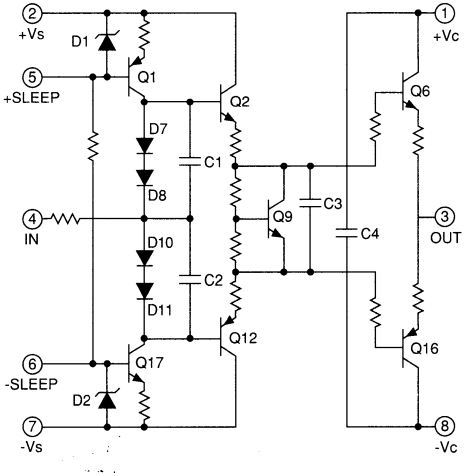
- LASER DIODE DRIVE
- GATE DRIVE FOR LARGE FETS
- SEMICONDUCTOR TESTING

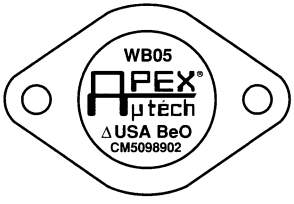
DESCRIPTION

The WB05 is a high slew rate, high current, wideband buffer capable of internal power dissipation of up to 15 watts. It provides high output currents of 1A continuous, and 1.5A peaks, under pulsed conditions. Typical circuit configuration using the WB05 will be a composite amplifier arrangement. Therefore, input capacitance has been minimized to reduce the drive requirements from the driver amplifier. A sleep mode feature has been incorporated to lower quiescent current during standby modes for battery powered applications.

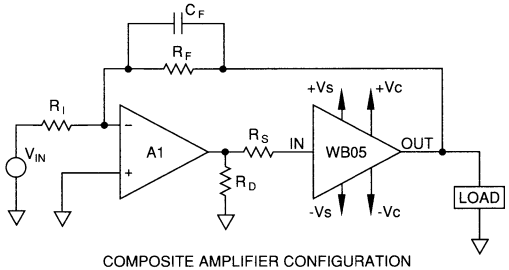
This hybrid circuit utilizes thick film (cermet) resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8 pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible isolation washers may void the warranty.

EQUIVALENT SCHEMATIC





TYPICAL APPLICATION

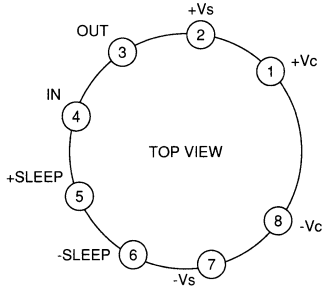


COMPOSITE AMPLIFIER CONFIGURATION

In this composite amplifier configuration, R_F and R_I should be kept as small as possible consistent with input impedance and gain requirements. Using low value resistors prevents high impedance nodes from acting as antennas, which could cause output signals to be picked up as positive feedback and result in oscillations. Low values also keep input and stray capacitance time constants low, for high speed and improved settling time. C_F is used to optimize settling time by compensating for input and stray capacitances. R_D (typically 500Ω) reduces the ouput impedance of A1 while R_S (typically 10-30Ω) provides damping for strays. The driver op amp must be capable of supplying adequate phase margin for itself and the WB05 at the closed loop gain used.

The driver amplifier also must be capable of providing enough current to drive R_D as well as charge the WB05's input and any other stray capacitances, at the intended slew rate. The phase shift introduced by the WB05 will increase the minimum required gain of the driver amplifier to guarantee stability. If the driver amplifier is a transimpedance amplifier, the inverting configuration shown will typically exhibit better slew rate and rise time than a noninverting configuration. This effect is due to the nature of the front end of most transimpedance amplifiers and the current available for turning on the output stage in the two different configurations.

EXTERNAL CONNECTIONS



NOTE: If SLEEP pins are unused, leave open

WB05 ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$, $+V_C$ to $-V_C$	30V
OUTPUT CURRENT, within SOA	1.5A
POWER DISSIPATION, internal at T_C = 25°C	15W
INPUT VOLTAGE RANGE	$\pm V_S$
TEMPERATURE, pins solder—10 sec max	300°C
TEMPERATURE, junction(1)	175°C
TEMPERATURE, storage	-65 to 175°C
OPERATING TEMPERATURE RANGE, case	-25 to +85°C

SPECIFICATIONS

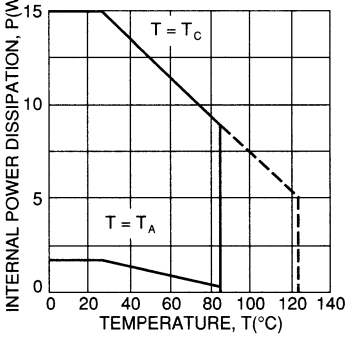
		WB05			
PARAMETER	**TEST CONDITIONS(2)**	**MIN**	**TYP**	**MAX**	**UNITS**
OFFSET VOLTAGE, initial			30	100	mV
OFFSET VOLTAGE, vs. temperature			100	500	µV/°C
BIAS CURRENT	V_{IN} = 0V		150	700	µA
INPUT CAPACITANCE			4		pF
INPUT VOLTAGE RANGE	I_{IN} < 1mA	$\pm V_S \mp 2$	$\pm V_S \mp 1.7$		V
INPUT OVERDRIVE CURRENT	$V_{IN} = +V_S$ or $V_{IN} = -V_S$		5	7	mA
PHASE SHIFT	f = 40MHz, R_L = 10Ω		8		°
	f = 150MHz, R_L = 10Ω		25		°
OUTPUT					
SATURATION VOLTAGE, (V_C-V_O)	I_O = 0.5A, $V_C = V_S$ - 3	2.2	1.8		V
	I_O = 1A, $V_C = V_S$ - 3	3.5	2.7		V
	I_O = 1A, $V_C = V_S$	6.5	6		V
OUTPUT CURRENT, continuous				1	A
OUTPUT CURRENT, pulsed	50% duty cycle, 10 ms pulse			1.5	A
SLEW RATE	R_L = 10Ω, V_{IN} = 15V/ns	8	10		V/ns
POWER BANDWIDTH	$V_C = V_S = \pm 15$, R_L = 20Ω	50	70		MHz
POWER BANDWIDTH	$V_C = V_S = \pm 5$, R_L = 20Ω		10		MHz
SETTLING TIME	8V step, R_L = 8Ω, to 0.1%		60		ns
	2V step, R_L = 10Ω, to 0.1%		22		ns
SMALL SIGNAL BANDWIDTH	$V_C = V_S = \pm 15$		250		MHz
OUTPUT IMPEDANCE	$V_C = V_S = \pm 15$, f = 1MHz		2		Ω
SMALL SIGNAL RISETIME	1V step, R_L = 10, $\pm V_S = \pm V_C$ = 15V		1.7		ns
SMALL SIGNAL PROP. DELAY	1V step, R_L = 10, $\pm V_S = \pm V_C$ = 15V		0.8		ns
DC GAIN	R_L = 10Ω, $\pm V_S = \pm V_C$ = 15V	0.82	0.87	0.93	V/V
POWER SUPPLY					
VOLTAGE (V_C, V_S)	Full temperature range	±5	±15	±15	V
QUIESCENT CURRENT			30	35	mA
	Sleep mode		2.5	3.5	mA
THERMAL					
RESISTANCE, AC junction to case(3)	Full temp. range, f > 60Hz		6	7.2	°C/W
RESISTANCE, DC junction to case	Full temp. range, f < 60Hz		8.3	10	°C/W
RESISTANCE, junction to air	Full temperature range		30		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	-25	25	85	°C

NOTES:
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
2. Case temperature is 25°C and the power supply voltage for all specifications is the TYP rating otherwise noted as a test condition.
3. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.

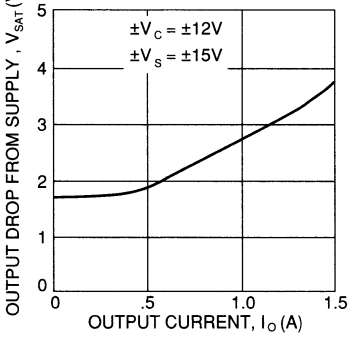
CAUTION: The internal substrate contains beryllia (BeO). Do not break the seal. If broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

WB05 TYPICAL PERFORMANCE GRAPHS

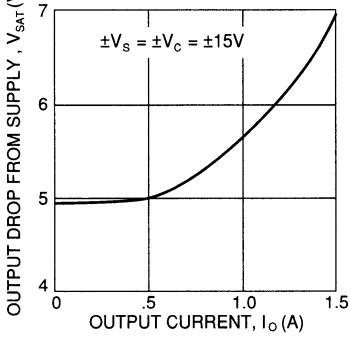
POWER DERATING



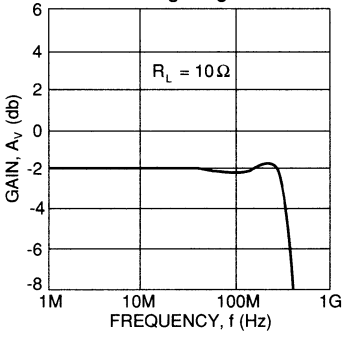
SATURATION VOLTAGE



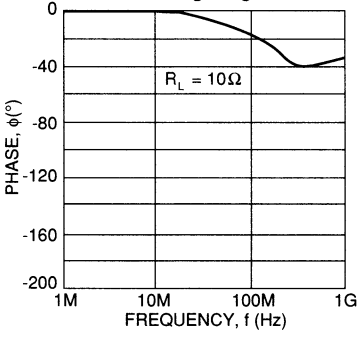
SATURATION VOLTAGE



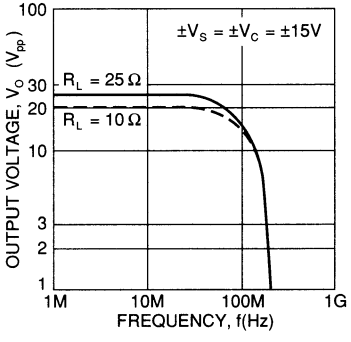
GAIN, $V_S = V_C = 15V$



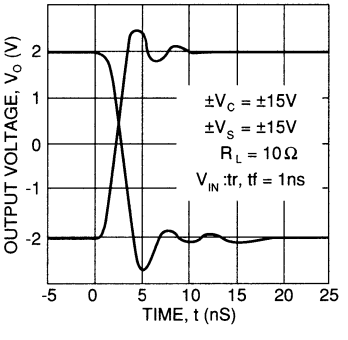
PHASE, $V_S = V_C = 15V$



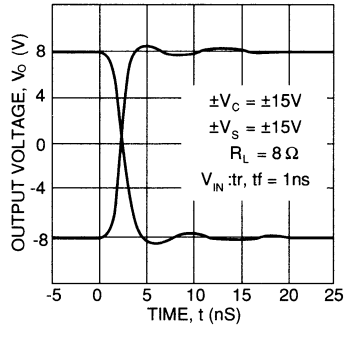
POWER RESPONSE



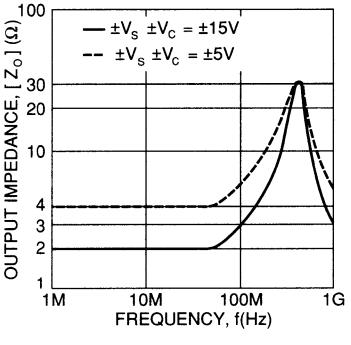
SMALL SIGNAL PULSE RESPONSE



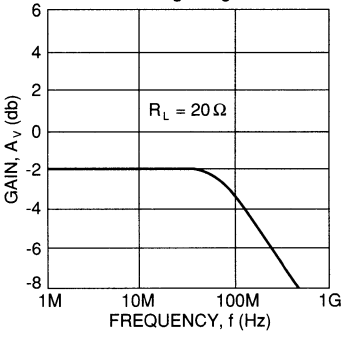
LARGE SIGNAL PULSE RESPONSE



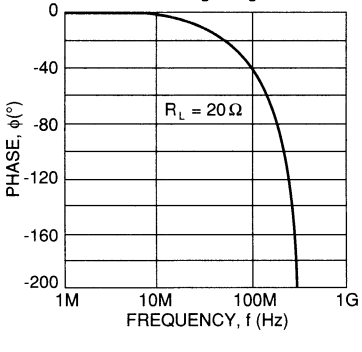
OUTPUT IMPEDANCE



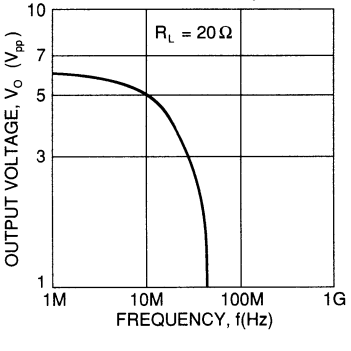
GAIN, $V_S = V_C = 5V$



PHASE, $V_S = V_C = 5V$



POWER RESPONSE, $V_S = V_C = 5V$

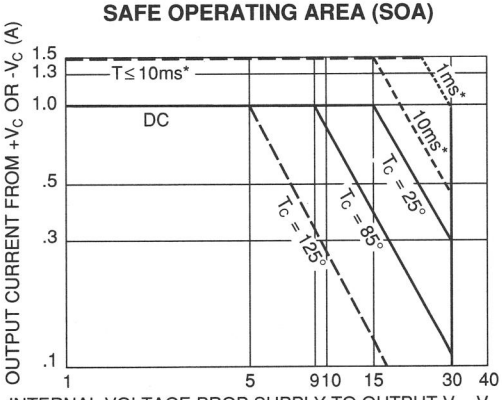


WB05 OPERATING CONSIDERATIONS

GENERAL

Please read the "General Operating Considerations" section, which covers stability, supplies, heatsinking, mounting, current limit, SOA interpretation, and specification interpretation. Additional information can be found in AN #15, "Applying the Ultra-fast WB05." For information on the package outline, heatsinks, and mounting hardware, consult the "Accessory and Package Mechanical Data" section of the handbook.

SAFE OPERATING AREA (SOA)



*Pulsed operation: duty cycle less than or equal to 50%.

USE OF SUPPLY PINS FOR BOOST

The output stage supply voltage can be reduced or have series resistors installed to reduce power dissipation in the buffer if required. Output stage supply pins should be bypassed on the buffer side of the series resistors if they are used. Reduced output supplies (or increased input supplies) will also improve output voltage swing to the rail (V_{SAT}).

HIGH Z_L AND/OR C_L

The WB05 has been optimized for high current/low impedance loads. With large load impedances (Z_L > 100Ω) or high capacitive loading (C_L > 150pF), the buffer may show peaking in the small signal response. If required, a series R-C network with 22Ω and 68 pF can be connected from the output to ground to flatten the response.

CURRENT LIMIT

The scheme shown in Figure 1 is rather slow but is cost effective if the WB05 must be operated in a system where available supply voltages exceed ±15V or when it is desired to reduced power dissipation in the WB05 by running the output stage power supplies ($\pm V_c$) at a lower voltage. This circuit provides both regulated voltage and output current limit.

The circuit shown in Figure 2 takes advantage of the WB05 sleep pins. With Figure 2 there is a 10μs delay until the current is limited.

SLEEP MODE

The WB05 quiescent current will drop from ≈30mA to ≈2.5mA when both sleep pins are pulled within 100mV of their respective supply pins. A typical circuit is shown in Figure 3.

COMPOSITE AMPLIFIER CONSIDERATIONS

When the WB05 is used as shown in the "TYPICAL APPLICATION" figure, the phase shift of the WB05 is inside the feedback loop for A1 and must be considered for stability calculations. See AN #15.

SLEW RATE

The WB05 output can slew no faster than its input is driven. To achieve high input slew rates, keep driving impedances as low as practical. Note that any strays from layout will add to the input capacitance of the buffer and may form a pole with driving network resistance or driver output impedance.

LAYOUT AND BYPASS

The WB05 requires good VHF/UHF lead dress and layout due to its 250MHz small signal bandwidth. Output currents of up to 1.5A and high dV/dt at the output can cause unwanted inductive and capacitive coupling, respectively, in your layout. Recommended power supply bypassing is as follows:

Vc = Vs: On each supply rail, V+ and V-, place in parallel the following capacitors:
C1, C4 = 330 to 1000 pF ceramic capacitor
C2, C5 = 0.01 to 0.033 μF ceramic capacitor
C3, C6 = 2.2 to 6.8 μF low ESR tantalum electrolytic

Vc ≠ Vs: On each Vc supply rail, +Vc and -Vc, place in parallel the following capacitors:
C1, C6 = 330 to 1000 pF ceramic capacitor
C2, C7 = 0.01 to 0.033 μF ceramic capacitor
C3, C8 = 2.2 to 6.8 μF low ESR tantalum electrolytic

On each Vs supply rail, +Vs and -Vs, place in parallel the following capacitors:
C4, C9 = 0.01 to 0.033 μF ceramic capacitor
C5, C10 = 330 to 1,000pF ceramic capacitor

All capacitors must be as close to the buffer supply pins as possible, with short leads (1/8" to 1/4") and/or short, wide PCB traces to minimize stray inductances.

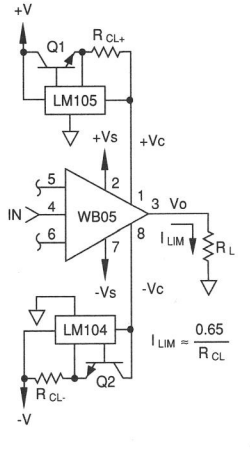


Figure 1: Output voltage regulation and current limit.

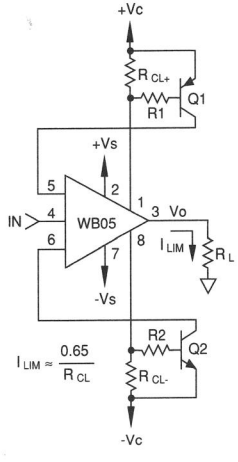


Figure 2: Current limit using sleep pins.

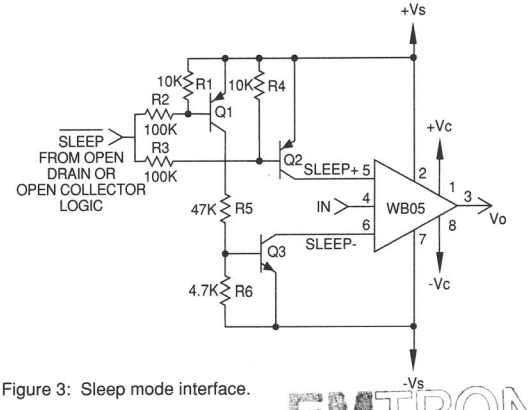


Figure 3: Sleep mode interface.