Am29501A

Multi-Port Pipelined Processor (Byte-Slice™)

DISTINCTIVE CHARACTERISTICS

- Expandable Byte-Slice™ Register-ALU
  - Sign extend input and output
  - Carry and $\overline{P}/\overline{G}$ expansion with force/inhibit/normal carry modes
- Eight instruction ALU
  - Four arithmetic operations
  - Four logic operations
- Ten internal data paths
  - Highly parallel architectures
  - Multiple simultaneous data manipulations

- Pipeline register file has six 8-bit registers
  - Multilevel pipelining
  - Multiple simultaneous register-to-register moves
- Completely microprogrammable
  - No instruction encoding
  - All operation combinations available
- Three I/O ports for maximum system interconnect flexibility
- Single 5-V supply with TTL I/O
- Plug-in compatible with Am29501

GENERAL DESCRIPTION

The Am29501A is an expandable Byte-Slice™ register-ALU designed to bring maximum speed to array processing and digital signal processing systems. It provides a flexible processor building block for implementing highly pipelined, highly parallel architectures where speed is achieved by a combination of optimized integrated circuit technology (IMOX™ process and internal ECL circuitry) and customized system architecture. I/O port flexibility and multiple concurrent data moves make it possible to construct processors capable of very high throughput. Parallel processors are especially efficient for array/vector operations or signal processing algorithms requiring complex number arithmetic (e.g., FFT, convolution, correlation, etc.).

The Am29501A's Pipeline Register File provides data storage and pipelining flexibility. Any combination of register instructions, ALU instructions, and I/O instructions can be microprogrammed to occur in the same cycle. This allows overlap of external multiplication, ALU operations, and memory I/O.

Three I/O ports support a wide variety of parallel, pipelined architectures by providing separate I/O ports for the multiplier and the memory data bus. Either of two bidirectional I/O ports, DIO and MIO, can interface to the data bus or multiplier Y-input port, and a separate MI port connects to the multiplier output port.

BLOCK DIAGRAM

BDR02301
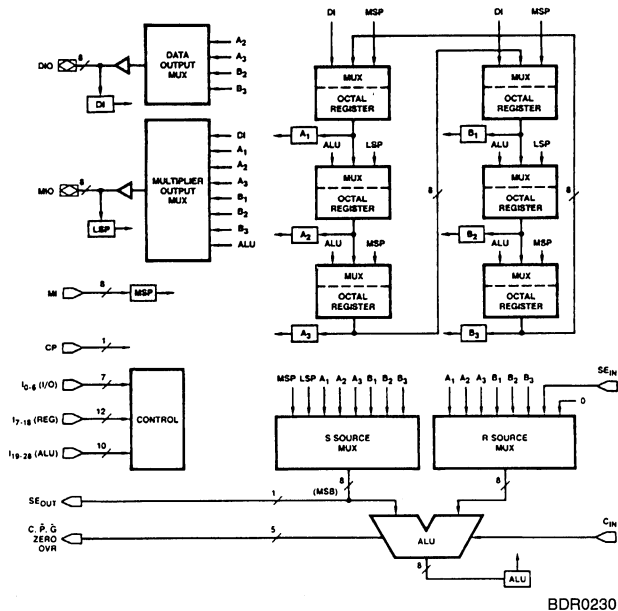
RELATED AMD PRODUCTS

| Part No.	Description
Am25S558, Am25S557	8 x 8-Bit Bipolar Combinatorial Multipliers
Am2902A	Carry Look-Ahead Generator
Am2910A, Am29C10A	Bipolar and CMOS 12-Bit Microprogram Controller
Am29116, Am29L116A, Am29116A, Am29C116, Am29C116A, Am29117, Am29C117	16-Bit Bipolar and CMOS Microprocessors
Am29130	16-Bit Barrel Shifter
Am29516, Am29516A, Am29L516, Am29L516A, Am29517, Am29517A, Am29L517, Am29L517A	16 x 16-Bit Bipolar Parallel Multipliers
Am29C516, Am29C516A, Am29C517, Am29C517A	16 x 16-Bit CMOS Parallel Multipliers
Am29325, Am29C325	32 x 32-Bit Bipolar and CMOS Floating Point Processors
Am29C509	CMOS 12 x 12-Bit MAC
Am29L510, Am29510	Bipolar 16 x 16-Bit MACs
Am29520A, Am29521A, Am29524, Am29525	Multilevel Pipeline Registers
Am29540	FFT Address Sequencer
Am29818, Am29818-1, Am29818A	SSR Diagnostics Pipeline Register

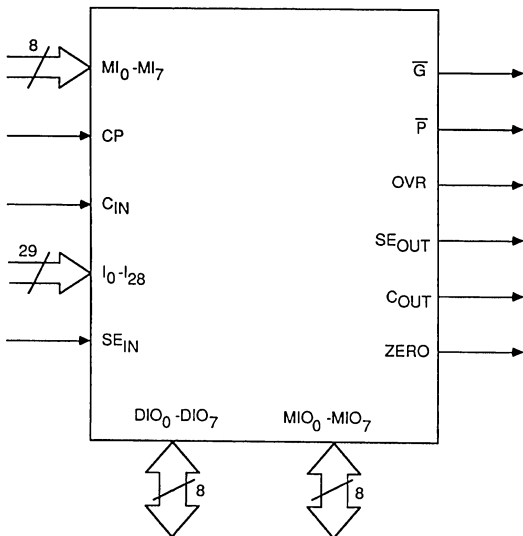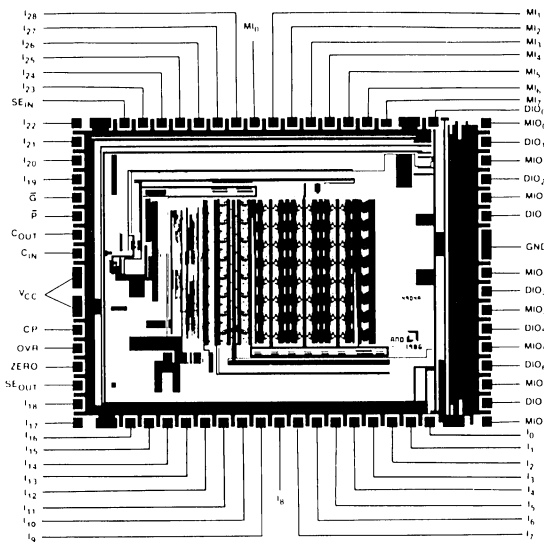# CONNECTION DIAGRAMS
Top View

DIP
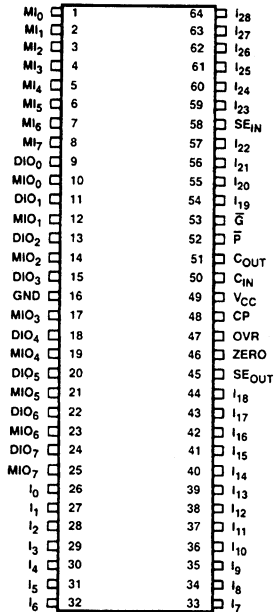
CDR04421

LCC*
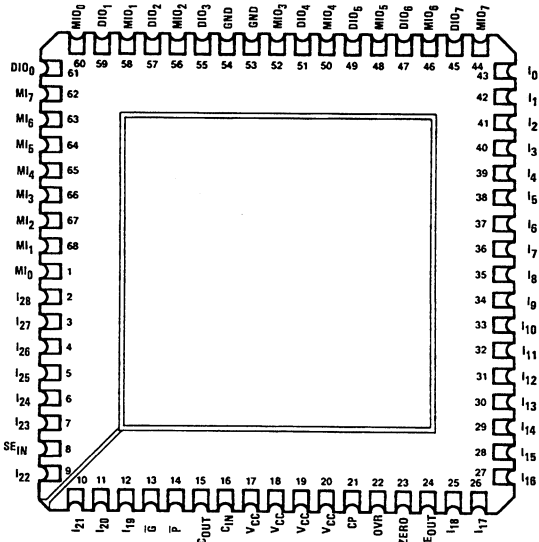
CDR04433

*Also available in 68-Pin PLCC. Pinout is identical to LCC.

LOGIC SYMBOL

MI_0-MI_7 (8)

CP

C_{IN}

I_0-I_{28} (29)

SE_{IN}

$\overline{G}$

$\overline{P}$

OVR

SE_{OUT}

C_{OUT}

ZERO

DIO_0-DIO_7 (8) MIO_0-MIO_7 (8)

LS002990

METALLIZATION AND PAD LAYOUT

Left pads (top to bottom): I_{28}, I_{27}, I_{26}, I_{25}, I_{24}, I_{23}, SE_{IN}, I_{22}, I_{21}, I_{20}, I_{19}, $\overline{G}$, $\overline{P}$, C_{OUT}, C_{IN}, V_{CC}, CP, OVR, ZERO, SE_{OUT}, I_{18}, I_{17}, I_{16}, I_{15}, I_{14}, I_{13}, I_{12}, I_{11}, I_{10}, I_9

Top: MI_0

Right pads: MI_1, MI_2, MI_3, MI_4, MI_5, MI_6, MI_7, DIO_0, MIO_0, DIO_1, MIO_1, DIO_2, MIO_2, DIO_3, GND, MIO_3, DIO_4, MIO_4, DIO_5, MIO_5, DIO_6, MIO_6, DIO_7, MIO_7, I_0, I_1, I_2, I_3, I_4, I_5, I_6, I_7

Bottom: I_8

Die Size: .211″ x .159″
Gate Count: 850

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing

AM29501A   D   C   B

e. OPTIONAL PROCESSING
Blank = Standard processing
B = Burn-in

d. TEMPERATURE RANGE
C = Commercial (0 to +70°C)

c. PACKAGE TYPE
D = 64-Pin Topbrazed Ceramic DIP (TDX064)
J = 68-Pin Plastic Leaded Chip Carrier (PL 068)
L = 68-Pin Ceramic Leadless Chip Carrier (CLT068)

b. SPEED OPTION
Not Applicable

a. DEVICE NUMBER/DESCRIPTION
Am29501A
Multi-Port Pipelined Processor

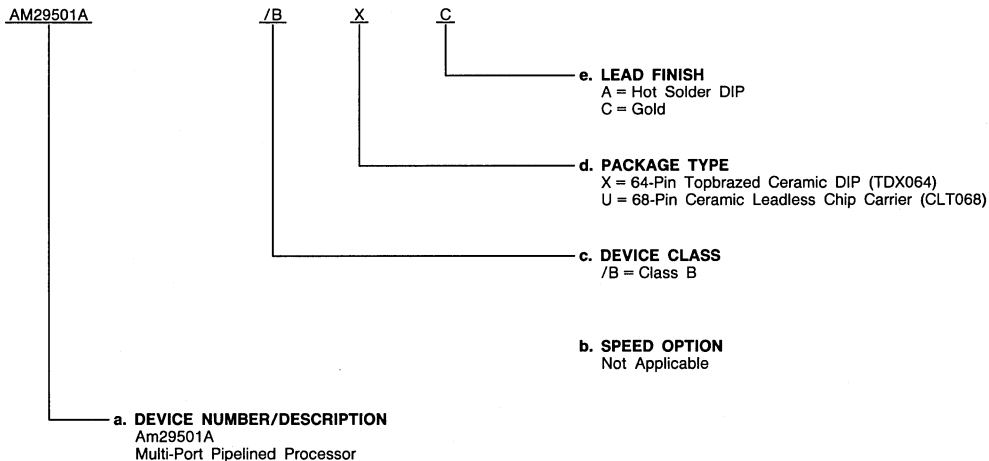| Valid Combinations	
AM29501A	DC, DCB, JC, LC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

3

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish

AM29501A   /B   X   C

e. LEAD FINISH
A = Hot Solder DIP
C = Gold

d. PACKAGE TYPE
X = 64-Pin Topbrazed Ceramic DIP (TDX064)
U = 68-Pin Ceramic Leadless Chip Carrier (CLT068)

c. DEVICE CLASS
/B = Class B

b. SPEED OPTION
Not Applicable

a. DEVICE NUMBER/DESCRIPTION
Am29501A
Multi-Port Pipelined Processor

Valid Combinations	
AM29501A	/BXC, /BUA

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of subgroups 1, 2, 3, 9, 10, 11.

PIN DESCRIPTION

C_{IN} Carry-In (Input)
Input to the internal 8-bit ALU.

C_{OUT} Carry-Out (Output)
Output from the internal 8-bit ALU.

CP   Clock (Input)
Input for the internal pipeline register file. Data selected by $I_7 - I_{18}$, meeting the setup and hold time requirements of the respective register, is clocked into the register on the clock LOW-to-HIGH transition.

$DIO_0 - DIO_7$ Data I/O Port (Input/Output)
This is a general-purpose data port. The names are derived from the typical usage in a typical Am29500 system, but are not restricted to this interconnection scheme.

$\overline{G}, \overline{P}$ Carry $\overline{Generate}$ and $\overline{Propagate}$ (Output; Active LOW)
Outputs of the internal ALU. These signals are used with the Am2902A for carry-lookahead.

$I_0 - I_{28}$ Instruction Inputs (Input)
Designed to be driven under microprogram control. All Instruction inputs control multiplexers or drivers, or the ALU directly. There is no instruction encoding. See Control Input Function Tables for operating modes.

$MI_0 - MI_7$ Multiplier Data Input Port (Input)
This is a general-purpose data port. The names are derived from the typical usage in a typical Am29500 system, but are not restricted to this interconnection scheme.

$MIO_0 - MIO_7$ Multiplier Data I/O Port (Input/Output)
This is a general-purpose data port. The names are derived from the typical usage in a typical Am29500 system, but are not restricted to this interconnection scheme.

OVR   Overflow (Output)
This pin is logically the Exclusive-OR of the carry-in and carry-out of the MSB of the ALU. At the most significant end of the word, this pin indicates that the result of an arithmetic two's-complement operation has overflowed into the sign-bit.

SE_{OUT} Sign Extension (Output)
The most-significant bit of the S-operand. This is used in multiple precision arithmetic operations for sign extension of two's-complement operations.

SE_{IN} Sign Extension (Input)
A single-bit input which generates an 8-bit sign extension R-operand for multiple precision two's-complement arithmetic operations.

ZERO   Zero (Output; Open Collector)
This is an open-collector output which goes HIGH if the data on the ALU outputs are all LOW.

CONTROL INPUT FUNCTION TABLES

1. Data I/O Port (DIO) Output Select			
I_3	I_2	I_0	Source
L	L	L	A_2
L	H	L	A_3
H	L	L	B_2
H	H	L	B_3
X	X	H	Output Disabled

2. Multiplier I/O Port (MIO) Output Select				
I_6	I_5	I_4	I_1	Source
L	L	L	L	A_1
L	L	H	L	A_2
L	H	L	L	A_3
L	H	H	L	B_1
H	L	L	L	B_2
H	L	H	L	B_3
H	H	L	L	ALU
H	H	H	L	DI
X	X	X	H	Output Disabled

3. Register A_1 Data Source Select		
I_8	I_7	Source
L	L	MSP (MI)
L	H	DI (DIO)
H	L	B_3
H	H	A_1 (Hold)

4. Register A_2 Data Source Select		
I_{10}	I_9	Source
L	L	LSP (MIO)
L	H	ALU
H	L	A_1
H	H	A_2 (Hold)

5. Register A_3 Data Source Select

I_{12}	I_{11}	Source
L	L	MSP (MI)
L	H	ALU
H	L	A_2
H	H	A_3 (Hold)

6. Register B_1 Data Source Select

I_{14}	I_{13}	Source
L	L	MSP (MI)
L	H	DI (DIO)
H	L	A_3
H	H	B_1 (Hold)

7. Register B_2 Data Source Select

I_{16}	I_{15}	Source
L	L	LSP (MIO)
L	H	ALU
H	L	B_1
H	H	B_2 (Hold)

8. Register B_3 Data Source Select

I_{18}	I_{17}	Source
L	L	MSP (MI)
L	H	ALU
H	L	B_2
H	H	B_3 (Hold)

9. ALU Operating Instructions

I_{22}	I_{21}	I_{20}	I_{19}	OP	C_{OUT}	$\overline{P}$	$\overline{G}$	
L	L			$R + S + C_{IN}$				
L	H			$R - S - C_{IN}$				
H	L	L	L	$R + C_{IN}$	Carry	$\overline{P}$	$\overline{G}$	Normal Operating Mode**
H	H			$-R + S - C_{IN}$				
L	L			$R + S + C_{IN}$				Inhibit Carry Mode
L	H			$R - S - C_{IN}$				
H	L	L	H	$R + C_{IN}$	L	H	H	
H	H			$-R + S - C_{IN}$				
L	L			$R + S + C_{IN}$				Force Carry Mode
L	H			$R - S - C_{IN}$				
H	L	H	L	$R + C_{IN}$	H	$\overline{P}$	L	
H	H			$-R + S - C_{IN}$				
L	L			R XOR S				Logic Operations
L	H			R AND S				
H	L	H	H	$\overline{R}$	(L)*	(H)*	(H)*	
H	H			R OR S				

*C_{OUT}, $\overline{P}$, and $\overline{G}$ are not applicable to logic operation; Am29501A functions as shown.
**Carry is used for 16-bit expansion. $\overline{P}$ and $\overline{G}$ are used with an Am2902A for expansion to more than 16 bits.

10. ALU R Operand Selection

I_{25}	I_{24}	I_{23}	Source
L	L	L	A_1
L	L	H	A_2
L	H	L	A_3
L	H	H	B_1
H	L	L	B_2
H	L	H	B_3
H	H	L	Sign Extend Input Bussed to All Bits
H	H	H	Arithmetic Zero (All Inputs LOW)

11. ALU S Operand Selection

I_{28}	I_{27}	I_{26}	Source
L	L	L	A_1
L	L	H	A_2
L	H	L	A_3
L	H	H	B_1
H	L	L	B_2
H	L	H	B_3
H	H	L	MSP (MI)
H	H	H	LSP (MIO)

FUNCTIONAL DESCRIPTION

Figure 1 contains a block diagram of the Am29501A. It shows four major sections – an 8-bit cascadable ALU, a register file consisting of six 8-bit registers, three I/O ports, and a microcode control section.
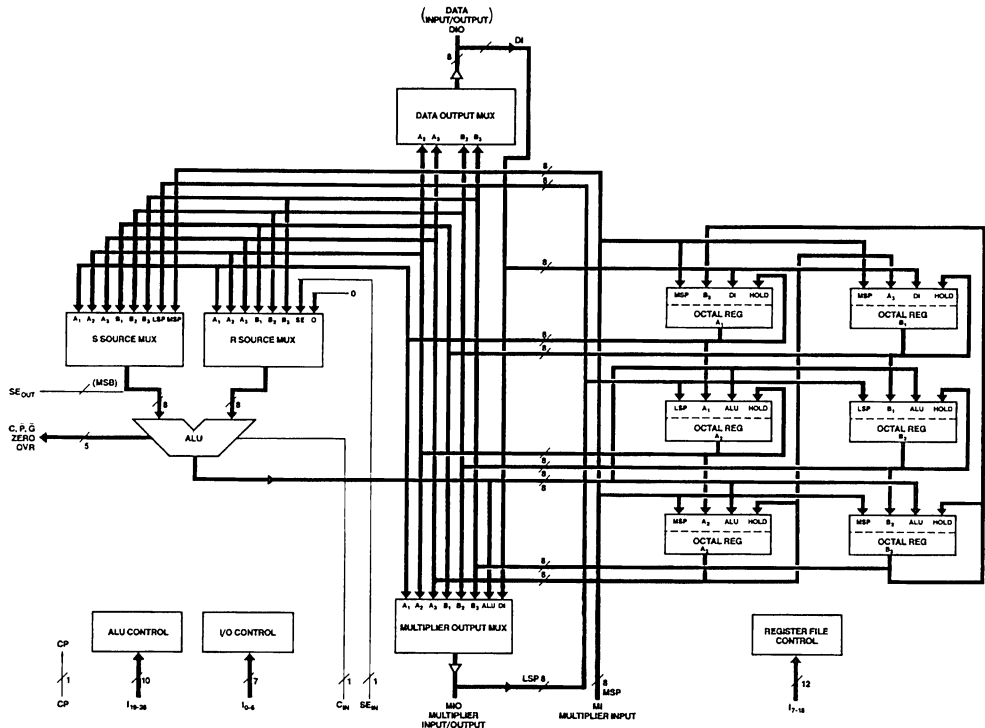
DFR00711

Figure 1. Detailed Am29501A Block Diagram

ALU

The ALU performs arithmetic on an 8-bit Byte-Slice^{TM} with full internal carry lookahead, and carry input and output for cascading. The carry can ripple between byte-slices by connecting the C_{OUT} of one slice to C_{IN} of the next byte-slice. Carry generate ($\overline{G}$) and propagate ($\overline{P}$) outputs are also provided for faster operation when the ALU is used in conjunction with a carry lookahead generator such as the Am2902A.

There are three arithmetic modes — cascade, carry inhibit, and forced carry. The cascade mode produces an output carry based on the results of the operation, and is the normal mode. The carry inhibit mode produces no carry output, and is used to decouple cascaded ALUs. A 16-bit ALU consisting of two Am29501As can operate as two 8-bit ALUs simultaneously by programming the carry inhibit mode. This mode could also be used with a second 16-bit ALU for double precision where the more significant slice is programmed in the carry inhibit mode for single precision, and in the cascade mode for double precision. The less significant slices would be programmed in normal mode for either case. The forced carry mode is the converse; it always produces a carry. All three modes treat the input carry in the same way. The Am29501A uses the input

carry as a true borrow during subtraction as opposed to most two's-complement ALUs which use $\overline{borrow}$. The usual requirement is that input borrow be programmed HIGH (inactive) when doing a subtraction. Since the Am29501A has a true borrow, the input carry is programmed to be LOW for both addition and subtraction. This is consistent with the carry inhibit mode discussed previously.

In addition to arithmetic operations, the ALU also does bitwise logic operations — OR, AND, exclusive-OR, and invert. Carries are not applicable for these operations and are inactive. Codes to program the ALU function are contained in Control Input Function Table 9.

Each operand of the ALU has eight possible sources. Operand R can be any register in the register file, or one of the I/O ports MI or MIO, as shown in Table 10. Operand S can be any register, zero, or a sign extension input (SE_{IN}) from another ALU (Table 11). The ALU result can be steered to registers A2, A3, B2, and B3 of the register file or the MIO I/O port.

Register File

The register file provides for fully independent use of the registers. Each register has a four-input MUX which can be programmed so that the register holds its previous contents,

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or is loaded from the ALU and I/O port, or the "preceding" register. If all registers are programmed for the preceding register, a ring is formed and data circulates through all the registers. This facilitates the construction of a pipelined data flow. Various combinations of I/O ports and the ALU make up the remaining inputs to each register. The sources for each register are shown in the Control Input Function Tables 3–8.

I/O Ports

The Am29501A has two bidirectional ports (DIO and MIO) and one input port (MI). As an input, the DIO port can be loaded into registers A1 and B1 and directed to the MIO output port. Output from the DIO comes from registers A2, A3, B2, or B3 using the codes from Control Input Function Table 1. This separation of input and output registers connected to the DIO port is in keeping with the pipelined organization of the part when the DIO port is used for data flow in and out of the processor.

Input through the MIO port can be directed to registers A2 and B2 in the register file and to the ALU. Output can come from any of the six registers, the DIO input port, or from the ALU. This structure allows the user to direct operands to an auxiliary processor (such as a multiplier or barrel shifter) from any point in the pipeline. The MIO port could be connected to a processor with a bidirectional data bus. The auxiliary processor would receive data and return its results to registers A2 and B2 through the MIO port.

The MI port provides another entry point for inserting data in the processing pipeline. An auxiliary processor with flow-through architecture could receive data from the MIO port and return data through the MI port, which can be directed to registers A1, A3, B1, and B3, and to the ALU.

A potential use of the ports would be to connect the bidirectional bus of an Am29116A microprocessor to the MIO port. An Am29516A would have its inputs connected to the same MIO port and its output to the MI port. This architecture could calculate magnitudes by computing the sum of the squares with the Am29516A and Am29501A and the square root with the Am29116A.

Control

The Am29501A is controlled by 29 microcode bits which select operations with no encoding. This provides the maximum flexibility for the independent control of parallel operations. Sources may be directed to multiple destinations simultaneously wherever data paths are provided.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature .... −65 to +150°C
Temperature Under Bias-T_C .... −55 to +125°C
Supply Voltage to Ground Potential
  Continuous .... −0.5 to +7.0 V
DC Voltage Applied to Outputs For
  HIGH Output State .... −0.5 V to +V_{CC} Max.
DC Input Voltage .... −0.5 to +5.5 V
DC Output Current, Into Outputs .... 30 mA
DC Input Current .... −30 to +5.0 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
  Temperature
    DIPs (T_A) .... 0°C to +70°C
    Chip Carriers (T_C) .... 0°C to 85°C
  Supply Voltage (V_{CC}) .... +4.75 V to +5.25 V

Military (M) Devices
  Temperature (T_C) .... −55°C to +125°C
  Supply Voltage (V_{CC}) .... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Thermal Resistance (Typical) – TDX064
  $\theta_{JA} = 10°C/W$
  $\theta_{JC} = 35°C/W$

DC CHARACTERSITICS over operating range unless otherwise specified (Included in Group A, Subgroups 1, 2, 3 are tested unless otherwise noted).

Parameter Symbol	Parameter Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min. $V_{IN} = V_{IH}$ or V_{IL}		$I_{OH} = -2.6$ mA	2.4			Volts
V_{OL}	Output Low Voltage	V_{CC} = Min.	COM'L	$I_{OL} = 24$ mA			0.5	Volts
			MIL	$I_{OL} = 16$ mA			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = Min., $I_{IN} = -18$ mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = Max., $V_{IN} = 0.5$ V					−500	μA
	Input LOW Current (CP)						−800	μA
I_{IH}	Input HIGH Current	V_{CC} = Max., $V_{IN} = 2.7$ V					20	μA
I_I	Input HIGH Current	V_{CC} = Max., $V_{IN} = 5.5$ V					0.1	mA
$I_{CEX(Z)}$	Output OFF	V_{CC} = Min., $V_O = 5.5$ V					250	μA
I_{OZL}	Off State (High Impedance) Output Current	V_{CC} = Max.		$V_O = 0.5$ V			−500	μA
I_{OZH}				$V_O = 2.4$ V			100	
I_{SC}	Output Short-Circuit Current (Note 3)	V_{CC} = Max. + 0.5 V		$V_O = 0.5$ V	−20		−85	mA
I_{CC}	Power Supply Current (Note 5)	COM'L Only V_{CC} = MAX		$T_A = 0$ to 70°C (Note 4)			400	mA
				$T_A = +70°C$ (Note 4)			375	
		MIL Only V_{CC} = MAX		$T_C = -55$ to +125°C			420	
				$T_C = 125°C$			360	

Notes: 1. For conditions shown as Min. or Max., use the appropriate value specified under Operating Ranges for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0$ V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short-circuit test should not exceed one second.
4. Chip Carriers: $T_C = 85°C$.
5. All outputs LOW; three-state outputs disabled.

Minimum Setup/Hold Times and Maximum Propagation Delays

From Input	Setup, t_s/Hold, t_h		Propagation Delay Times, t_{PD}										Units
	Register Input	Reg via ALU	MIO Port	MIO via ALU	DIO Port	C_{OUT}	$\bar{P}$	$\bar{G}$	Z	Overflow	SE_{OUT}		
CLK			18	25	18	22	22	22	25	25	18	ns
DIO	10/5		15									ns
MIO	10/5	15/5				21	21	21	25	25	18	ns
MI	10/5	15/5		25		22	22	22	25	25	18	ns
C_{IN}		10/5		18		16			21	21		ns
SE_{IN}		15/5		20		18	18	18	22	15		ns
I_{2-3}(DIO)					16							ns
I_{4-6}(MIO)			16									ns
I_{7-18}(REG)	10/5											ns
I_{19-22}(ALU OP)		15/5		25		20	22	22	25	20		ns
I_{23-28}(ALU SEL)		15/5		25		20	22	22	25	20	18	ns
$I_0 - I_1$ Enable			20		20							ns
$I_0 - I_1$ Disable			25		25							ns

Minimum Setup/Hold Times and Maximum Propagation Delays

From Input	Setup, t_s/Hold, t_h		Propagation Delay Times, t_{PD}										Units
	Register Input	Reg via ALU	MIO Port	MIO via ALU	DIO Port	C_{OUT}	$\bar{P}$	$\bar{G}$	Z	Overflow	SE_{OUT}		
CLK			21	28	21	25	25	25	28	28	21	ns
DIO	12/6		18									ns
MIO	12/6	18/6				24	24	24	28	28	21	ns
MI	12/6	18/6		28		25	25	25	28	28	21	ns
C_{IN}		12/6		21		19			24	24		ns
SE_{IN}		18/6		23		21	21	21	25	18		ns
I_{2-3}(DIO)					19							ns
I_{4-6}(MIO)			19									ns
I_{7-18}(REG)	12/6											ns
I_{19-22}(ALU OP)		18/6		28		23	25	25	28	23		ns
I_{23-28}(ALU SEL)		18/6		28		23	25	25	28	23	21	ns
$I_0 - I_1$ Enable			23		23							ns
$I_0 - I_1$ Disable			28		28							ns

Am29501A Minimum Clock Pulse Widths

Parameter	Description		TYPICAL	COMMERCIAL	MILITARY	Units
t_{PW}	Clock Pulse Width	HIGH		15	18	ns
		LOW		15	18	ns

SWITCHING TEST CIRCUITS

TCR01342

TC001421
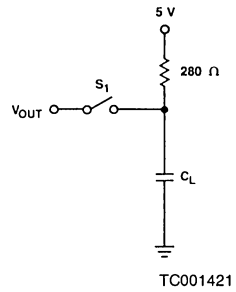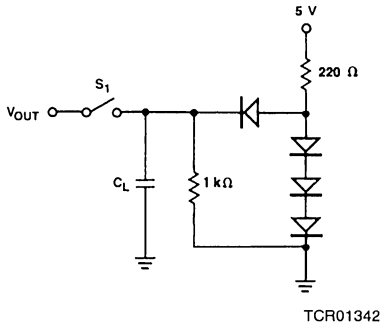
A. Three-State and Normal Outputs

B. Open-Collector Outputs
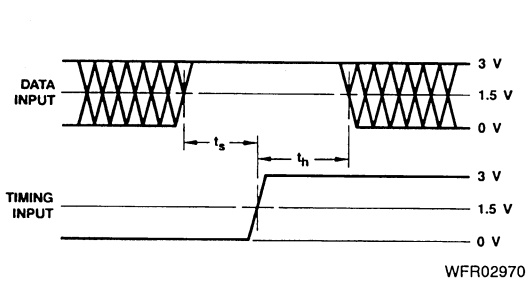
Notes: 1. $C_L = 50$ pF includes scope probe, wiring, and stray capacitances without device in test fixture.

SWITCHING TEST WAVEFORMS
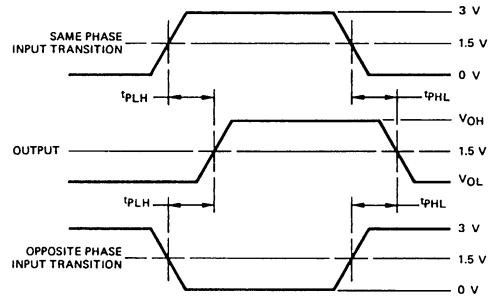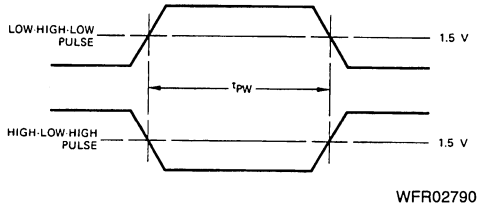

WFR02970

Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross-hatched area is don't care condition.
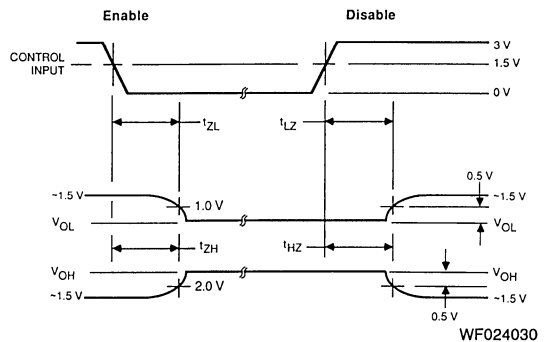
Setup, Hold, and Release Times

WFR02980

Propagation Delay

WFR02790

Pulse Width

WF024030

Notes: 1. Diagram shown for Input Control Enable-LOW and Input Control Disable-HIGH.

Enable and Disable Times

NOTE: 1. Pulse generator for all pulses: Rate $\leqslant 1.0$ MHz; $Z_O = 50 \ \Omega$; $t_r \leqslant 2.5$ ns; $t_f \leqslant 2.5$ ns.

Test Philosophy and Methods

The following points give the general philosophy that we apply to tests which must be properly engineered if they are to be implemented in an automatic enviroment. The specifics of what philosophies applied to which test are shown in the data sheet.

1. Ensure the part is adequately decoupled at the test head. Large changes in V_{CC} current as the device switches may cause erroneous function failures due to V_{CC} changes.

2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.

3. Do not attempt to perform threshold tests at high speed. Following an output transition, ground current may change by as much as 400 mA in 5-8 ns. Inductance in the ground cable may allow the ground pin at the device to rise by hundreds of millivolts momentarily.

4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leqslant 0$ V and $V_{IH} \geqslant 3.0$ V for AC tests.

5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.

6. Capacitive Loading for AC Testing
Automatic testers and their associated hardware have stray capacitance which varies from one type of tester to another but is generally around 50 pF. This makes it impossible to make direct measurements of parameters that call for smaller capacitive load than the associated stray capacitance. Typical examples of this are the so-called "float delays" which measure the propagation delays into the high-impedance state and are usually specified at a load capacitance of 5.0 pF. In these cases, the test is performed at the higher load capacitance (typically 50 pF) and engineering correlations based on data taken with a bench setup are used to predict the result at the lower capacitance.

Similarly, a product may be specified at more than one capacitive load. Since the typical automatic tester is not capable of switching loads in mid-test, it is impossible to make measurements at both capacitances even though they may both be greater than the stray capacitance. In these cases, a measurement is made at one of the two capacitances. The result at the other capacitance is predicted from engineering correlations based on data taken with a bench set up and the knowledge that certain DC measurements (I_{OH}, I_{OL}, for example) have already been taken and are within spec. In some cases, special DC tests are performed in order to facilitate this correlation.

7. Threshold Testing
The noise associated with automatic testing (due to the long, inductive cables) and the high gain of the tested device when in the vicinity of the actual device threshold, frequently give rise to oscillations when testing high-speed circuits. These oscillations are not indicative of a reject device, but instead, of an overtaxed test system. To minimize this problem, thresholds are tested at least once for each input pin. Thereafter, "hard" high and low levels are used for other tests. Generally this means that function and AC testing are performed at "hard" input levels rather than at V_{IL} Max. and V_{IH} Min.
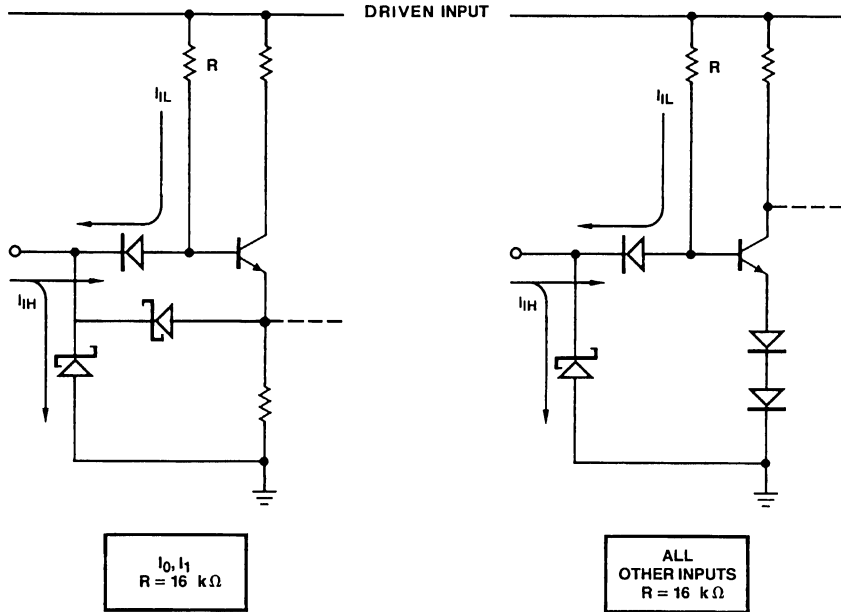
8. AC Testing
Occasionally, parameters are specified which cannot be measured directly on automatic testers because of tester limitations. Data input hold times often fall into this category. In these cases, the parameter in question is guaranteed by correlating these tests with other AC tests which have been performed. These correlations are arrived at by the cognizant engineer by using data from precise bench measurements in conjunction with the knowledge that certain DC parameters have already been measured and are within spec.

In some cases, certain AC tests are redundant since they can be shown to be predicted by other tests which have already been performed. In these cases, the redundant tests are not performed.
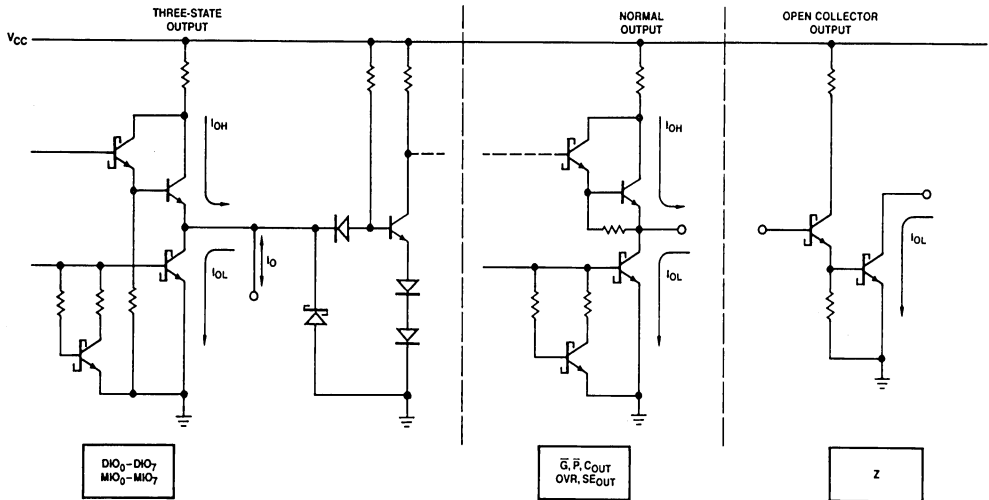
9. Output Short-Circuit Current Testing
When performing I_{OS} tests on devices containing RAM or registers, great care must be taken that undershoot caused by grounding the high-state output does not trigger parasitic elements which in turn cause the device to change state. In order to avoid this effect, it is common to make the measurement at a voltage (V_{output}) that is slightly above ground. The V_{CC} is raised by the same amount so that the result (as confirmed by Ohm's law and precise bench testing) is identical to the $V_{OUT} = 0$, $V_{CC} =$ Max. case.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

$$I_0, I_1$$
$$R = 16 \ k\Omega$$

ALL
OTHER INPUTS
$$R = 16 \ k\Omega$$

ICR00534

$$C_I \cong 5.0 \ pF, \ all \ inputs$$

THREE-STATE
OUTPUT

NORMAL
OUTPUT

OPEN COLLECTOR
OUTPUT

$$DIO_0 - DIO_7$$
$$MIO_0 - MIO_7$$

$$\overline{G}, \overline{P}, C_{OUT}$$
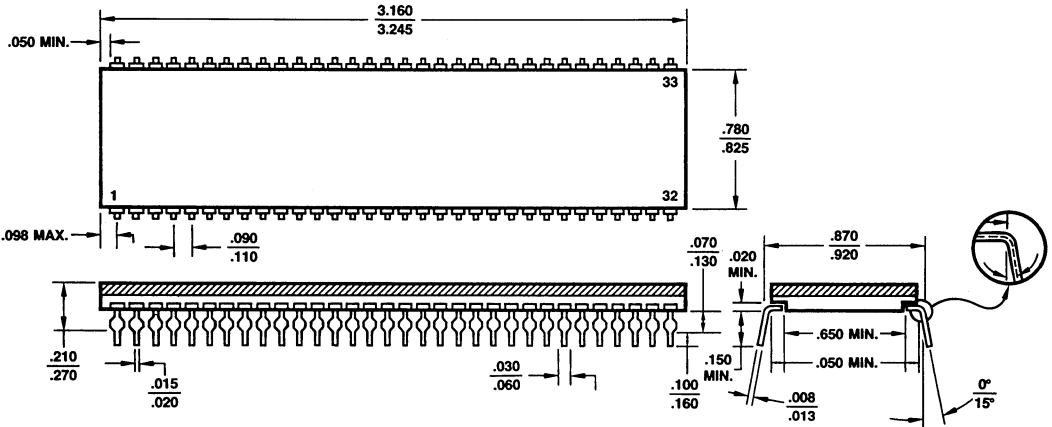$$OVR, SE_{OUT}$$

Z

ICR00520

$$C_O \cong 5.0 \ pF, \ all \ outputs$$
Note: Actual current flow direction shown.

PHYSICAL DIMENSIONS*

TDX064

PID # 06844A

PL 068

TOP VIEW
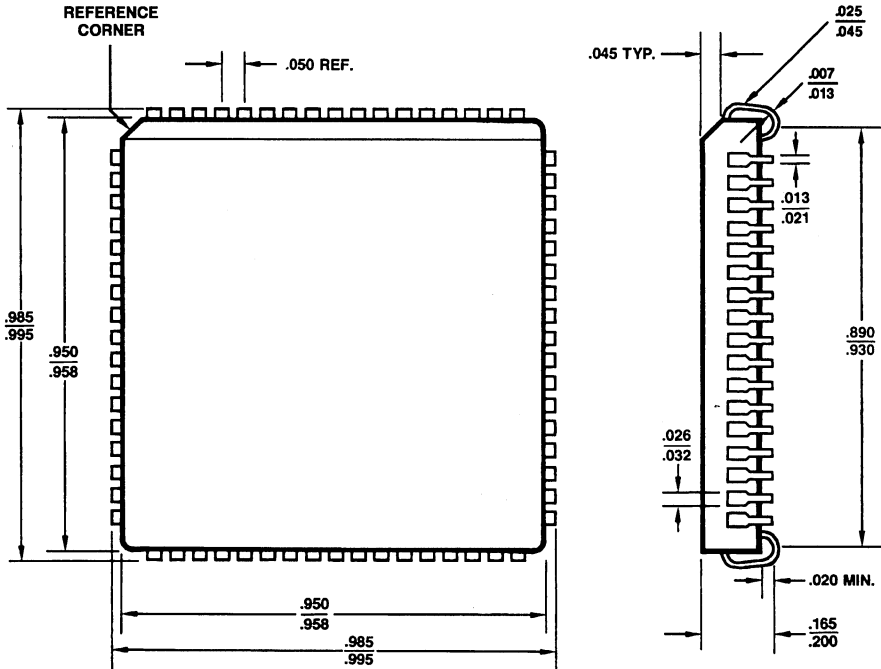
REFERENCE
CORNER

PID # 06753E

*For reference only.

PID # 08214A

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